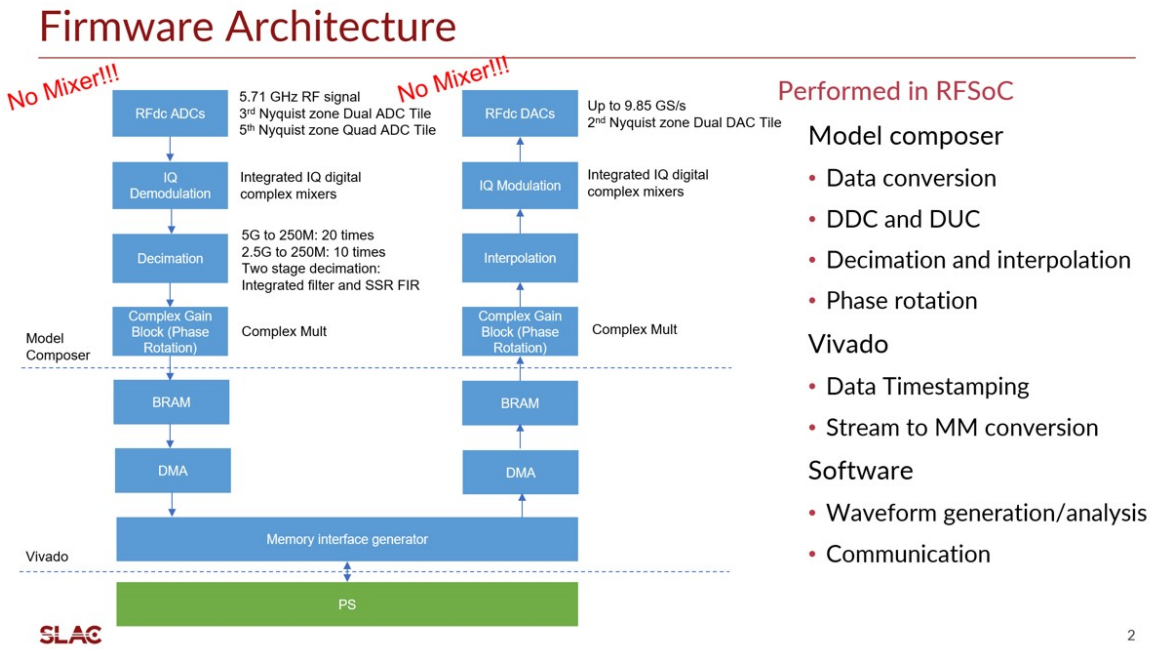

Figure 1: The block diagram of the RFSoC based LLRF control firmware.

RFSoC based LLRF control for DARPA

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Abstract

This document describes the high level design concepts of the RFSoC based low level RF (LLRF) control for ACCEL. Some of the critical technical aspects are discussed with more details.

1 Introduction

2 Firmware design

The RFSoC based low lever RF control firmware begins with the flow chart shown in Figure 1.

2.1 RF ADC sampling

The RF signal from the Klystrons is centred at 5.712 GHz and requires a bandwidth of 100 MHz minimum. The RF signal can be directly sampled by a 5 GS/s ADC at the 3rd Nyqusit zone or a 2.5 GS/s ADC at 5th Nyqusit zone. The

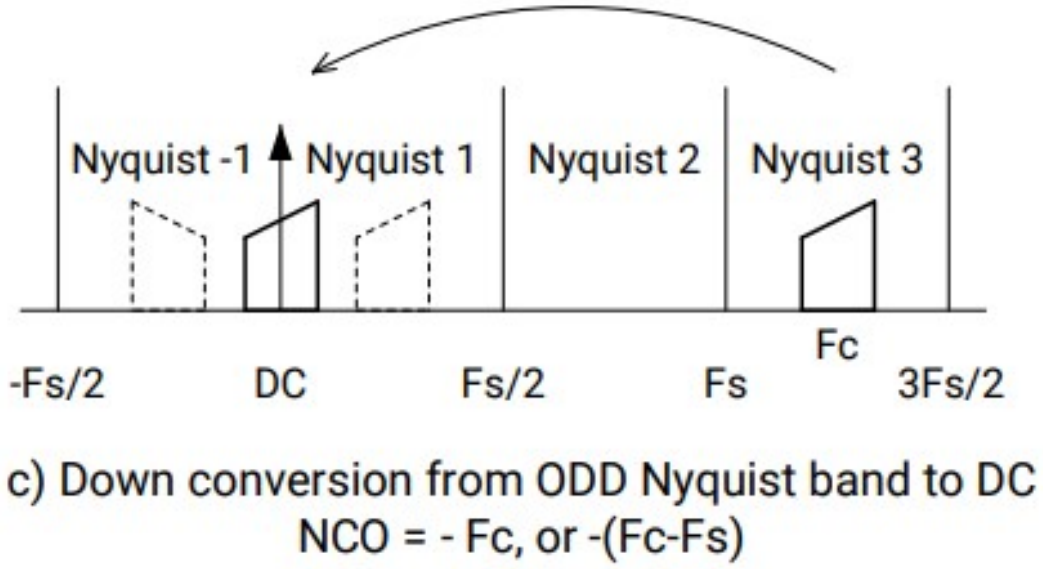


Figure 2: DDC from the odd Nyquist zones to DC bands.

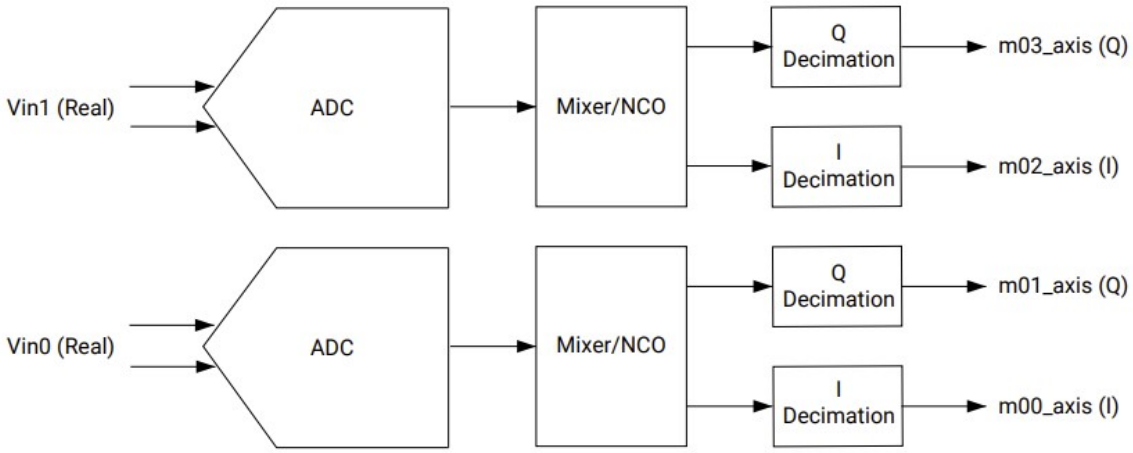


Figure 3: Dual RF-ADC Real Input to I/Q Output

Gen3 parts of RFSoC has the ADCs with analogue input bandwidth at 6 GHz. The ADCs use image aliased from 3rd or 5th Nyquist zone to the 1st Nyquist zone for digitizing, which is shown in Figure 2.

2.2 Digital Down Conversion with IQ mixing and Decimation

For the LLRF control system, the ADC needs to be configured to real to I/Q output mode as shown in Figure 3. The figure demonstrate the configuration for a tile of 5 GS/s dual RF-ADC part and the 2.5 GS/s quad RF-ADC part can be configured with the same mode. Figure 4 shows the data timing for the out AXI-Stream interfaces. The I and Q components are clocked independently with multiple samples per clock cycle. The I and Q components are generated by an integrated quadrature mixer with NCO with coarse and fine frequency control. As Figure 3 shown, there are decimation stages for the I and Q components for each of the ADCs.

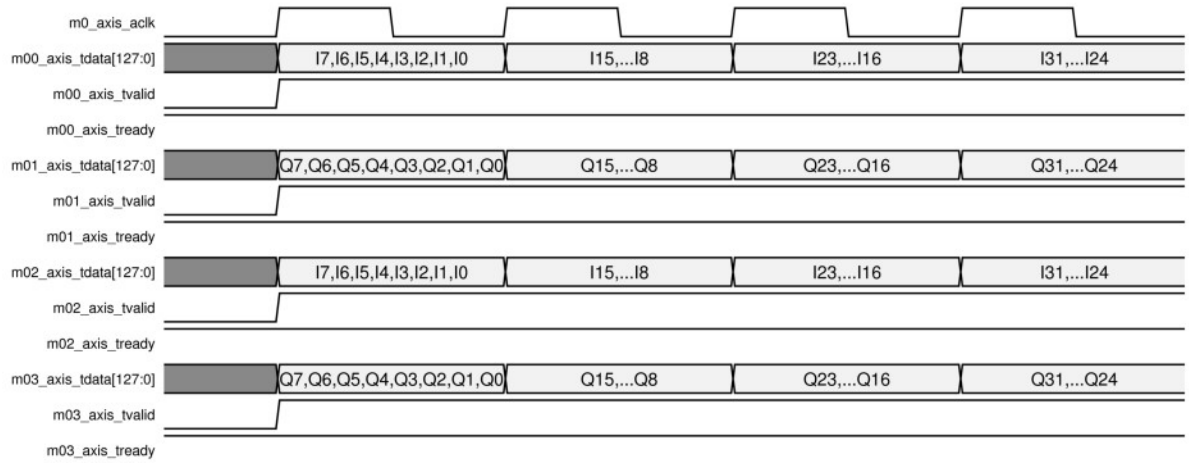


Figure 4: Dual RF-ADC Real Input to I/Q Output Data Timing

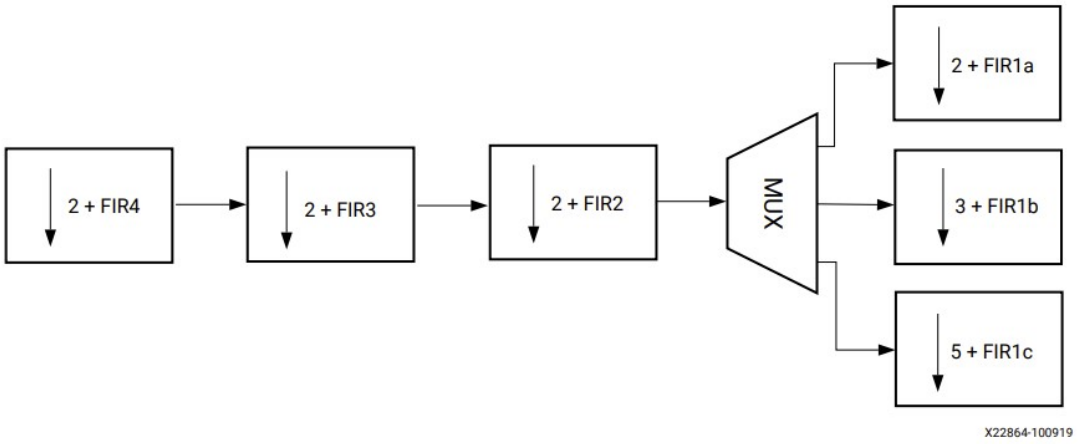


Figure 5: Decimation Filters Hierarchy (Gen 3)

The decimation circuit for each of the components is shown in Figure 5. There are four stages connected in series and any of those stages can be bypassed. The last stage can be selected from decimation factors of 2, 3 and 5. The overall decimation factor can be selected from the product of the decimation factors at each of the stages. The frequency responses for the stages are shown in Figure 6, 7 and 8. The decimation stages act as low pass filters and the cutoff frequency of the filter is roughly the Nyquist frequency divided by the decimation factor.

2.3 Simulation Model for RFdc IP

3 Measurement Results by Dan

Dan did the test with loopback setup shown in Figure 12. The test used the ZCU216 evaluation board, which has 16 2.5 GHz ADC and 16 10 GHz DACs. The test was done by using Xilinx RF data converter evaluation Labview UI. The ADC was configured to sample at 2.4576 GHz and the DAC was set to sample at 9.8304 GHz. The reference clock used are independently supplied to ADC and DAC tiles, but the reference frequency used is common at 245.76 MHz.

DAC samples was created that contained a 500 ns long pulse. The pulse does not have 50 % duty cycle pulse and on the DAC side the samples can be loaded is 16384 which at 9.8304 GS/s is only 1.66 us. The 5.712 GHz signal was generated at 4.1184 GHz calculated by using Equation 1. The bandpass filter shown in Figure 12 is used to filter out the images so ADC can digitize 5.712 GHz at the fifth Nyquist zone.

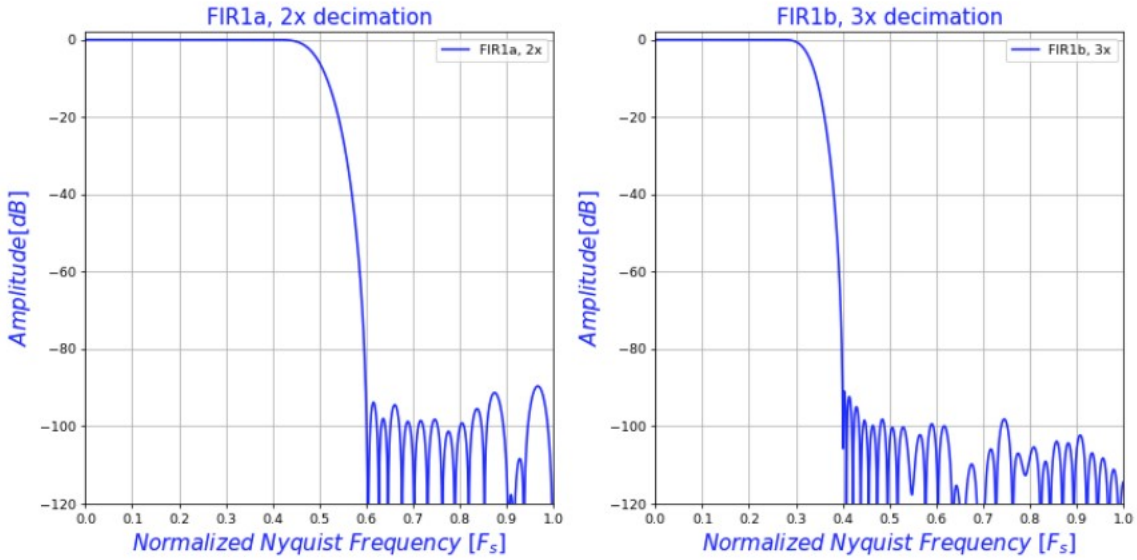


Figure 6: FIR 1a and FIR 1b Frequency Response (Gen 3)

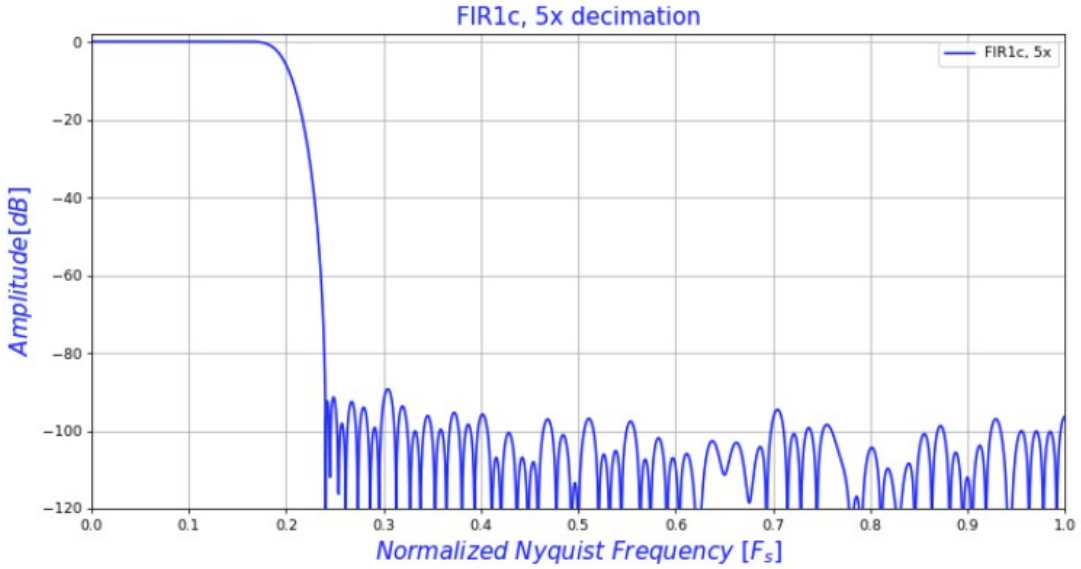


Figure 7: FIR 1c (5x) Frequency Response (Gen 3)

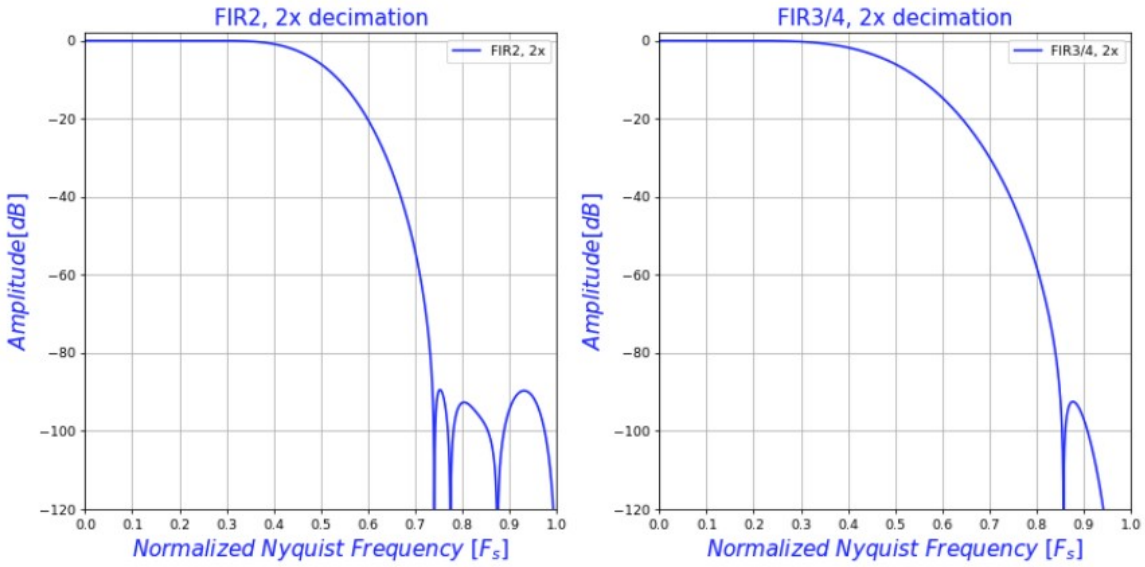


Figure 8: FIR 2, 3 and 4 Frequency Response (Gen 3)

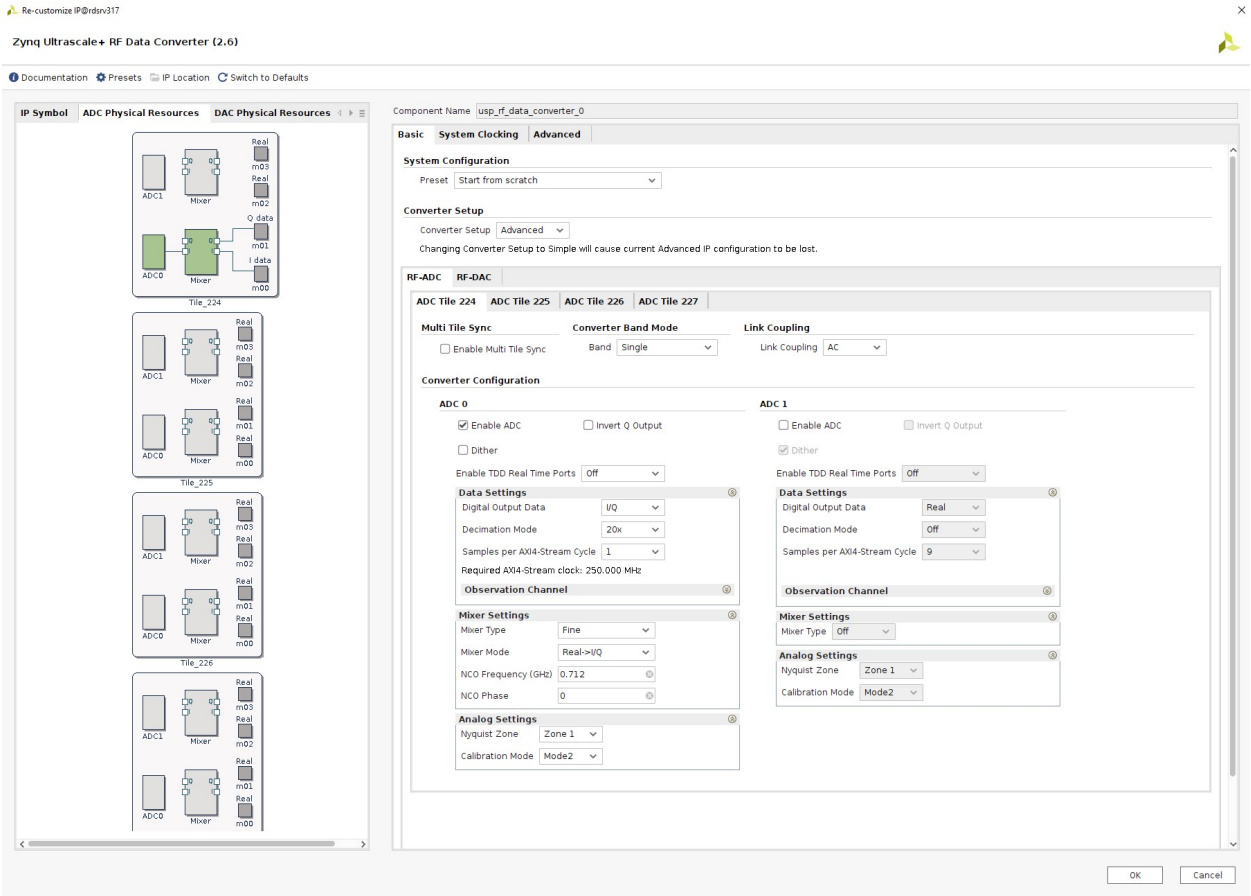


Figure 9: RFdc IP configuration

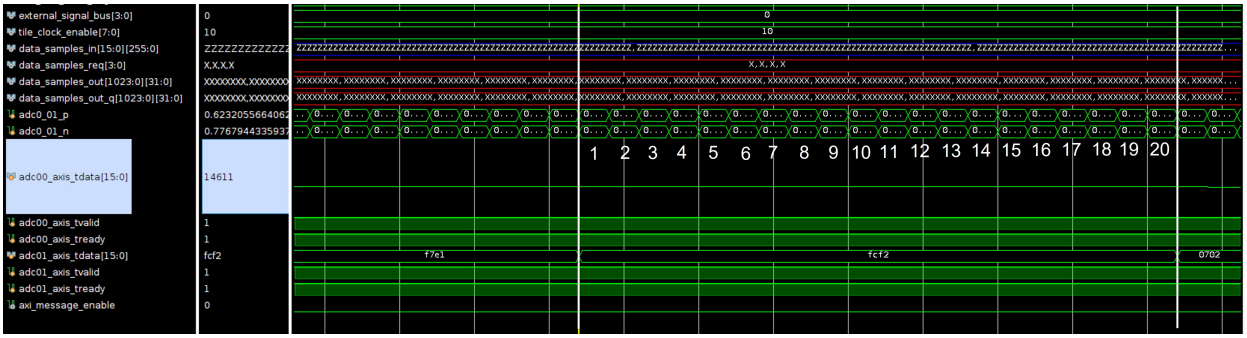


Figure 10: Simulation waveform window

Figure 11: Simulation waveform window

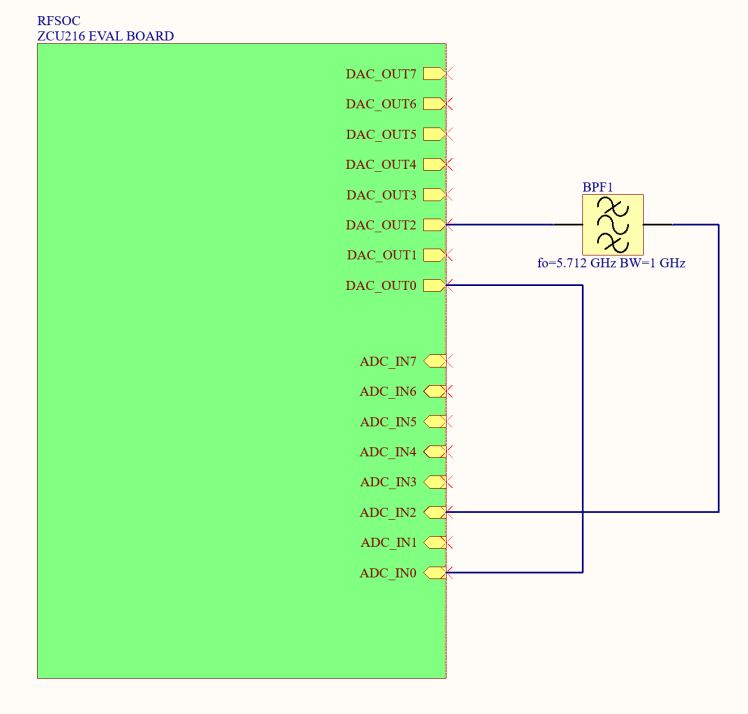


Figure 12: Dan's loop back test setup.

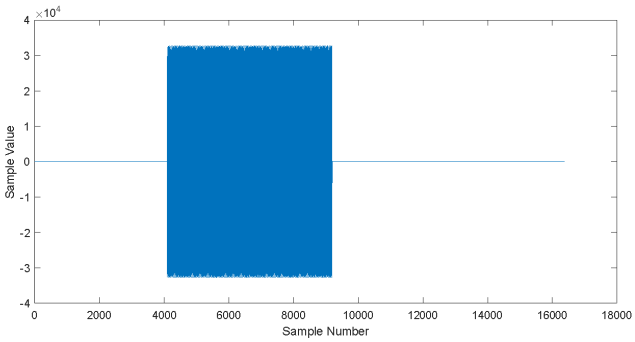


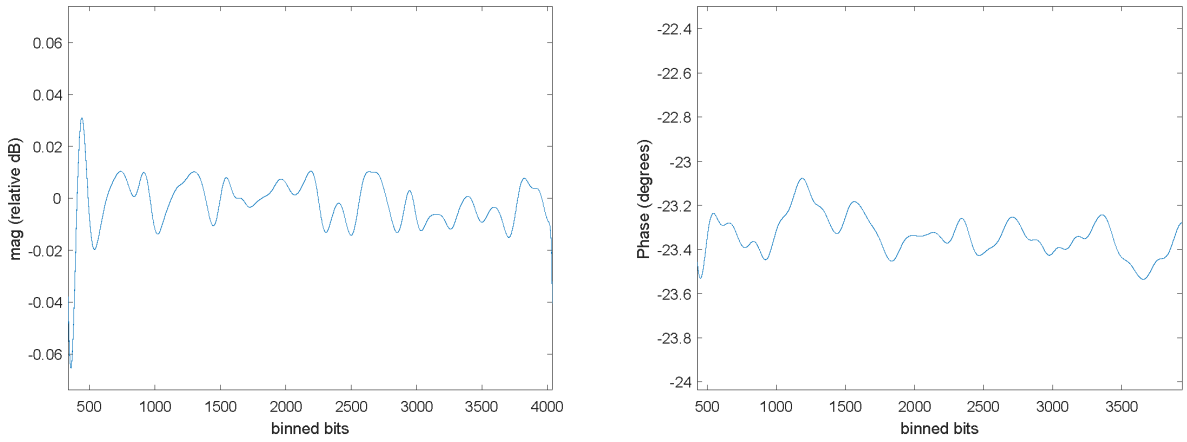
Figure 13: The samples loading to the DAC. The segment with signal has a frequency of 4.1184 GHz then mirrored to 5.712 GHz with respect to the Nyquist rate of the DAC. The rest of the signal are just 0s.

The ADC samples are then processed in Matlab with a bandpass filter centred at the Nyquist signal and then converted to IQ by multiplying by sine and cosine waves. Before the phase and amplitude were extracted, 150 MHz low pass filter was applied. This is equivalent to average the signal as the common control algorithm implementation, and the equivalent integration time needs to be confirmed or the moving average can be implemented in Matlab. The amplitude and phase stability test results are shown in Figure 15a and 15b. The variation in amplitude is $\pm$ 0.02 dB (about 0.05 %) and the phase variation is 0.5 degree, which are much better than 1 % and 1 degree requirement. Those figures can still be optimized using integration and filtering in the DSP.

$$F_{DAC} = F_{Nyquist} - (F_{desired} - F_{Nyquist}) \tag{1}$$

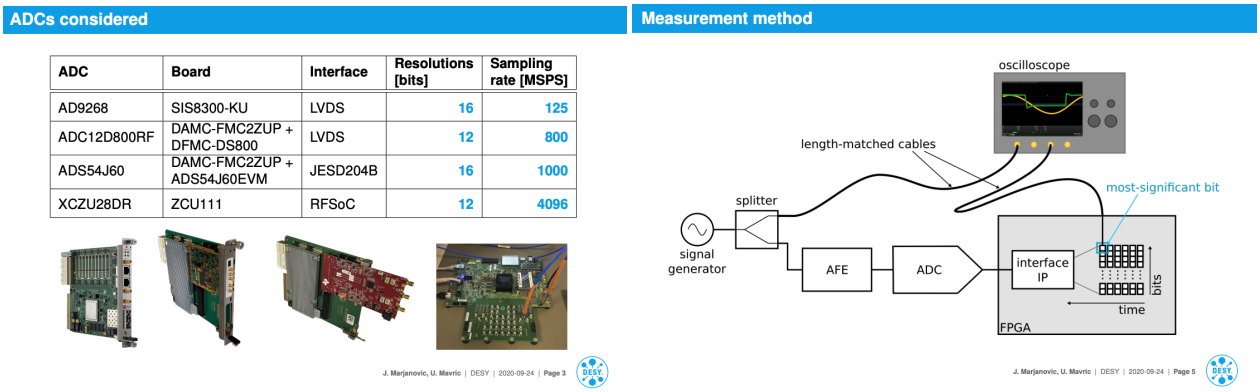
4 DESY's work in Latency Comparison of ADCs with Different Interfaces

DESY summarized their work in characterizing the ADC and frontend latency for applications (e.g. LLRF, Klystron Lifetime Management), in which the latency of the entire signal processing chain (ADC+FPGA (DSP algorithm)+DAC)



(a) Amplitude (b) Phase

Figure 14: Amplitude variation in 4000 samples. The best phase and amplitude stability achieved when the DAC was used in 2nd Nyqusit zone.



(a) ADC under test (b) Test setup

Figure 15: DESY's ADC tested and the test setup

is very important at `https://indico.desy.de/event/25669/contributions/57935/attachments/37380/46665/ard_st3_adc_latency.pdf`. The tested ADCs and test setup used are shown in Figure 15a and 15b. The test results are summarised in Figure 16.

5 Review of Kukhee's Algorithm

6 Design considerations

Power Consumption

The comparsion between Figure 17 and 18 shows how RF-sampling converters can be implemented in 9W versus 36W using discrete solutions.

Reference `https://docs.xilinx.com/v/u/en-US/wp489-rfsampling-solutions`

Choice of RFSoC SOM for phase 2 implementation

In the perspective of SWAP, the SOM with 16-Channel 2.5GS/s A/D and 9.8GS/s D/A Zynq UltraScale+ RFSoC Gen 3 is a better choice than the SOMs with 8 channel RFSoC Gen3. The 16 channel SOM can cover all the 52 RF input and 26 RF out channels with 4 SOMs, while 7 of 8 channel SOMs will be need. Using 16 channel SOM not only saves size

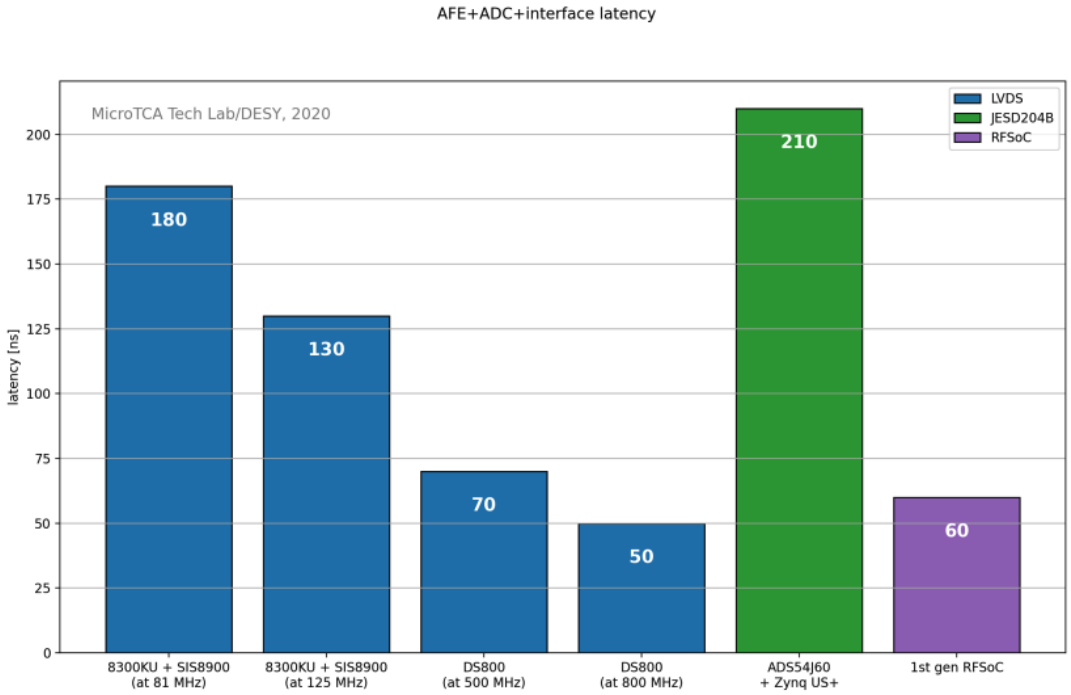


Figure 16: The comparison between the delay of the LVDS, JESD and RFSoC interfaces.

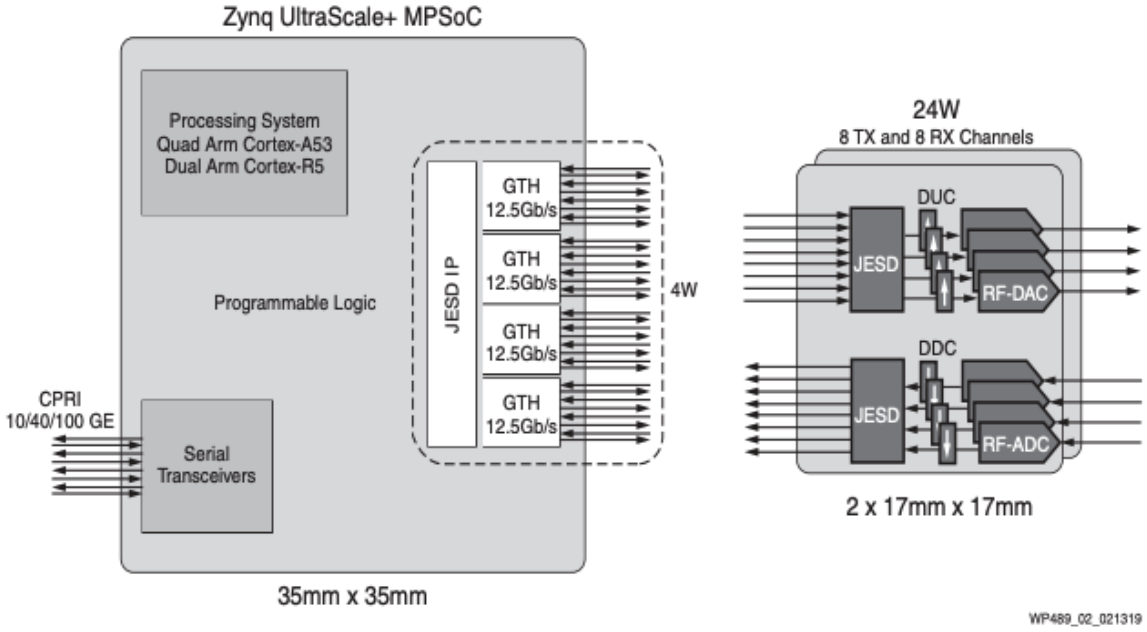


Figure 17: Power consumption of discrete ADCs with JESD solution.

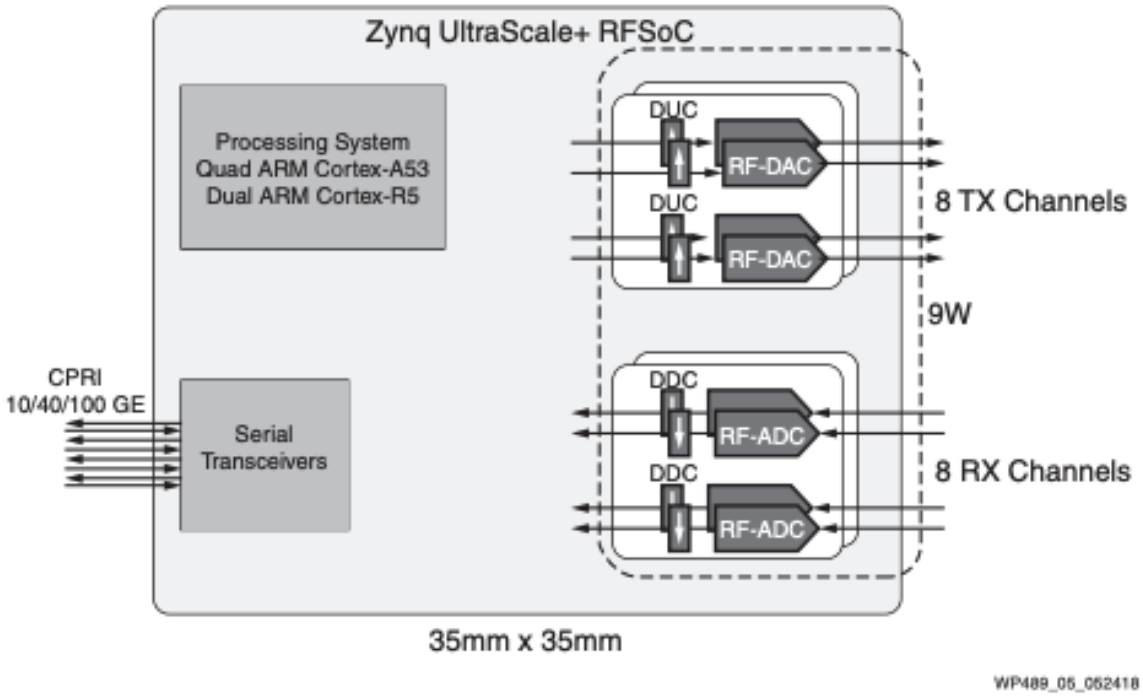


Figure 18: Power consumption of RFSoC solution.

and weight, but also power. With 16 channel SOM, we can cover twice the number of channels with similar amount of power compared with a single 8 channel SOM.

Pentek 6003 `https://www.pentek.com/products/detail.cfm?model=6003`

- 8-Channel 5GS/s A/D and 9.8GS/s D/A Zynq UltraScale+ RFSoC Gen 3
- 8G PL DDR and 8G PS DDR
- Deselected due to NDA requirements

Avnet XRF16 RFSoC System-on-Module `https://www.avnet.com/wps/portal/us/products/avnet-boards/avnet-board-families/xrf-soms/xrf16-gen3-som/`

- 16-Channel 2.5GS/s A/D and 9.8GS/s D/A Zynq UltraScale+ RFSoC Gen 3
- 4G PL DDR and 4G PS DDR
- 26 weeks lead time
- price $ 29,995

Avnet XRF8 RFSoC System-on-Module `https://www.avnet.com/wps/portal/us/products/avnet-boards/avnet-board-families/xrf-soms/xrf8-gen3-som/`

- 8-Channel 5GS/s A/D and 9.8GS/s D/A Zynq UltraScale+ RFSoC Gen 3
- 4G PL DDR and 4G PS DDR
- 77 weeks lead time
- price $ 27,495

The number of samples loading to the DAC

There are two ways input samples are stored and replayed:

Sample counts	Sample (b)	Bram (b)	Bram (Mb)	Bram in RFSoC (Mb)	Sample rate	Sequence duration (us)	Bram for x16 channels (Mb)
16384	16	262144	0.262	38	9.8304E+09	1.666666666666	4.192
65536	16	1048576	1.0486	38	9.8304E+09	6.666666666666	16.7776

Figure 19: Required BRAM calculated for 16384 and 65536 DAC sample storage.

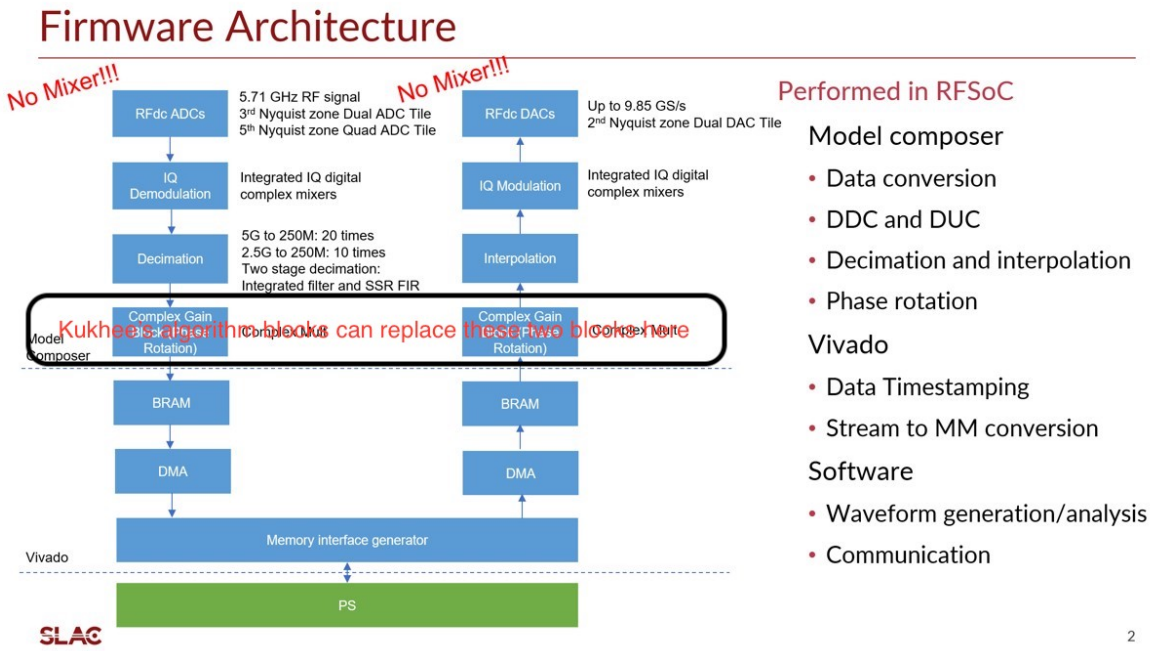


Figure 20: The high level firmware implementation plan.

- Samples are stored and looped over in PL DDR (high storage but reduced speed).
- Samples are stored and looped over in block RAM (low storage but highest speed).

If we need to replay all the 8 DACs at 9.8 GS/s simultaneously, the BRAM loopback play should be the way to go. Even if the PL DDR can be deterministic, but it can still be limited by the bandwidth of the interface. The PL DDR memory size varires between SOM to SOM. If there PL DDR on SOM, it is normally 4Gb or more. The BRAM in RFSoC is 38 Mb or less and it can running tight if the sample sequence is 6 μs or more and all 16 DACs are running as shown in Figure 19. However, we will only need 8 of DAC running simultaneously, so the BRAM reburied is about 8.5 Mb or so. That should be achievable with the BRAM available in RFSoC. Larry also suggested to move the AXI-Lite to DAC clock domain to enable the use of URAM if we have BRAM shortage in the future. The BRAM solution can consume less power than the PL DDR solution, which is favoured by the battery powered instrument.

7 Development Plan

Plan

Characterize the ADC and DAC performance with integrated DDC

- Review Dan's data/results.
- Recover Dan's test setup (find the bandpass filter centred at 5.712 GHz)
- Update the firmware with RFdc has DDC enabled
- Characterize the performance of the data converters in the mode we would like to use for LLRF control system

Architect the system firmware, software, clock distribution and trigger

Define the specification of the control algorithm with Kukhee

Define the interface between DDC and HLS control block

Develop a ADC and DAC loopback prototype with DUC and DDC

Integrate the loopack firmware with HLS blocks

Integrate the firmware with software running on processor (Kukhee can guide Radiobeam to develop the software) - the integration need to be finished by July 2023

References