RFSoC Data Converter Characterization for LLRF Control for DARPA ACCEL

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Abstract

This document describes the characterization results of the data converters integrated in the RFSoC targeted the low level RF (LLRF) control for DARPA ACCEL. The LLRF control requires both ADCs and DACs, as well as some of the digital down conversion (DDC) and digital up conversion (DUC) blocks integrated in RFSoC's data paths.

1 Introduction

The characterization of data converters begins with a DAC and ADC loop back test setup. The data path are configured with data converters enabled only for the first stage and then more blocks are enabled in the later stages.

2 Data Converter Characterization Setup

2.1 DAC-ADC Loop-back Setup

The LLRF control electronics requires both ADC and DAC, so the characterization starts with a loop-back setup. The centre frequency of the DARPA system is 5.712 GHz. As the DAC can only be operated in the first and second Nyquist zones, the DAC is operated at 9.8304 GS/s, which is quite close to the maximum speed of the DAC. The ADCs integrated in the ZU49DR device has a maximum sampling rate of 2.5 GS/s and analog input bandwidth of 6 GHz. The 5.712 GHz centre band with 100 MHz bandwidth can be digitized at the fifth Nyqusit zone when the ADC is operated at frequency close to 2.5 GS/s. For the convenience of clock generation, the ADC is operated at 2.4576 GS/s. As Figure 1 shows, the RF signal generated by a DAC and looped back to an ADCs via 4900 MHz to 6200 MHz band-pass filter.

The DAC samples are generated using a Matlab script and the exported file is converted to TDMS before load to the DAC. In this case, pulse train with 50%, 75% and 100% duty cycle. The CW wave signal within the pulse has the frequency of 5.712 GHz. When the duty cycle is set to 100 percent, the DAC signal will be a CW wave. The 5.712 GHz cannot generated directly, as the frequency is in the second Nyquist zone of the DAC. The actual frequency loaded to the DAC can be calculated by Equation 1 at 4.1184 GHz. By setting the DAC to Nyqusit zone 2, the mix mode of DAC is enable to push the power from first Nyquist zone to the second.

The choice of balun is critical, as the inappropriate choice of balun can attenuate the signal of interest. The setup shown in Figure 1 is used for the first set measurement, which is actually with the 10 MHz - 1GHz balun. The balun attenuate the signal significantly and the characterization results can be impacted. The test has been repeated with 5-6 GHz balun as shown in Figure . The test results with those two setups will be discussed separately in results section. In general, we need to be very careful about the RF signal routing on board and choice of balun on custom board or carrier board we select for version 2.0 of the LLRF control for DARPA.

2.2 Clock Generation

A clock system is essential for any digital systems. The clocks signal generation for this characterization test starts with the clocks for the data converters. In this case, the clocks for the data converters are generated by using PLLs and clock

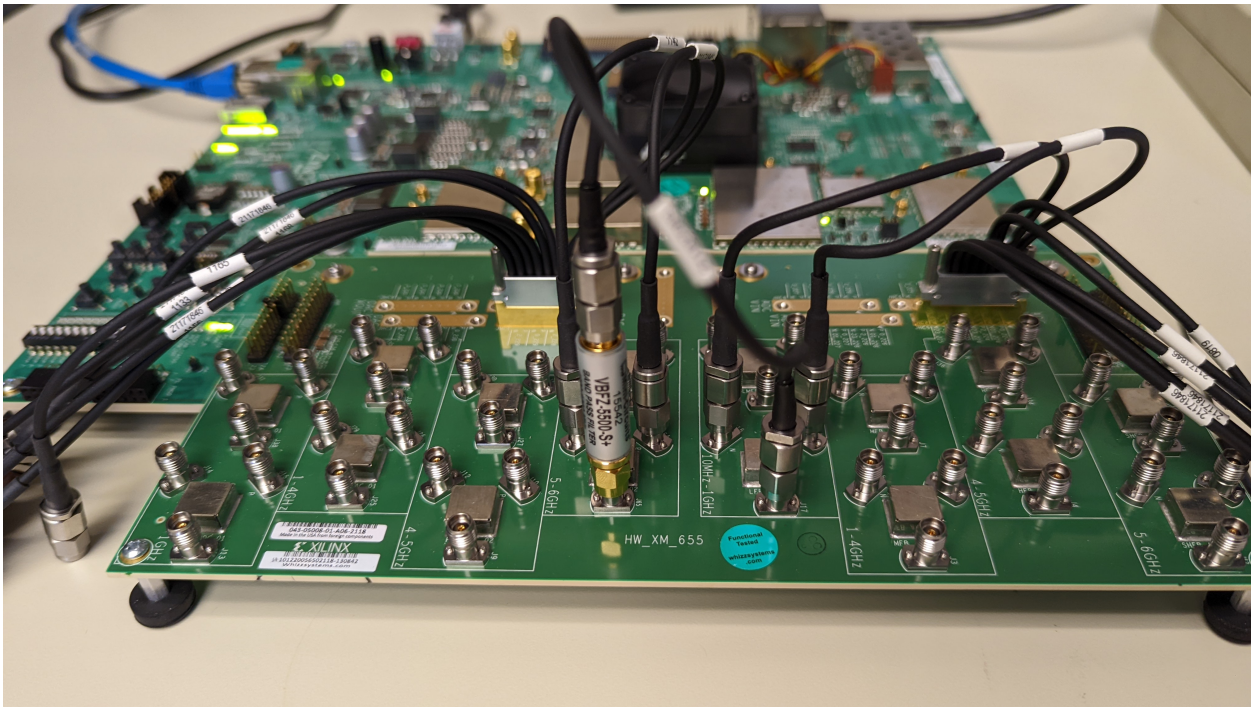


Figure 1: The DAC output looped back to ADC through a band-pass filter.

propagation functions included in Gen3 RFSoC as shown in Figure 2. A reference clock at 245.76 MHz generated by external PLL for each of ADC Tile 2 and DAC Tile 2 and then reference clock propagates to the rest of the data converter tiles. The PLL per tile uses the reference clock to generate the desired sampling clocks per data converter. As mentioned in the previous section, the sampling rate for DAC is 9.8304 GS/s and 2.4576 GS/s for ADC, which are the targeted clock to be generated by the PLLs integrated in each data converter tile of RFSoC.

2.3 Data Converter Configuration

The test starts with the simplest configuration with only ADC and DAC enabled and all the other blocks bypassed. The test aims to characterize the standalone performance of data converter. The DDC and DUC can always be implemented in PL if the integrated ones in the data-path are not perform as expected. Figure 3 shows the data path setup for DAC as an example and ADC data path is very similar with that.

$$F_{DAC} = F_{Nyquist} - (F_{desired} - F_{Nyquist}) \tag{1}$$

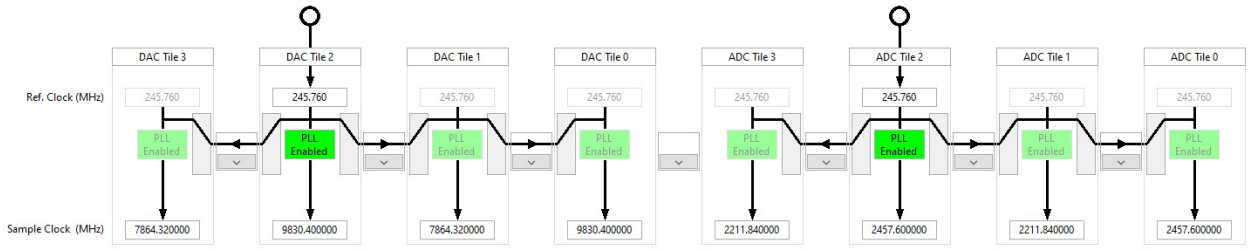
2.4 Digital Down Conversion Data Path Configuration

Since there are integrated DDC and DUC, we can use them without any extra cost in resources. In this case, the DDC is characterized with ADC data path. As Figure 4 shown, the mixer is enabled in fine mode with NCO at 796.8 MHz, which the 5.712 GHz signal aliased back to the first Nyquist zone. The mixer down-mix the signal to IF and generates both I and Q components of the IF signal. The I and Q components are still 2.4576 GS/s sample rate after the mixer. However, the IF signal do not need such a high data rate anymore, so a 10x decimation is enabled and the data rate after it is 245.76 MS/s. The DAC is still used with no DUC chain in this set of test.

3 Characterization Results with Off-line IQ Demodulation

3.1 DAC Sample Loading, ADC Sample Capturing and

The objective of this test is to characterize the magnitude and phase stability of the data converters for LLRF control application. The pulse width for DARPA is around 5 μs. The requirement for phase stability is within 1 degree and 1 %



Tile	Sample Clock (MHz)	PLL	Ref. Clock (MHz)	Source Tile	Distribute Clock
DAC Tile 3	7864.320000	☑	245.760	DAC Tile 2	None
DAC Tile 2	9830.400000	☑	245.760	DAC Tile 2	Input Ref. Clock
DAC Tile 1	7864.320000	☑	245.760	DAC Tile 2	None
DAC Tile 0	9830.400000	☑	245.760	DAC Tile 2	None
ADC Tile 3	2211.840000	☑	245.760	ADC Tile 2	None
ADC Tile 2	2457.600000	☑	245.760	ADC Tile 2	Input Ref. Clock
ADC Tile 1	2211.840000	☑	245.760	ADC Tile 2	None
ADC Tile 0	2457.600000	☑	245.760	ADC Tile 2	None

Figure 2: Clock generation regime for the data converters.

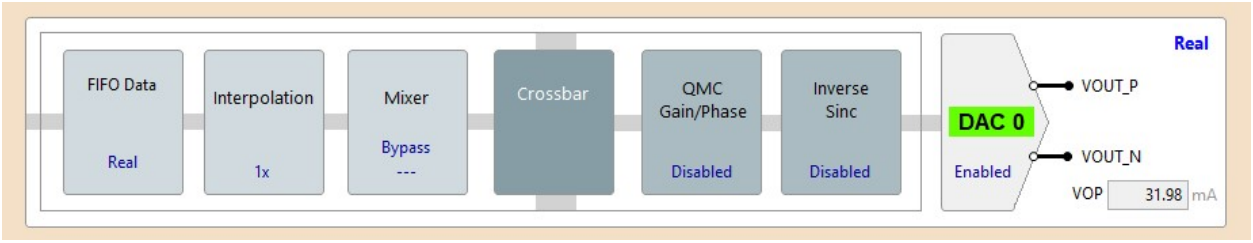


Figure 3: The configurations for the DAC used for characterization.

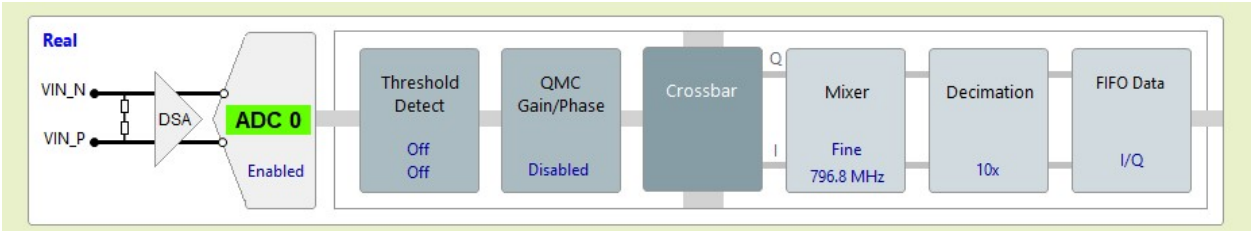


Figure 4: The configurations for the ADC data path used for characterizing the whole DDC chain.

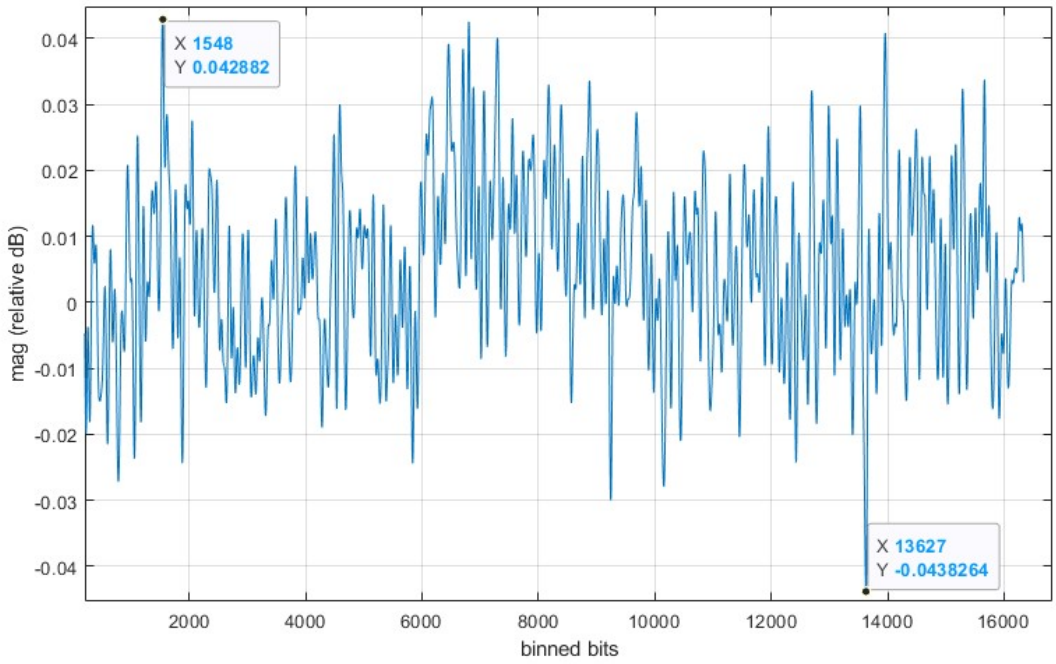


Figure 5: Magnitude fluctuation when the DAC generate the signal is set to the first Nyquist zone.

for magnitude. The software and firmware used for testing has load and capture of 16,384 samples. For DAC sampling at 9.8304 GS/s, about 1.67 μs of samples can be loaded to the DAC. For ADC samples at 2.4576 GS/s, about 6.67 μs of continuous samples can be captured from the ADC. If we load the pulsed signal with 50 % or 75 % of duty cycle, we cannot evaluate the stability of time longer than 1.67 μs. Therefore, the sequence of the carrier or the pulse with 100 % duty cycle at 5.712 GHz, is played from the DAC. The ADC samples is captured continuously for 6.67 μs. Although there will be some mismatch between the end of each of DAC sample loading cycle to the start of following one, it can give us an idea of the stability over 6.67 μs, which is long enough for the LLRF control application.

3.2 Test Results with 10MHz to 1 GHz Balun on ADC side

The incorrect balun used for the results in this section. However, the results are kept in this document for future reference.

3.3 Test Results with 5 to 6 GHz Balun on ADC side

The baluns used for both both DAC and ADC sides are 5-6 GHz.

Figure 9 shows the magnitude fluctuation over 6.67 μs with the DAC configured to the first and second Nyquist zones. As the figure shows, when the DAC is set to zone 1, the fluctuation in magnitude ranges between $\pm$ 0.047 dB which equivalent to $\pm$ 0.5 %. That is definitely within the 1 % specification of DARPA. When the DAC is set to zone 2, it should improve the magnitude stability but it acts reversely as the magnitude fluctuation increase to $\pm$ 0.1 dB. Figure 10 and 11 show the fluctuation in phase, which are about 0.5 and 0.6 degree of variation for DAC set to zone 1 and zone 2 respectively. The variations in phase in both zone 1 and zone 2 are within the 1 degree requirement of DARPA. Figure 12 shows the comparison between the magnitude fluctuations of test with different balun used on ADC side. Supurisingly, the magnitude fluctuation whne using 10 Mhz to 1 GHz balun is very similar with the results when using 5-6 GHz balun.

References

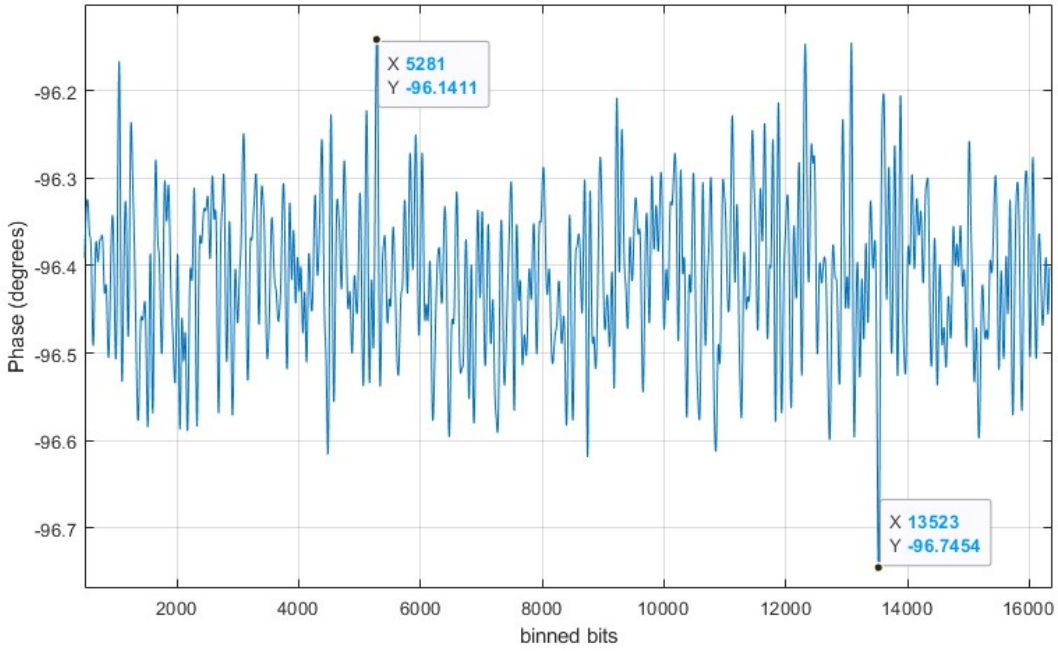


Figure 6: Phase fluctuation when the DAC generate the signal is set to the first Nyquist zone.

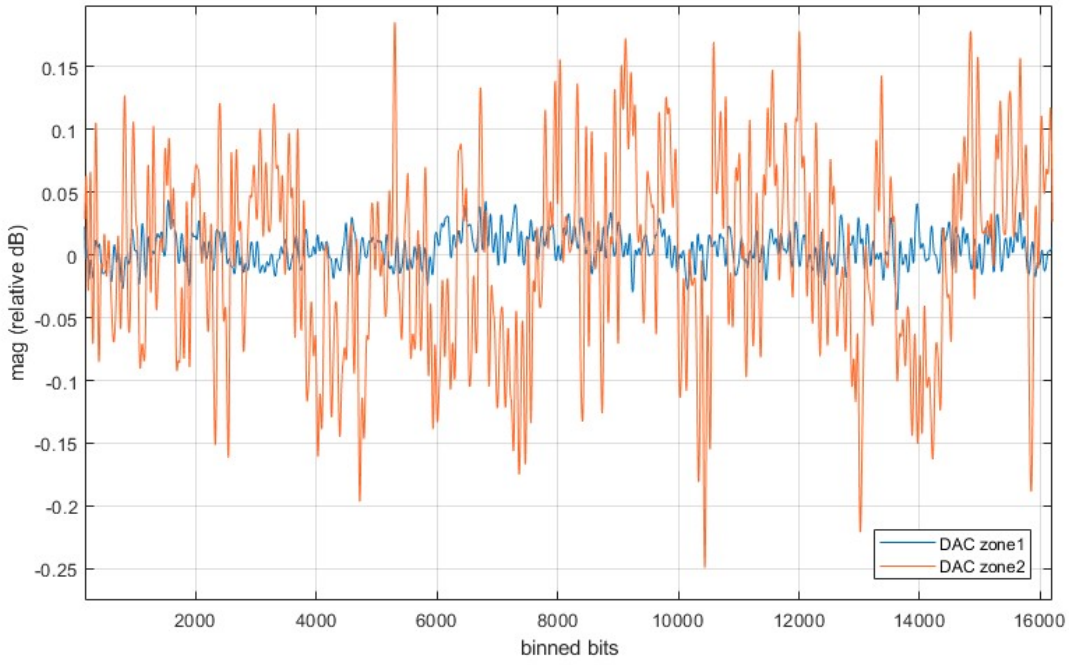


Figure 7: The comparison between the magnitude fluctuation with DAC configured to Nyqusit zone 1 and zone 2.

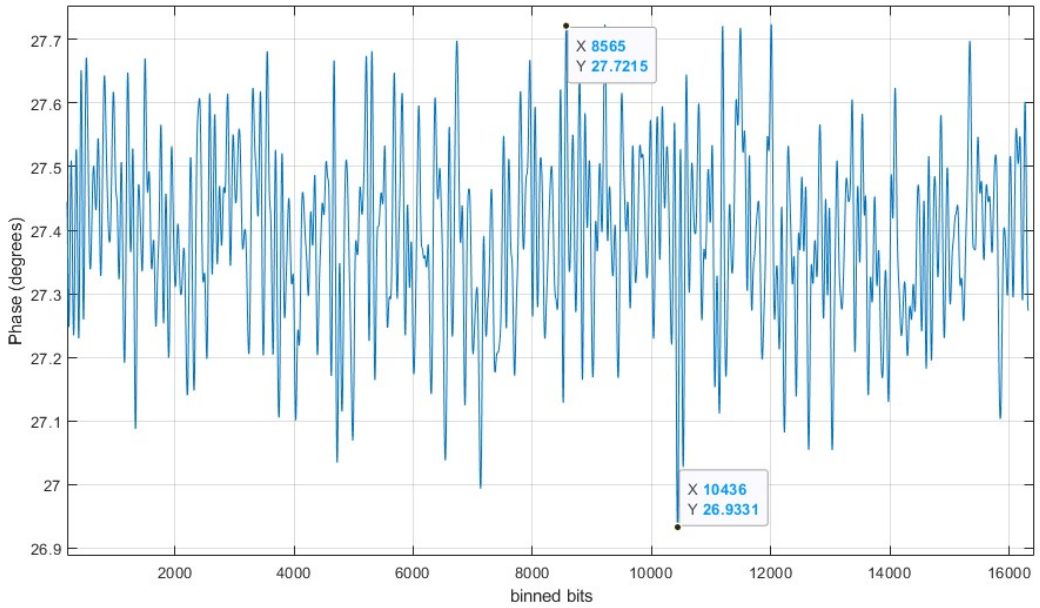


Figure 8: Magnitude fluctuation when the DAC generate the signal is set to the first Nyquist zone.

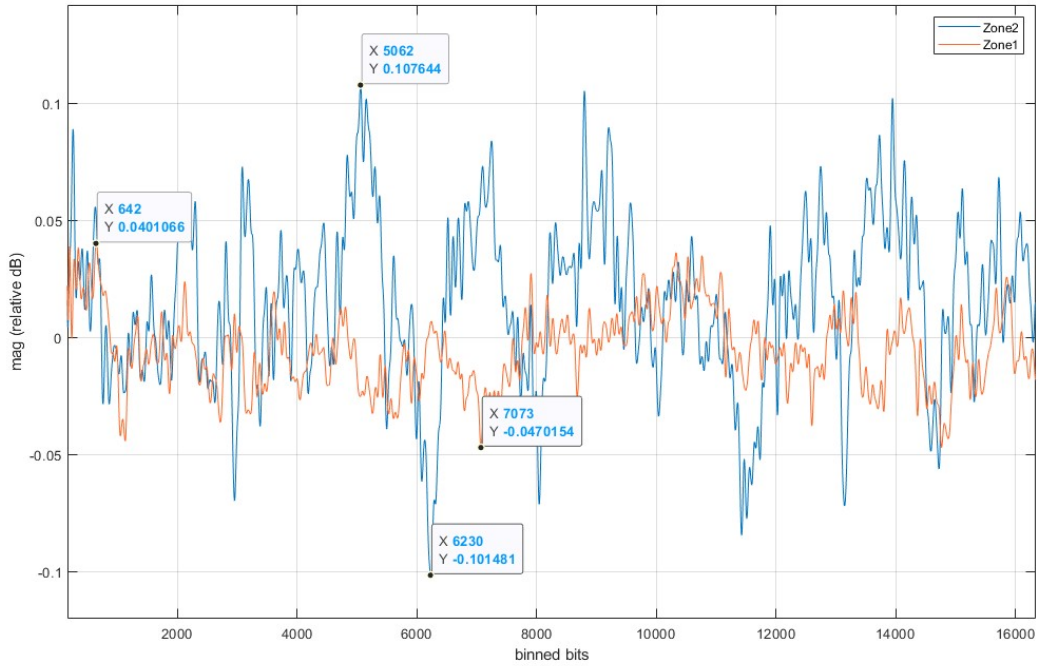


Figure 9: The comparison between the magnitude fluctuation with DAC configured to Nyqusit zone 1 and zone 2.

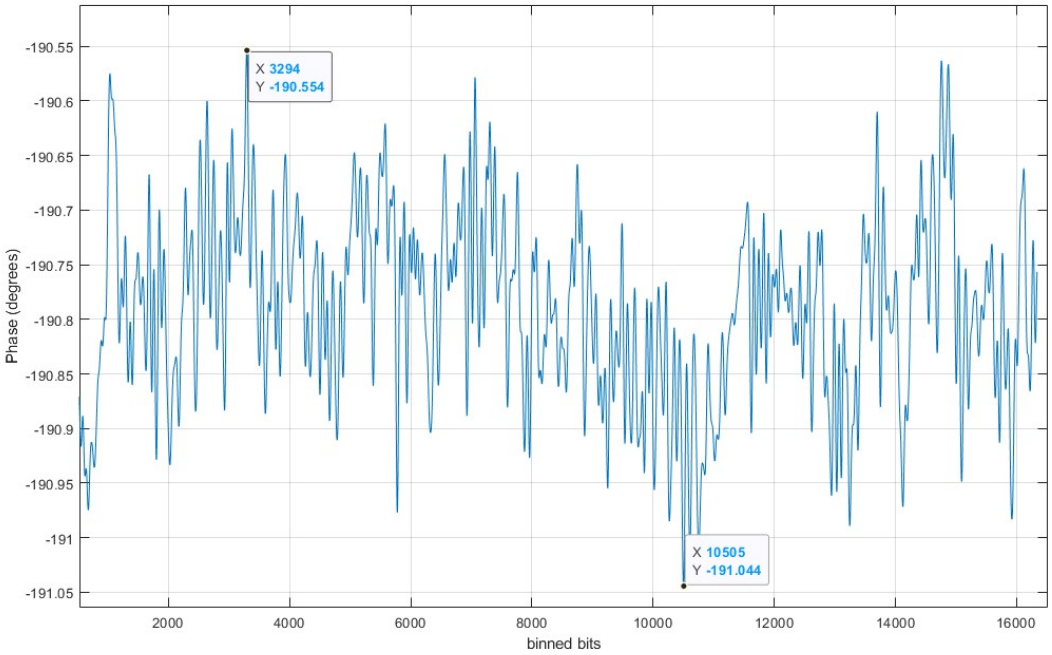


Figure 10: Phase fluctuation when the DAC generate the signal is set to the first Nyquist zone.

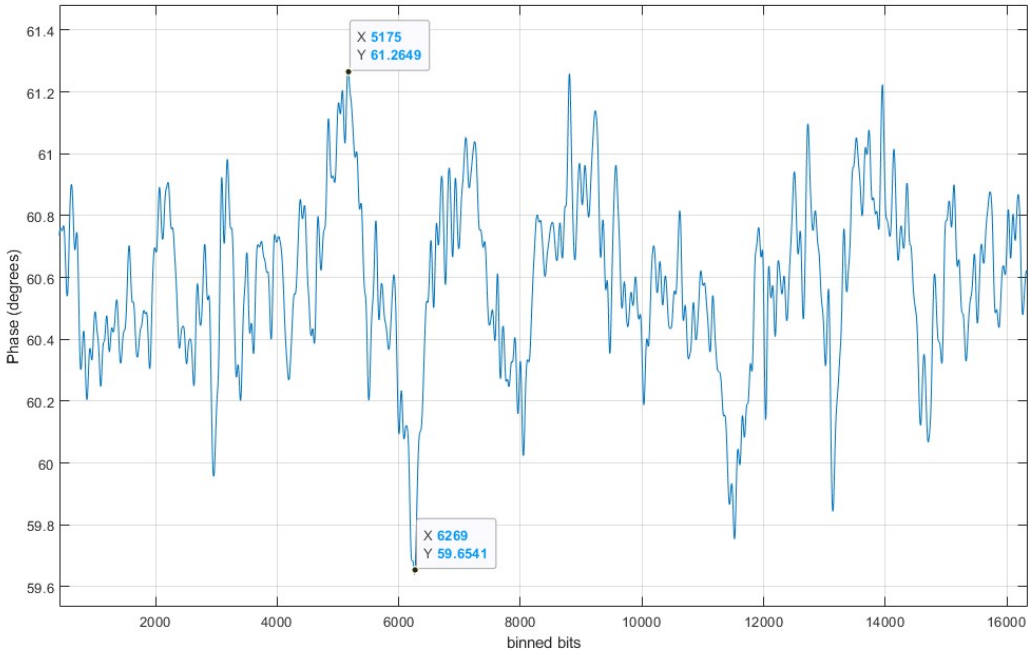


Figure 11: Phase fluctuation when the DAC generate the signal is set to the second Nyquist zone.

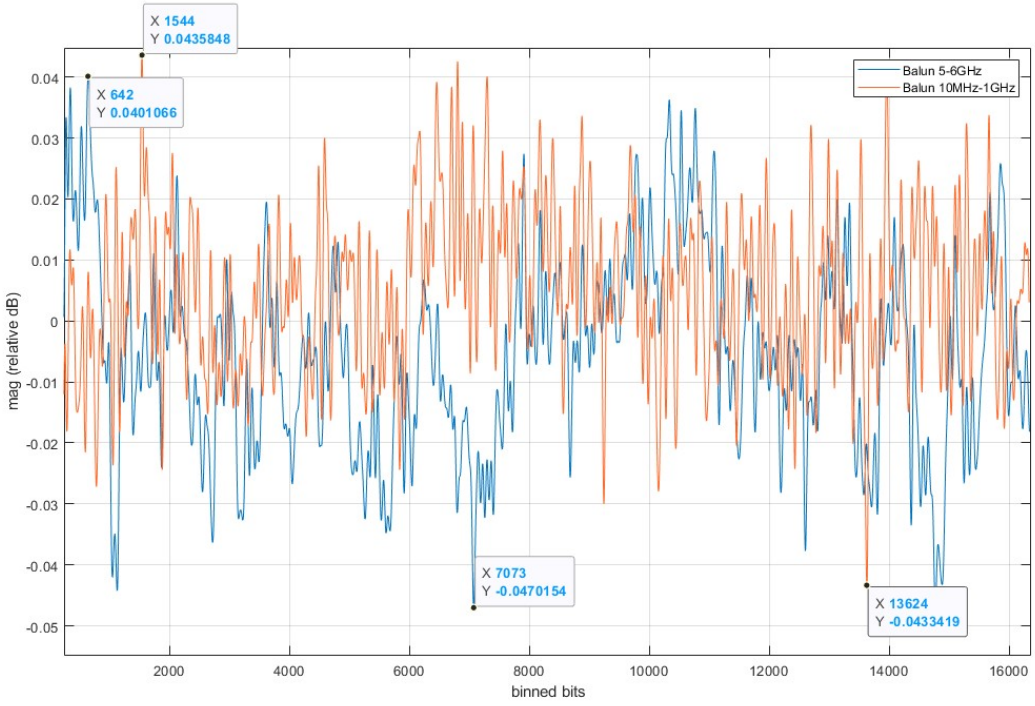


Figure 12: The comparison between the magnitude fluctuation with different baluns on ADC side.