ACCEL LLRF RFdc Test

Project: DARPA ACCEL

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Date: Feb 2023
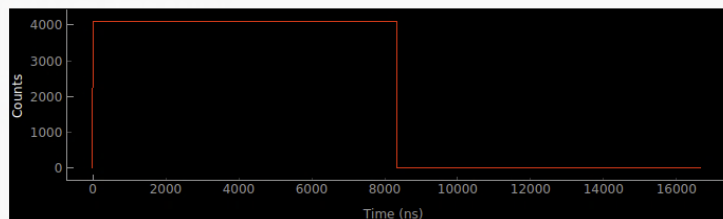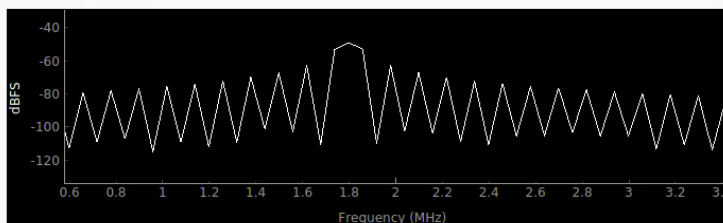
Loopback Test

DAC0 Time Domain: white=I, red=Q

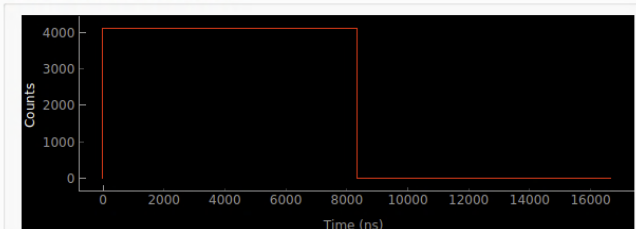ADC2 Time Domain: white=I, red=Q
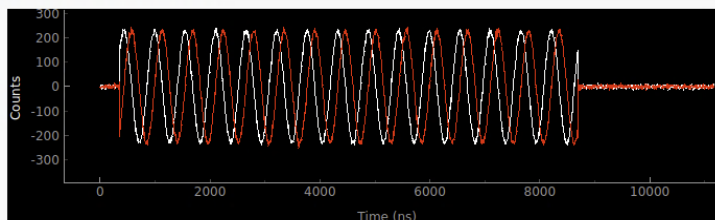
ADC2 Frequency Domain

- Test configuration
  - DC pulse load to DAC datapath
  - Interpolated x24
  - Upmixed by 5712 MHz
  - DAC running at 5.89824 GSPS
  - DAC signal looped back to ADC via BFP and baluns
  - ADC sampling at 2.4576 GSPS
  - Downmixed at 796.8 MHz and decimated x4
- Results
  - DC signal expected from the decimated IQ
  - 1.8 MHz signals on IQ components
  - Check the NCO settings – the downmix frequency mis-configured to 798.6 MHz
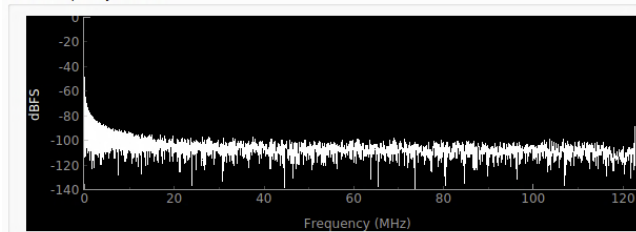
NCO Frequency Corrected

DAC0 Time Domain: white=I, red=Q

ADC0 Time Domain: white=I, red=Q
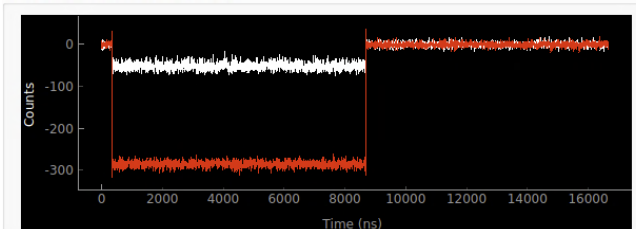
ADC0 Frequency Domain

- Test configuration
  - Same as last slide
- Code modification
  - New git branch created
  - RFdc IP updated
  - 'CopyIpCores' in Tcl Console and .xci file for the IP updated
  - 'git add .', 'git commit –m "" ' and 'git push'
  - 'make' the new .bit and 'scp' to RFSoC
- Results
  - DC values as expected for IQ components
  - Spectra centred at DC

Git branch and scp Jira ticket

Created a working branch at:

https://github.com/slaclab/darpa-accel-llrf-phase-1p5/tree/accel_llrf_cl

Jira ticket for the glitch of scp .bit to the RFSoC board

https://jira.slac.stanford.edu/browse/ESRFOC-47

Thank you!