XILINX
ALL PROGRAMMABLE™

KCU105 GTH IBERT Design Creation

October 2017

XTP346

Revision History

Date	Version	Description
10/09/17	12.0	Updated for 2017.3.
06/20/17	11.0	Updated for 2017.2.
04/19/17	10.0	Updated for 2017.1.
12/19/16	9.0	Updated for 2016.4.
10/13/16	8.0	Updated for 2016.3.
06/08/16	7.0	Updated for 2016.2.
04/13/16	6.0	Updated for 2016.1
11/24/15	5.0	Updated for 2015.4.
10/06/15	4.0	Updated for 2015.3.
06/30/15	3.0	Updated for 2015.2.
04/30/15	2.0	Updated for 2015.1.
03/06/15	1.0	Initial version. Added AR63771.

KCU105 IBERT Overview

- Xilinx KCU105 Board
- KCU105 Software Install and Board Setup
- Setup for the KCU105 IBERT Design
- IBERT Testing
  - FMC HPC (Bank 227 & 228)
  - FMC LPC (Bank 226)
  - SFP (Bank 226)
  - PCIe (Bank 224 & 225)
- Create IBERT Design for All Banks
  - Testing All Banks with Optional User Provided Hardware
- References

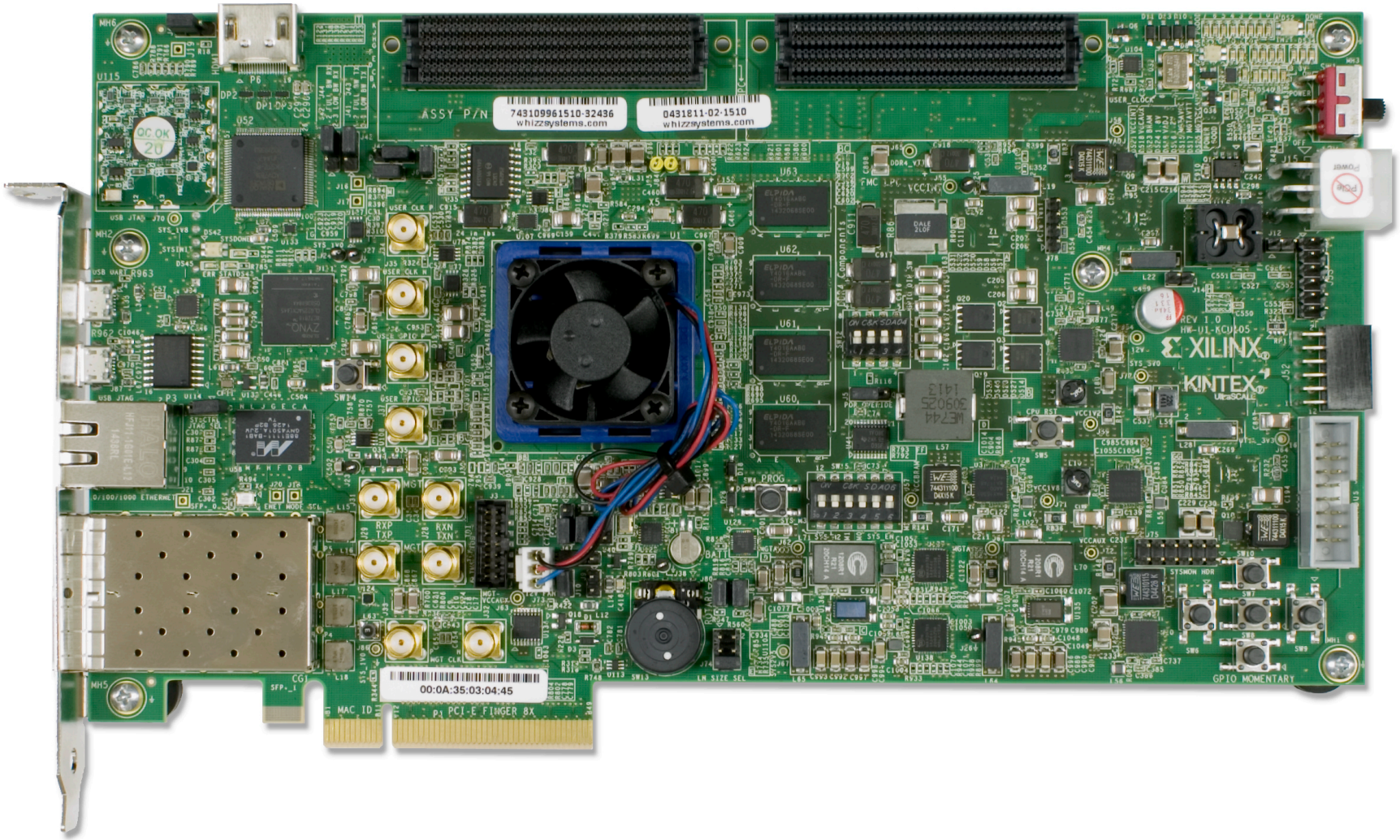
Note: This presentation applies to the KCU105

KCU105 IBERT Overview

- Description
  - The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the UltraScale Kintex GTH transceivers. A graphical user interface is provided through the Vivado Hardware Manager.
- Reference Design IP
  - LogiCORE UltraScale IBERT GTH Example Designs

Note: Presentation applies to the KCU105

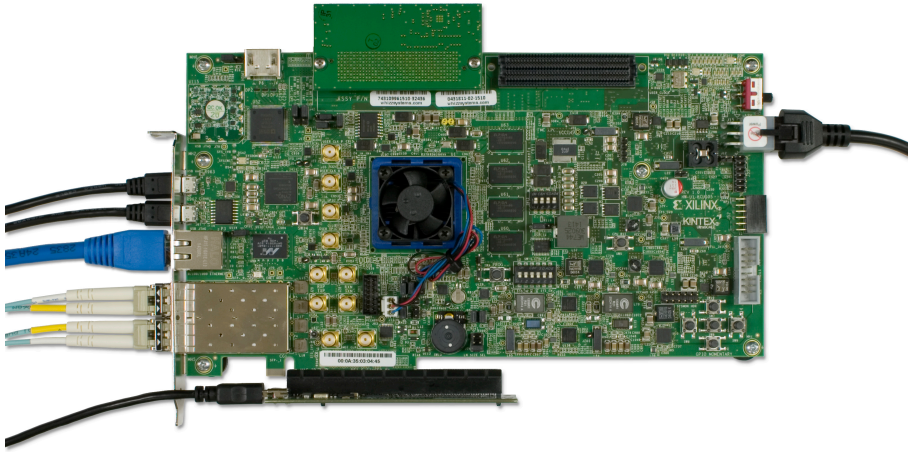
Xilinx KCU105 Board



Note: Presentation applies to the KCU105

KCU105 Software Install and Board Setup

- Refer to XTP352 – KCU105 Software Install and Board Setup for details on:
  - Software Requirements
  - KCU105 Board Setup
  - Clock Setup
  - Optional Hardware Setup

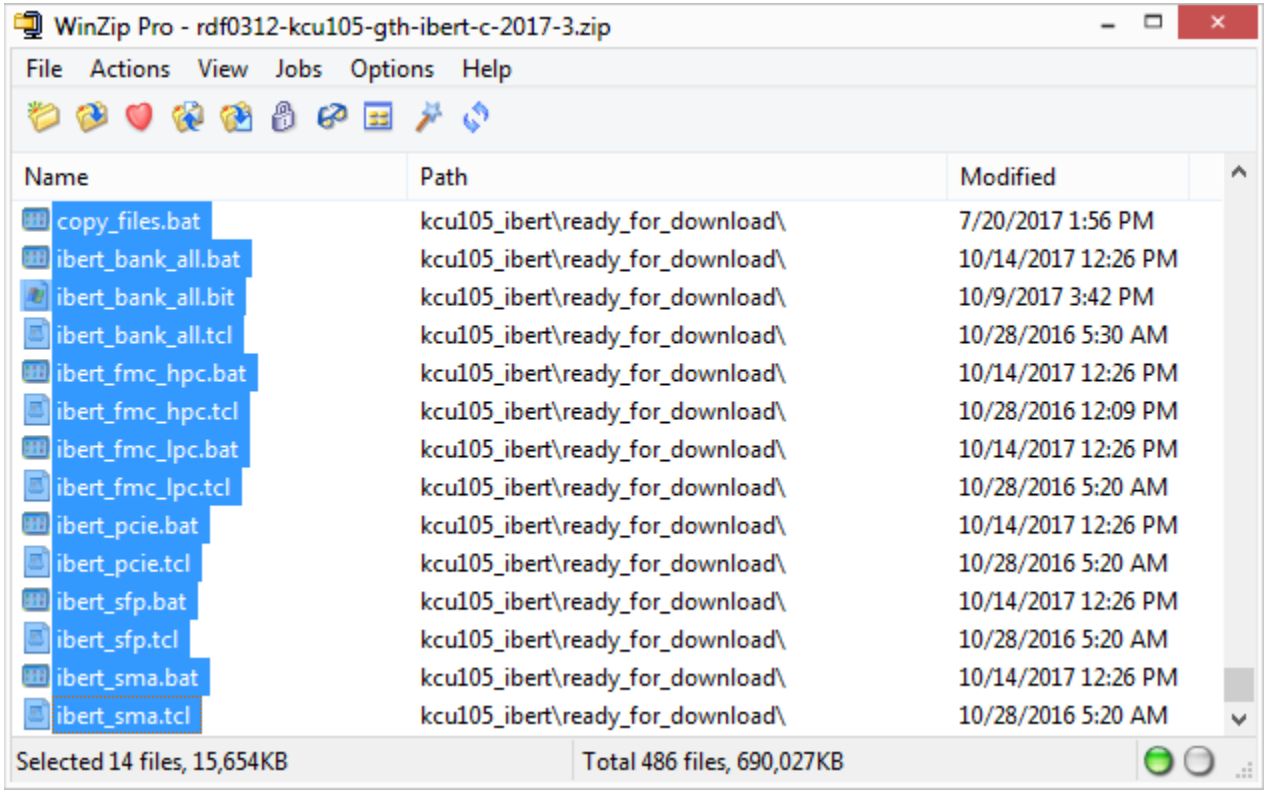


Note: The Clock Setup is required for this tutorial

Setup for the KCU105 IBERT Design

Setup for the KCU105 IBERT Design

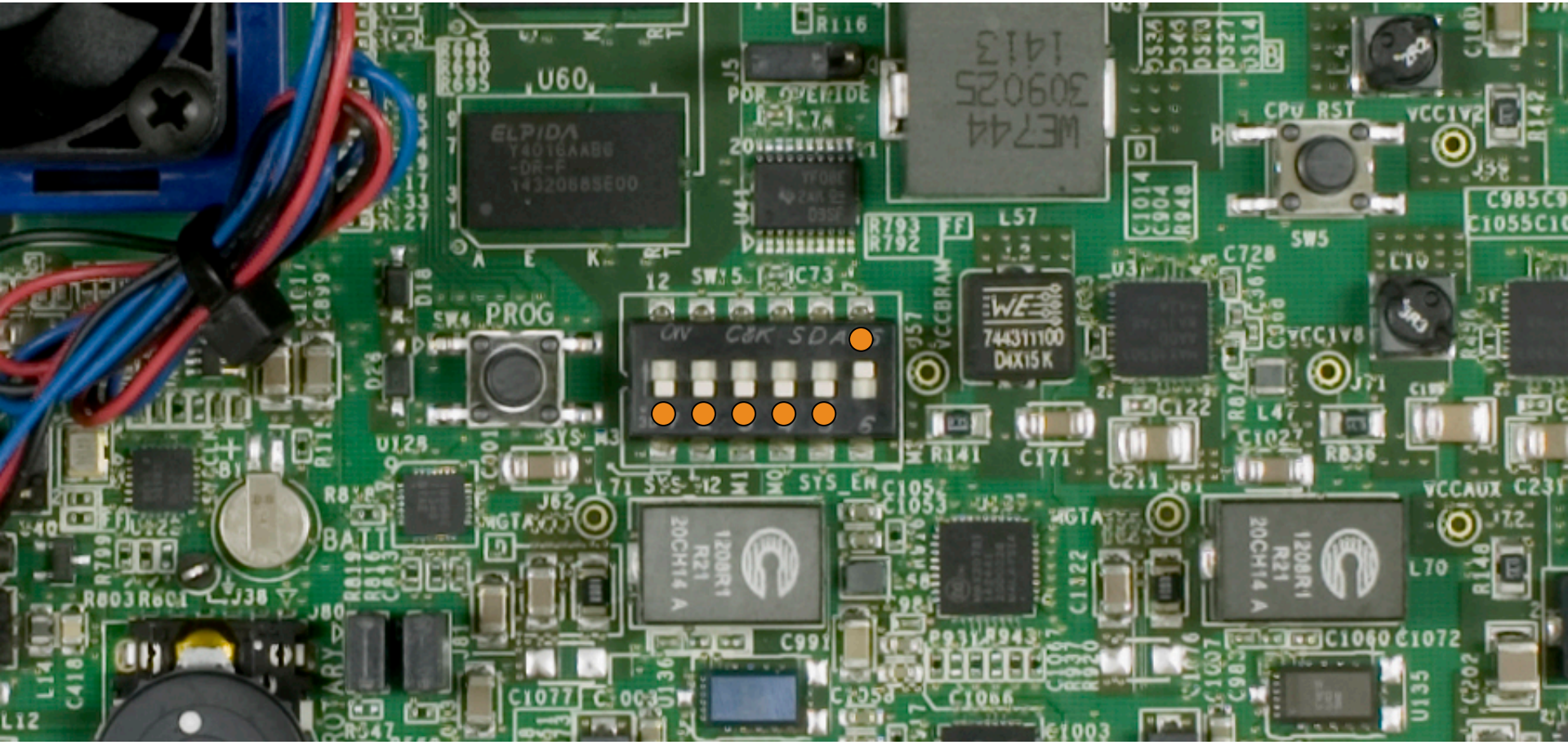
- Open the RDF0312 - KCU105 GTH IBERT Design Files (2017.3 C) ZIP file, and extract these files to your C:\ drive:
  - kcu105_ibert\ready_for_download*



Note: Presentation applies to the KCU105

Setup for the KCU105 IBERT Design

- Set SW15 to 000001 (1 = on, Position 1 → Position 6)
  - This enables JTAG configuration

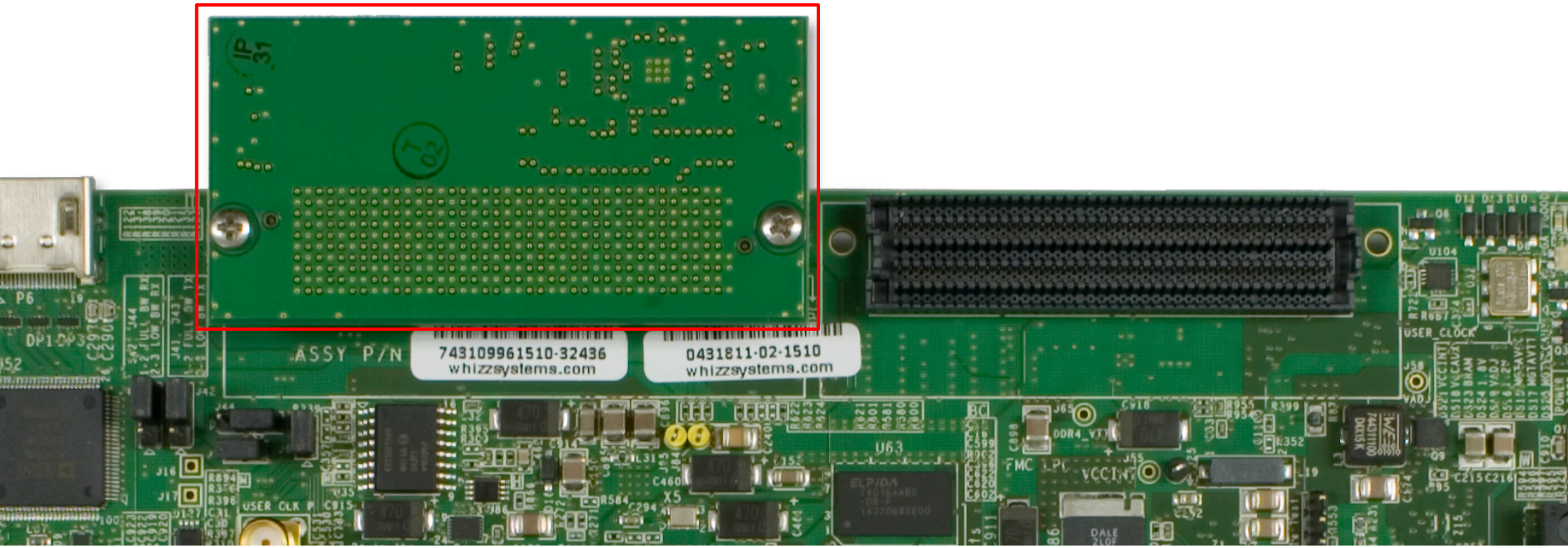


Note: Presentation applies to the KCU105

Testing FMC HPC IBERT

Testing FMC HPC IBERT

- As noted in the Setup Guide, XTP352, attach the FMC XM107 board to the FMC HPC connector

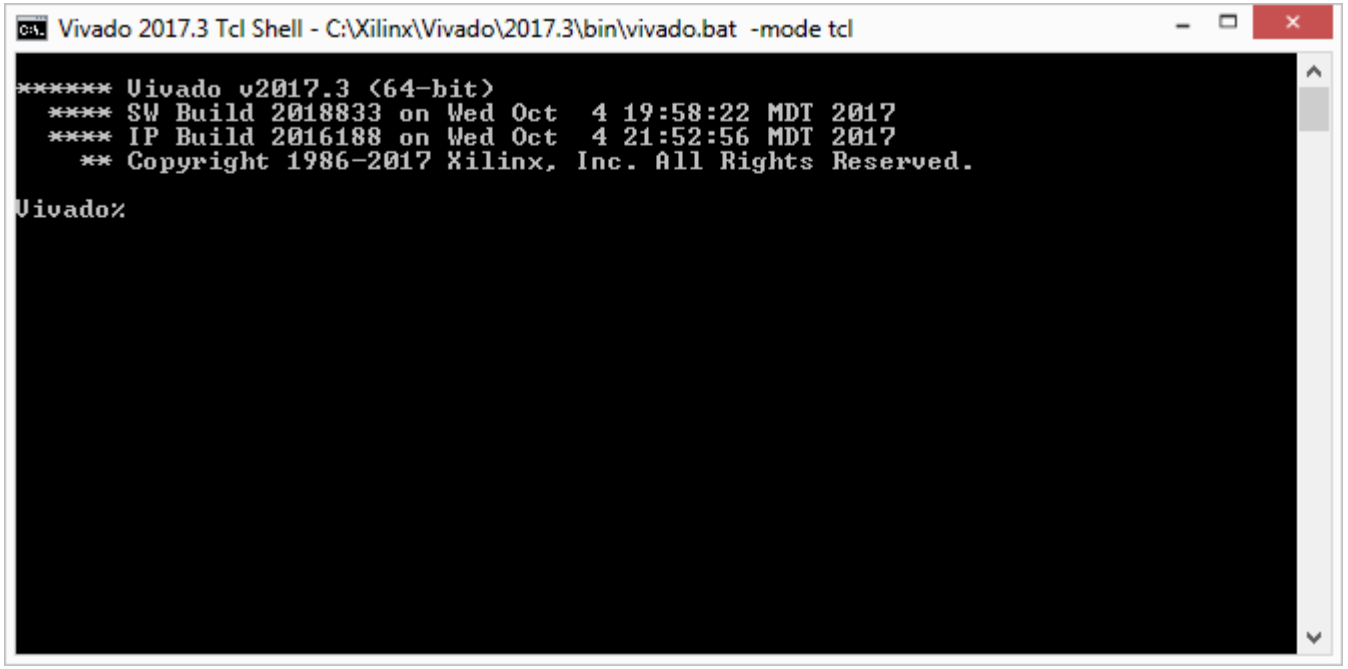


Note: Presentation applies to the KCU105

Testing FMC HPC IBERT

- Open a Vivado Tcl Shell:

  Start → All Programs → Xilinx Design Tools → Vivado 2017.3 → Vivado 2017.3 Tcl Shell



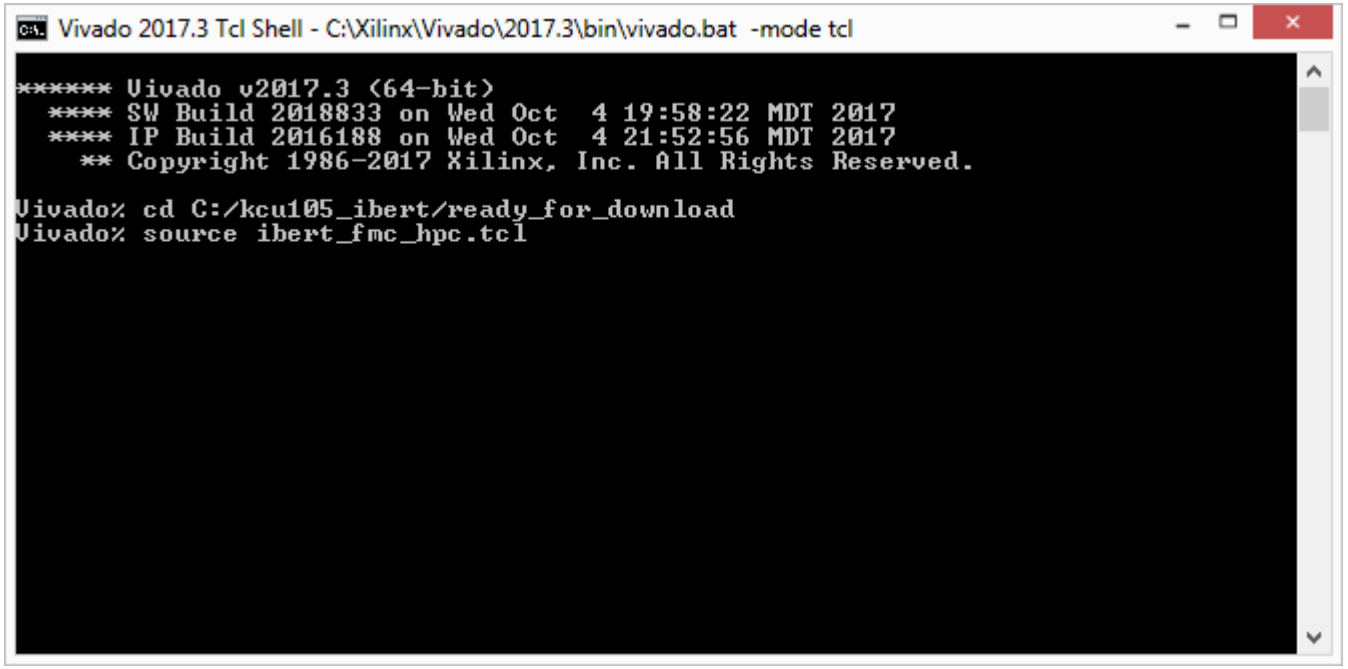
Note: Presentation applies to the KCU105

Testing FMC HPC IBERT

- In a Vivado Tcl Shell type:

  cd C:/kcu105_ibert/ready_for_download

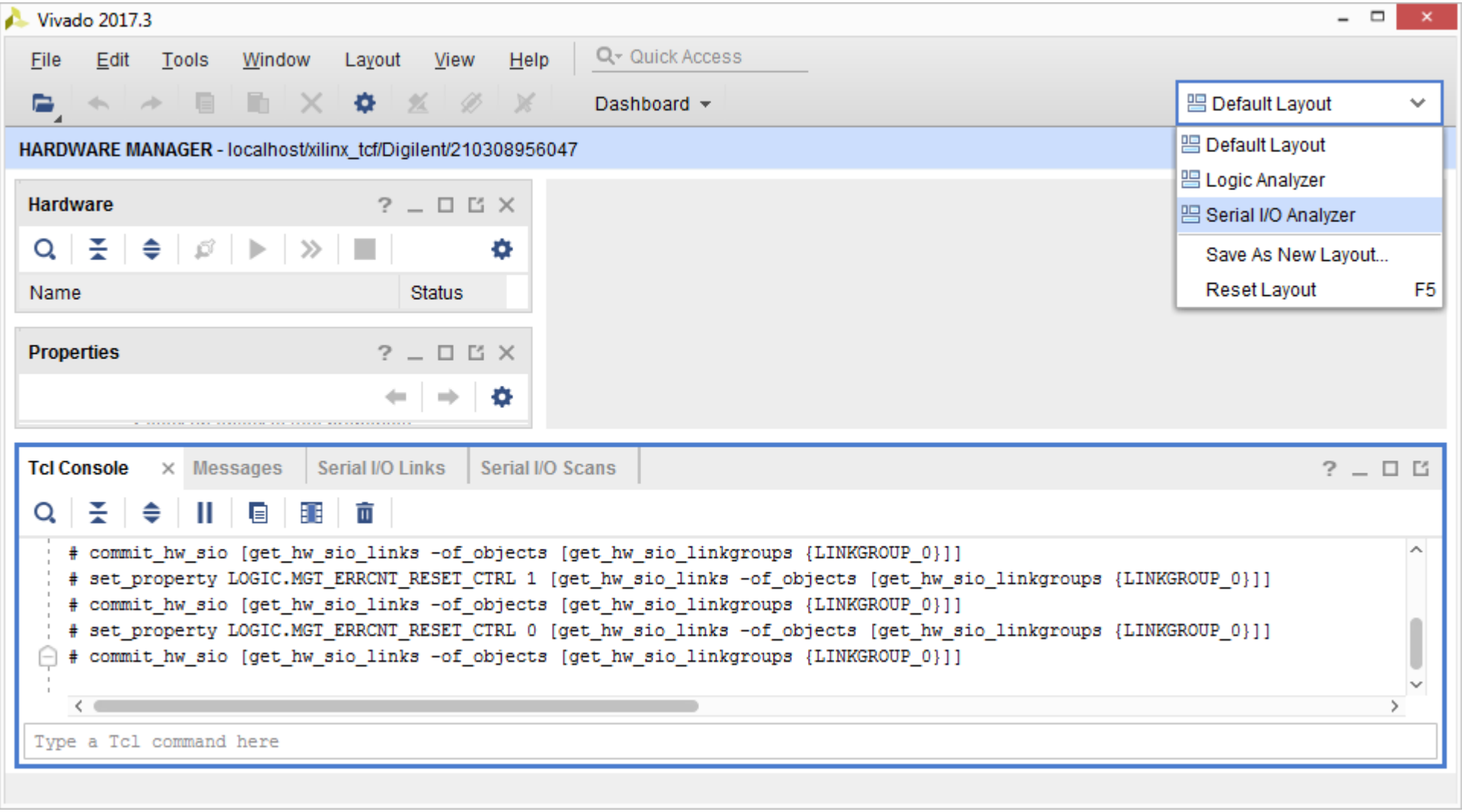
  source ibert_fmc_hpc.tcl



Note: Presentation applies to the KCU105

Testing FMC HPC IBERT

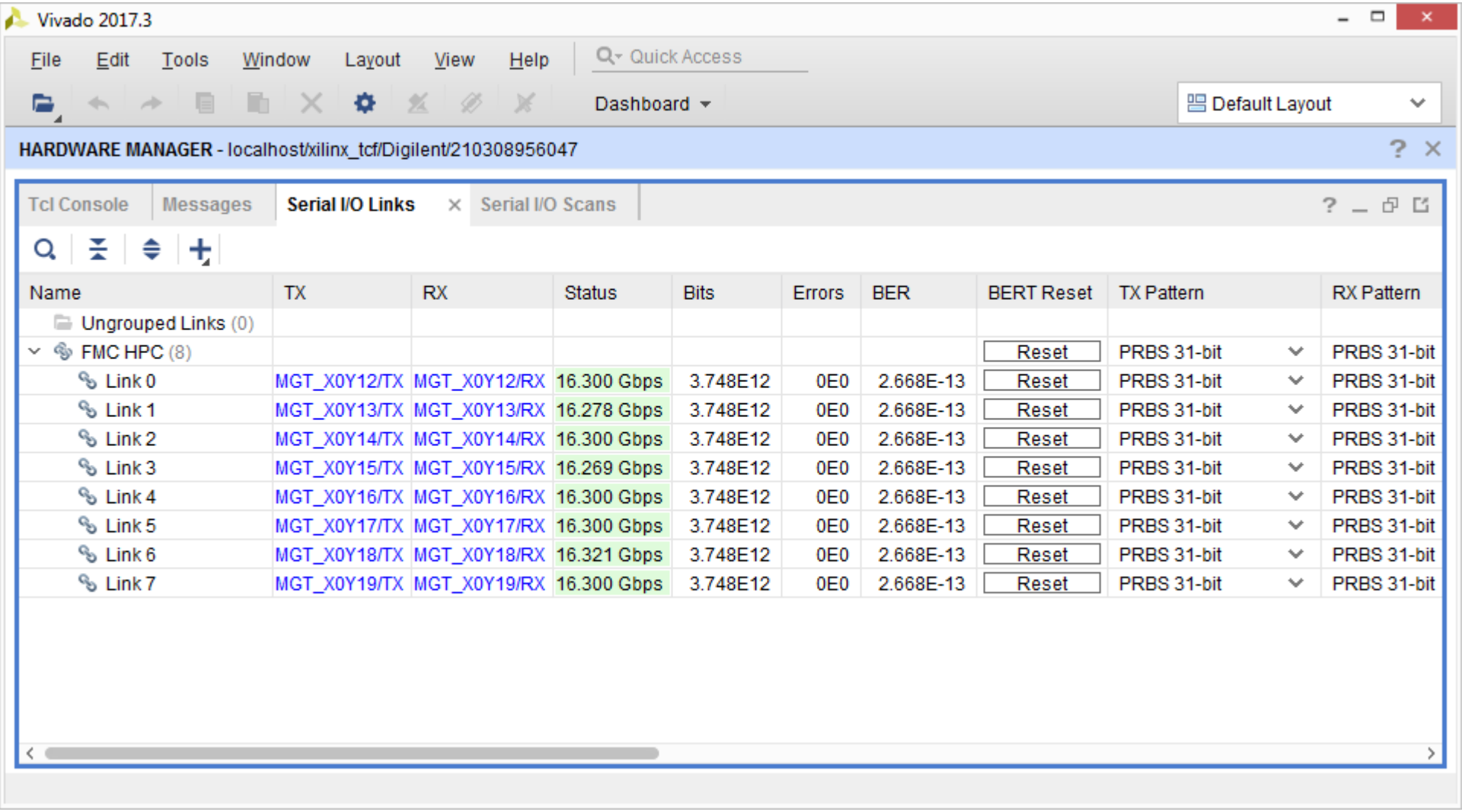
- If needed, set Vivado GUI layout to Serial I/O Analyzer



Note: Presentation applies to the KCU105

Testing FMC HPC IBERT

- FMC HPC line rate is 16.3 Gbps
- Close Vivado GUI after finished viewing



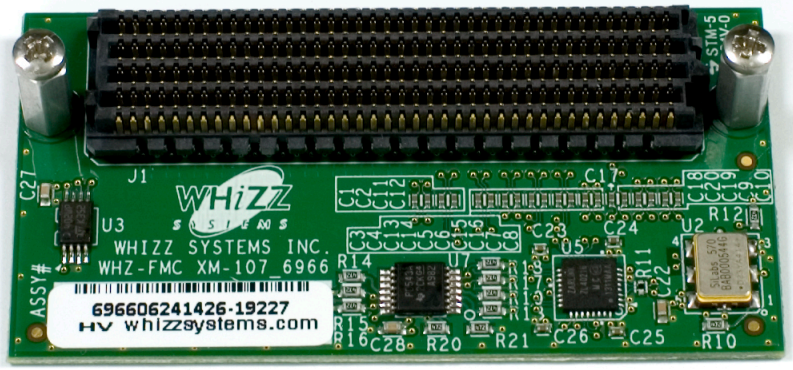
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
FMC HPC (8)							Reset	PRBS 31-bit	PRBS 31-bit
Link 0	MGT_X0Y12/TX	MGT_X0Y12/RX	16.300 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 1	MGT_X0Y13/TX	MGT_X0Y13/RX	16.278 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 2	MGT_X0Y14/TX	MGT_X0Y14/RX	16.300 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 3	MGT_X0Y15/TX	MGT_X0Y15/RX	16.269 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 4	MGT_X0Y16/TX	MGT_X0Y16/RX	16.300 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 5	MGT_X0Y17/TX	MGT_X0Y17/RX	16.300 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 6	MGT_X0Y18/TX	MGT_X0Y18/RX	16.321 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 7	MGT_X0Y19/TX	MGT_X0Y19/RX	16.300 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit

Note: User Si570 should be set to 163 MHz as per XTP352

Testing FMC LPC IBERT

Testing FMC LPC IBERT

- Move the FMC XM107 board to the FMC LPC connector



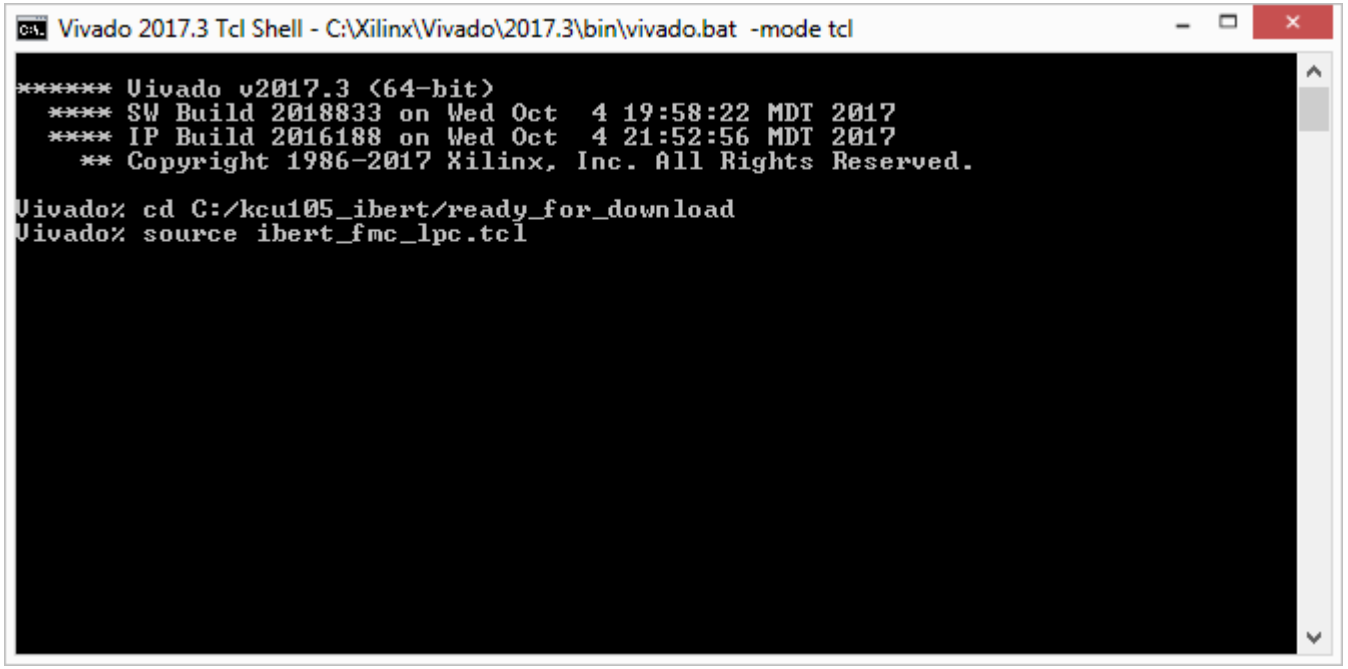
Note: Presentation applies to the KCU105

Testing FMC LPC IBERT

- In a Vivado Tcl Shell type:

  cd C:/kcu105_ibert/ready_for_download

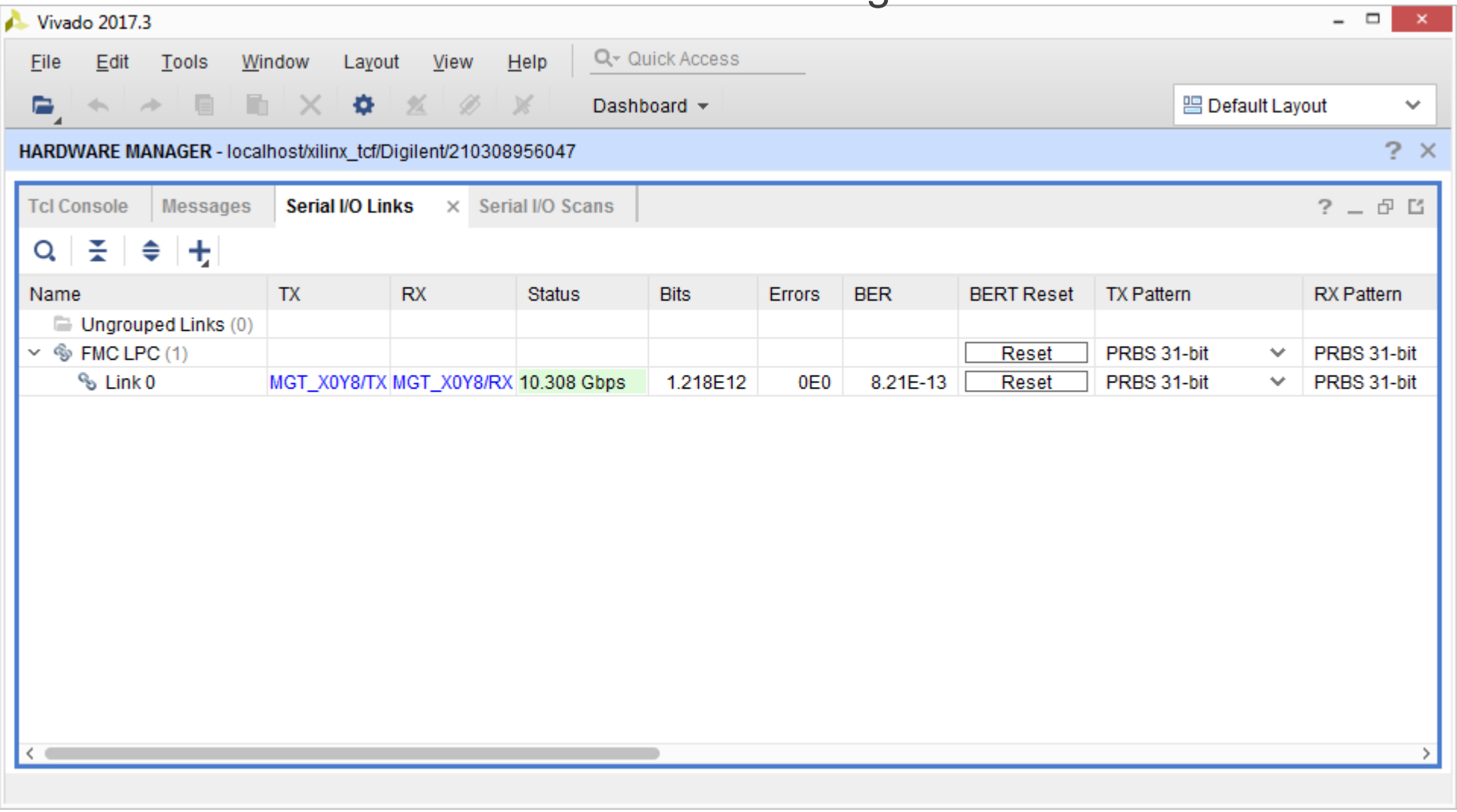
  source ibert_fmc_lpc.tcl



Note: Presentation applies to the KCU105

Testing FMC LPC IBERT

- FMC LPC line rate is 10.3125 Gbps
- Close Vivado GUI after finished viewing

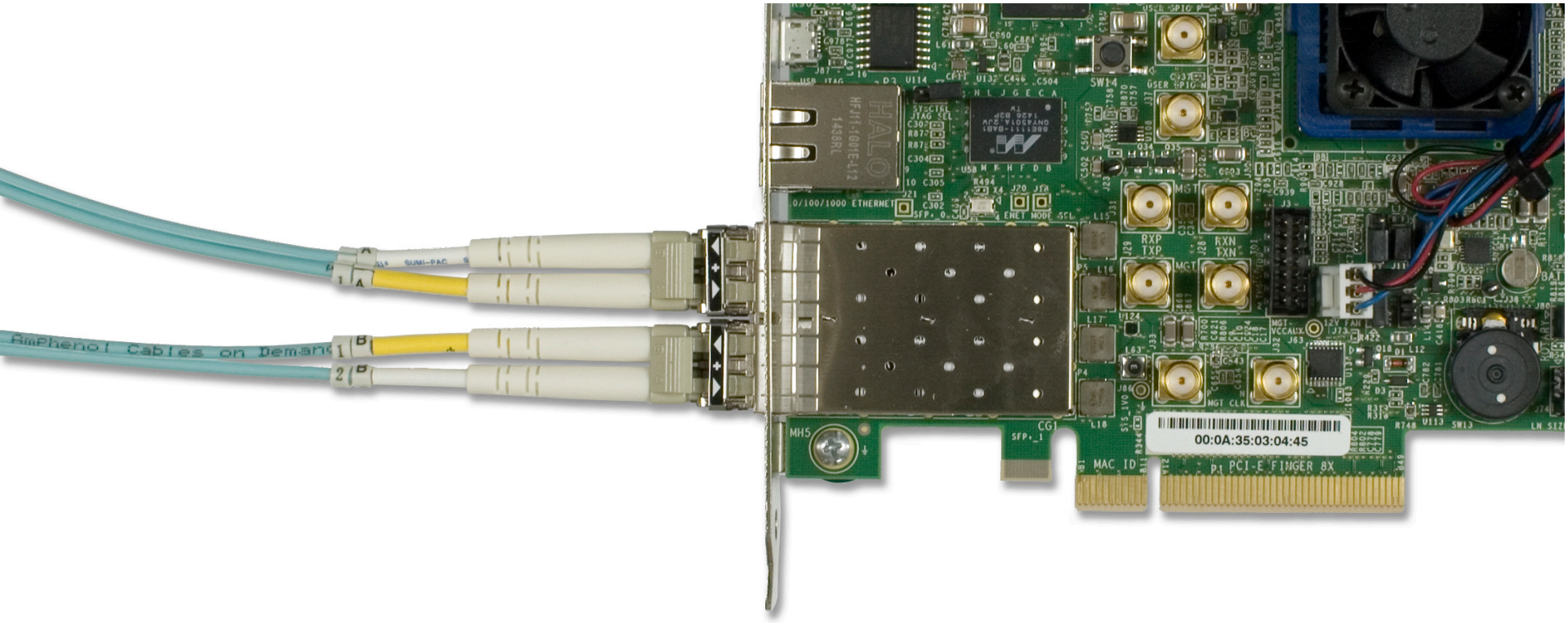


Note: Presentation applies to the KCU105

Testing SFP IBERT

Testing SFP IBERT

- As noted in the Setup Guide, XTP352, The Optical modules and Fiber optic cable should be attached for this test

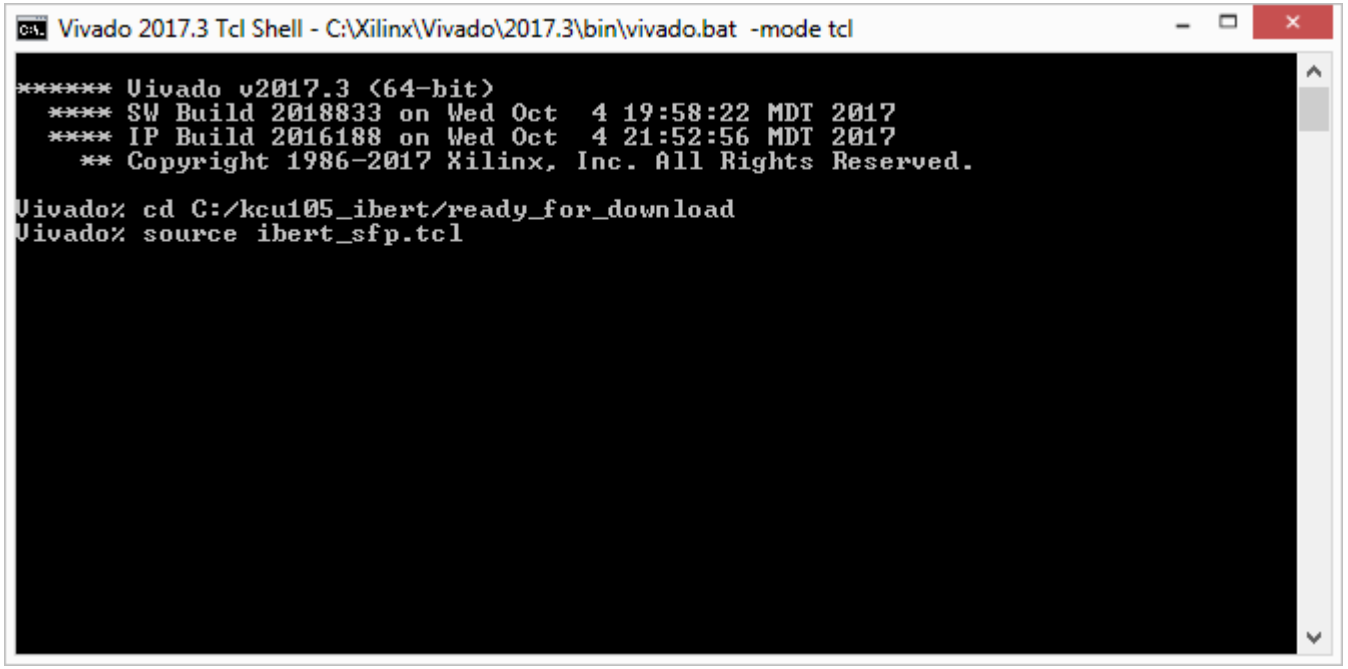


Testing SFP IBERT

- In the Vivado Tcl Shell type:

  cd C:/kcu105_ibert/ready_for_download

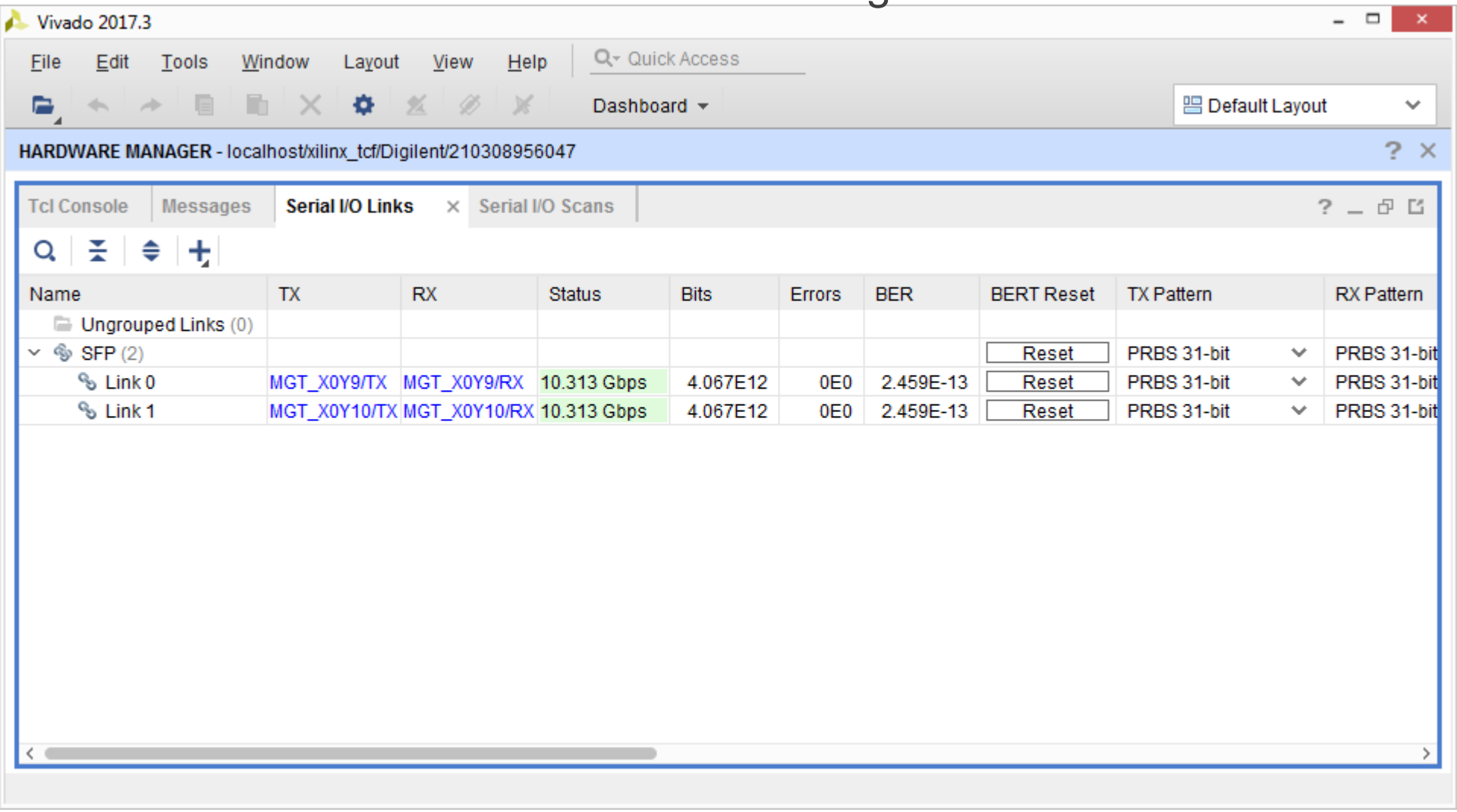
  source ibert_sfp.tcl



Note: Presentation applies to the KCU105

Testing SFP IBERT

- SFP line rate is 10.3125 Gbps
- Close Vivado GUI after finished viewing



Note: Presentation applies to the KCU105

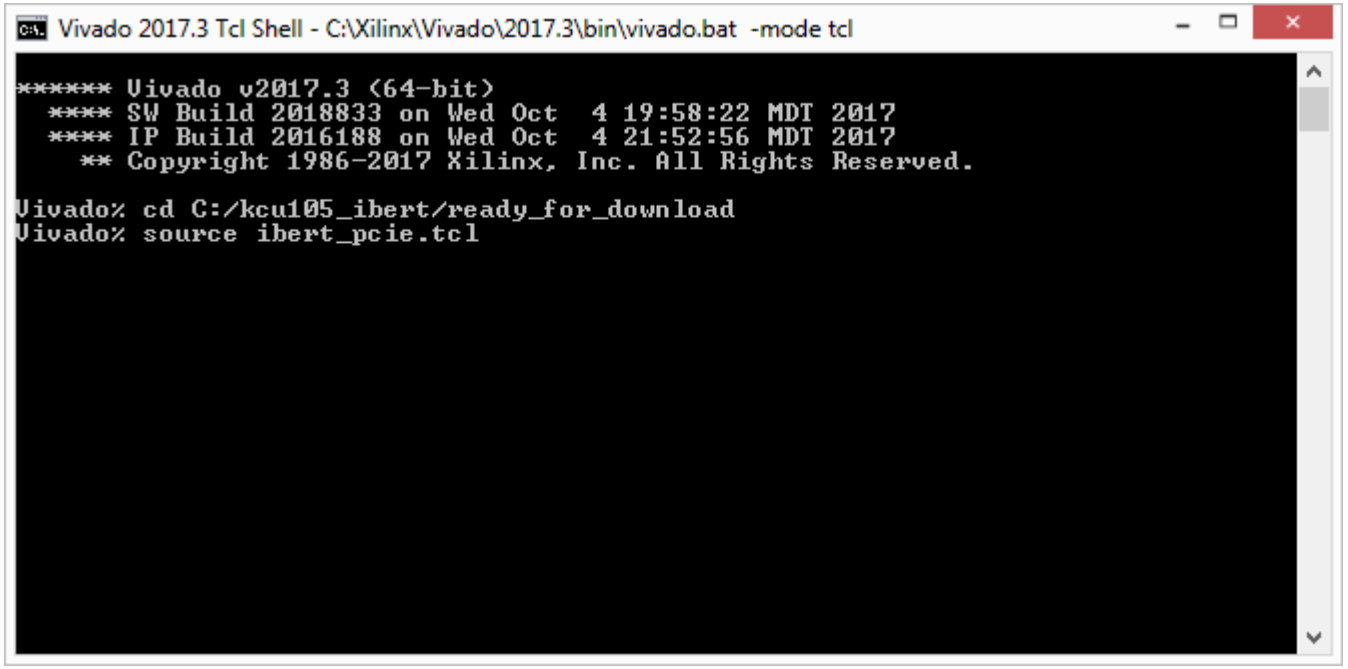
Testing PCIe IBERT

Testing PCIe IBERT

- In a Vivado Tcl Shell type:

  cd C:/kcu105_ibert/ready_for_download

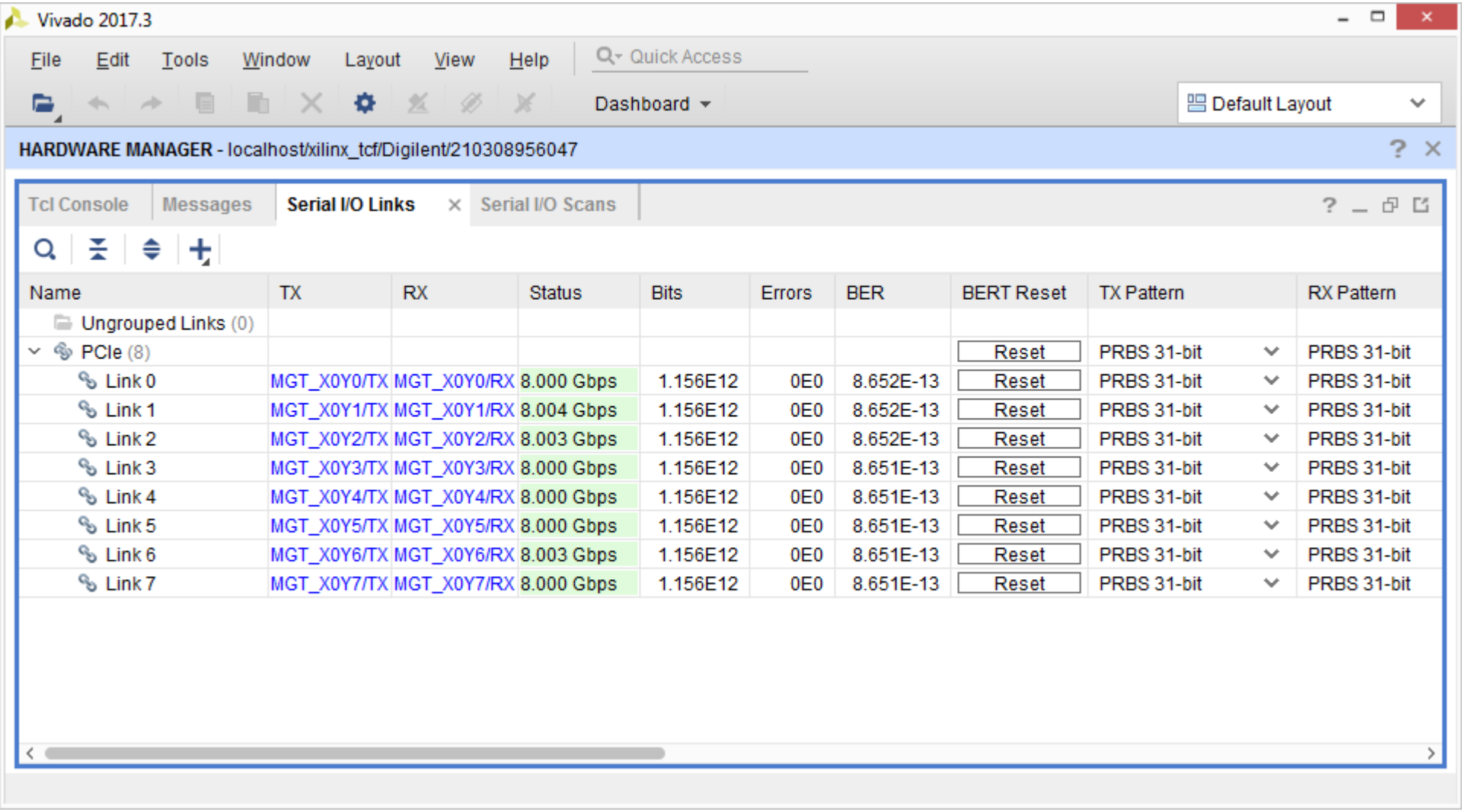
  source ibert_pcie.tcl



Note: Presentation applies to the KCU105

Testing PCIe IBERT

- PCIe line rate is 8 Gbps
- Close Vivado GUI after finished viewing



Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
PCIe (8)							Reset	PRBS 31-bit	PRBS 31-bit
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	8.000 Gbps	1.156E12	0E0	8.652E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	8.004 Gbps	1.156E12	0E0	8.652E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	8.003 Gbps	1.156E12	0E0	8.652E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	1.156E12	0E0	8.651E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	8.000 Gbps	1.156E12	0E0	8.651E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	8.000 Gbps	1.156E12	0E0	8.651E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	8.003 Gbps	1.156E12	0E0	8.651E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	8.000 Gbps	1.156E12	0E0	8.651E-13	Reset	PRBS 31-bit	PRBS 31-bit

Note: Presentation applies to the KCU105

Create IBERT Design for All Banks

Create IBERT Design for All Banks

- Open Vivado

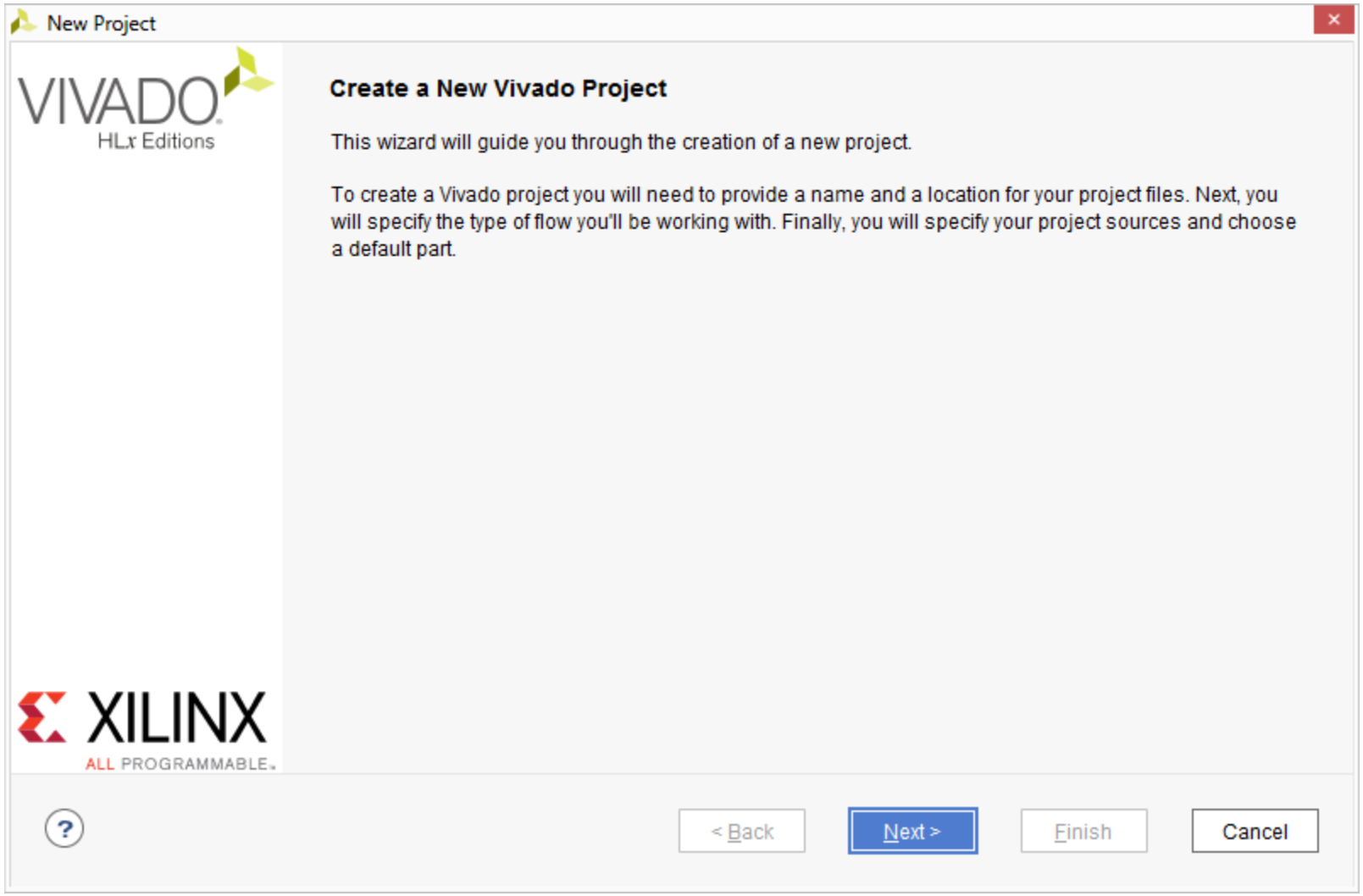
  Start → All Programs → Xilinx Design Tools → Vivado 2017.3 → Vivado

- Select **Create Project**

Note: Presentation applies to the KCU105

Create IBERT Design for All Banks

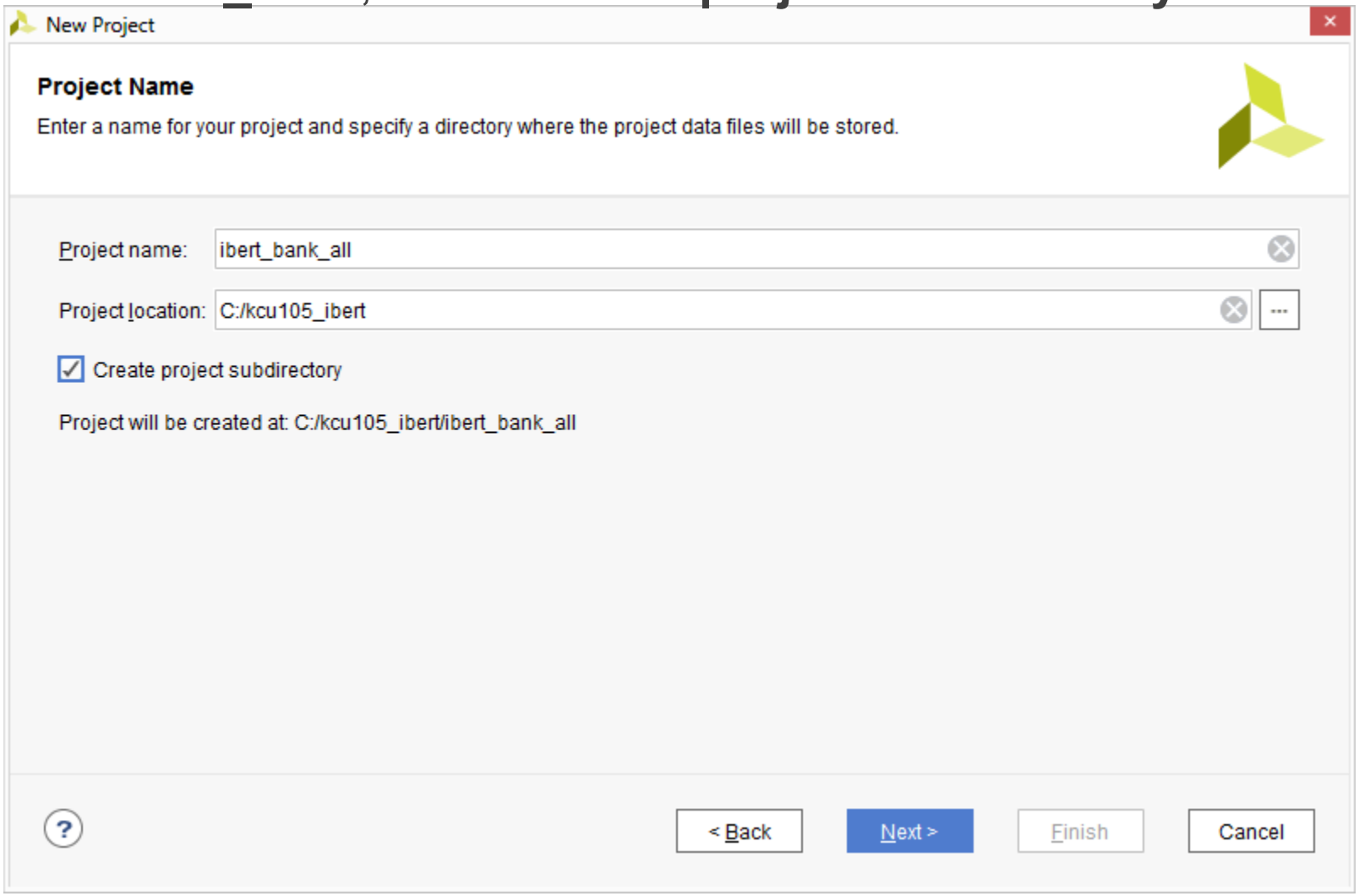
- Click **Next**



Note: Presentation applies to the KCU105

Create IBERT Design for All Banks

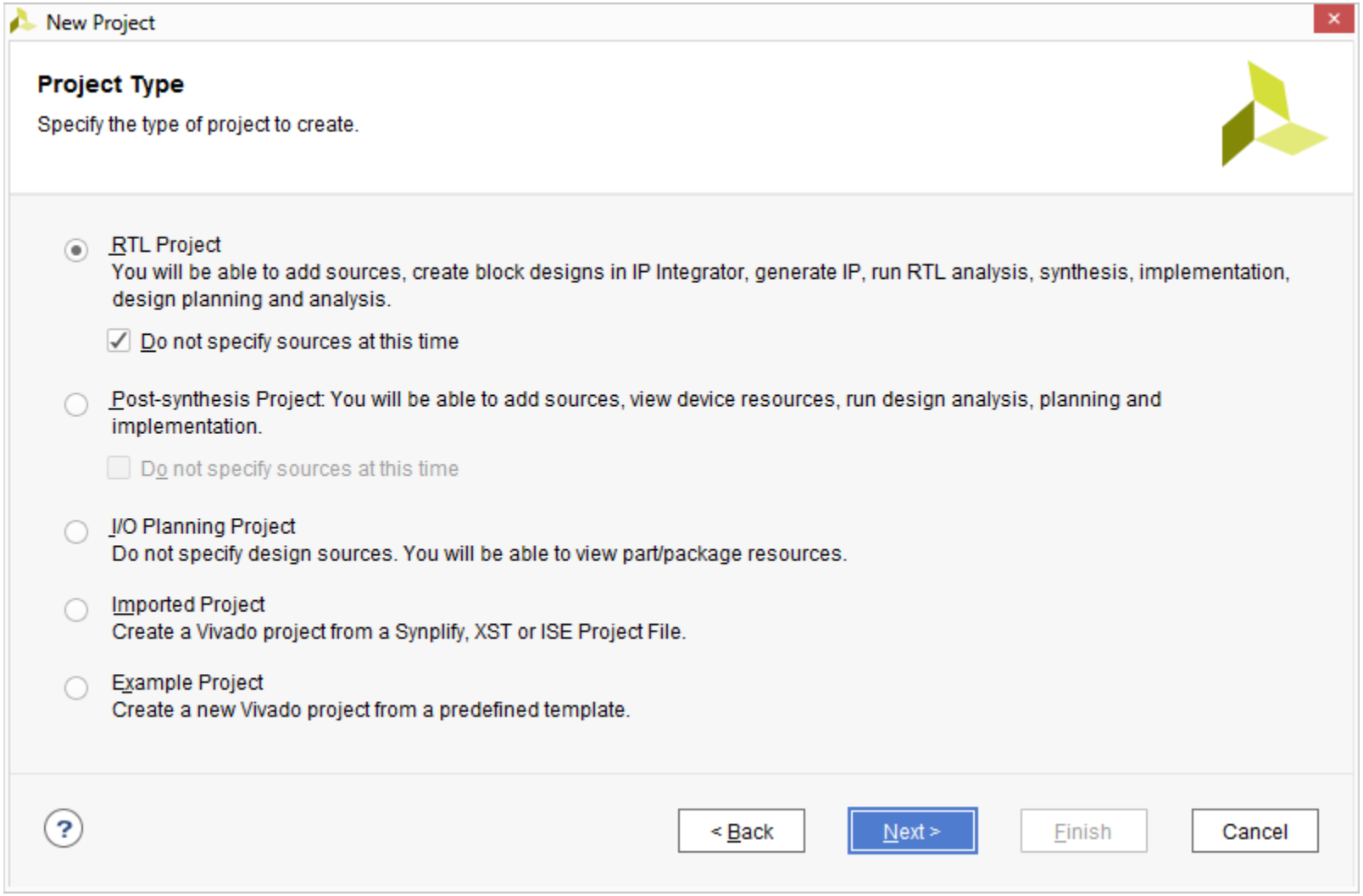
- Set the Project name and location to **ibert_bank_all** and **C:/kcu105_ibert**; check **Create project subdirectory**



Note: Vivado generally requires forward slashes in paths

Create IBERT Design for All Banks

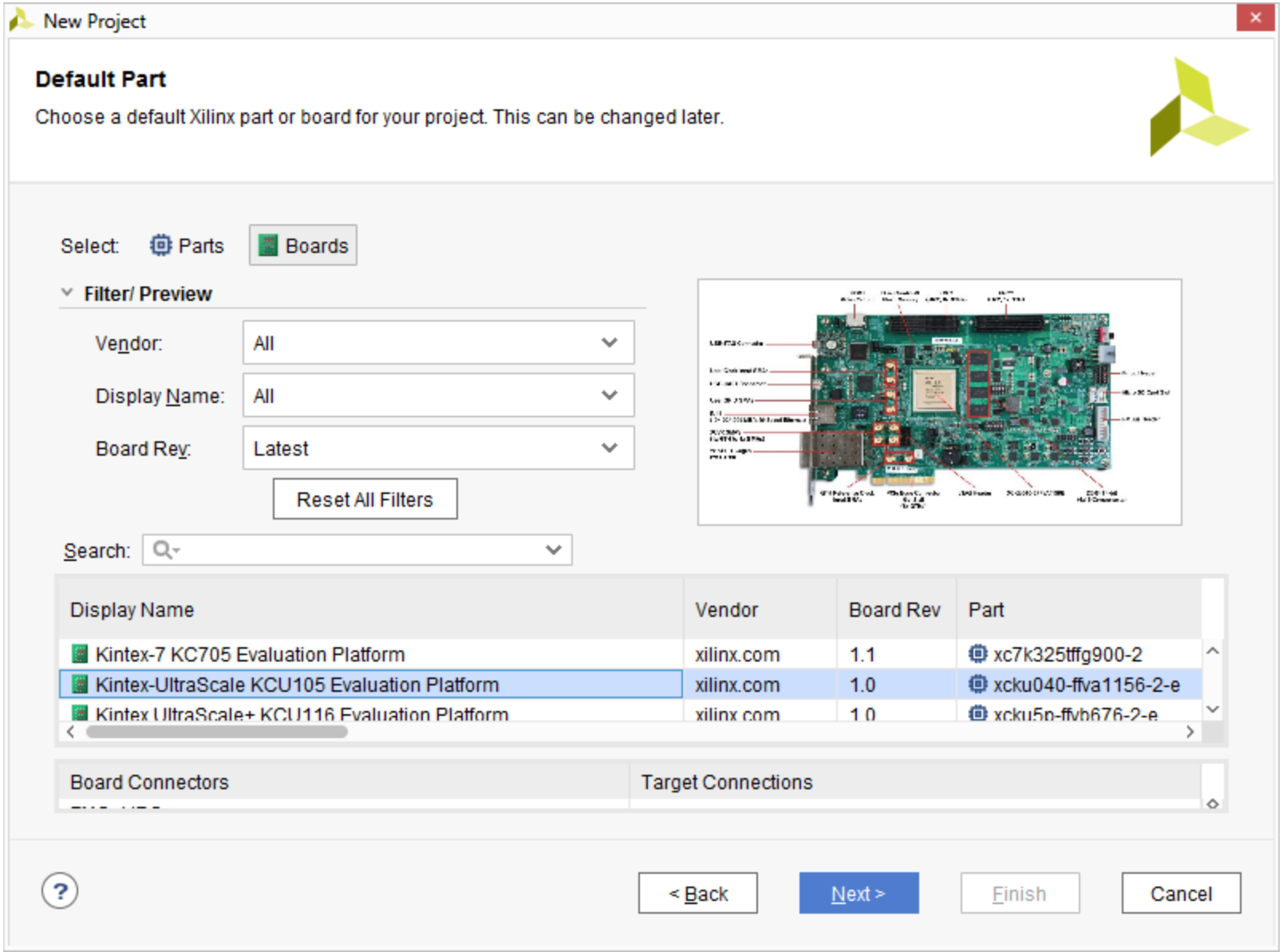
- Select **RTL Project**
  - Select **Do not specify sources at this time**



Note: Presentation applies to the KCU105

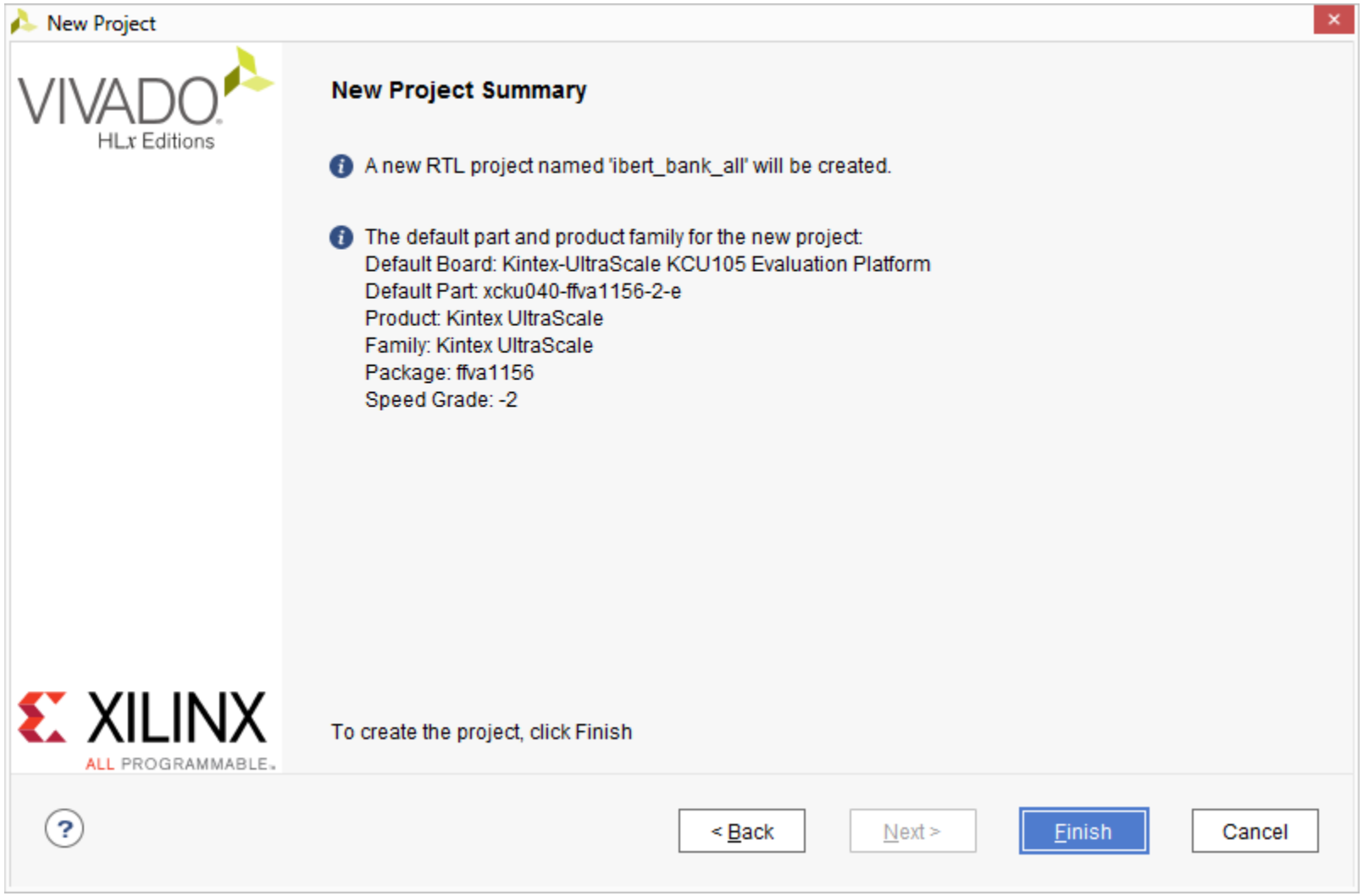
Create IBERT Design for All Banks

- Under Boards, select the **KCU105 Evaluation Platform**



Create IBERT Design for All Banks

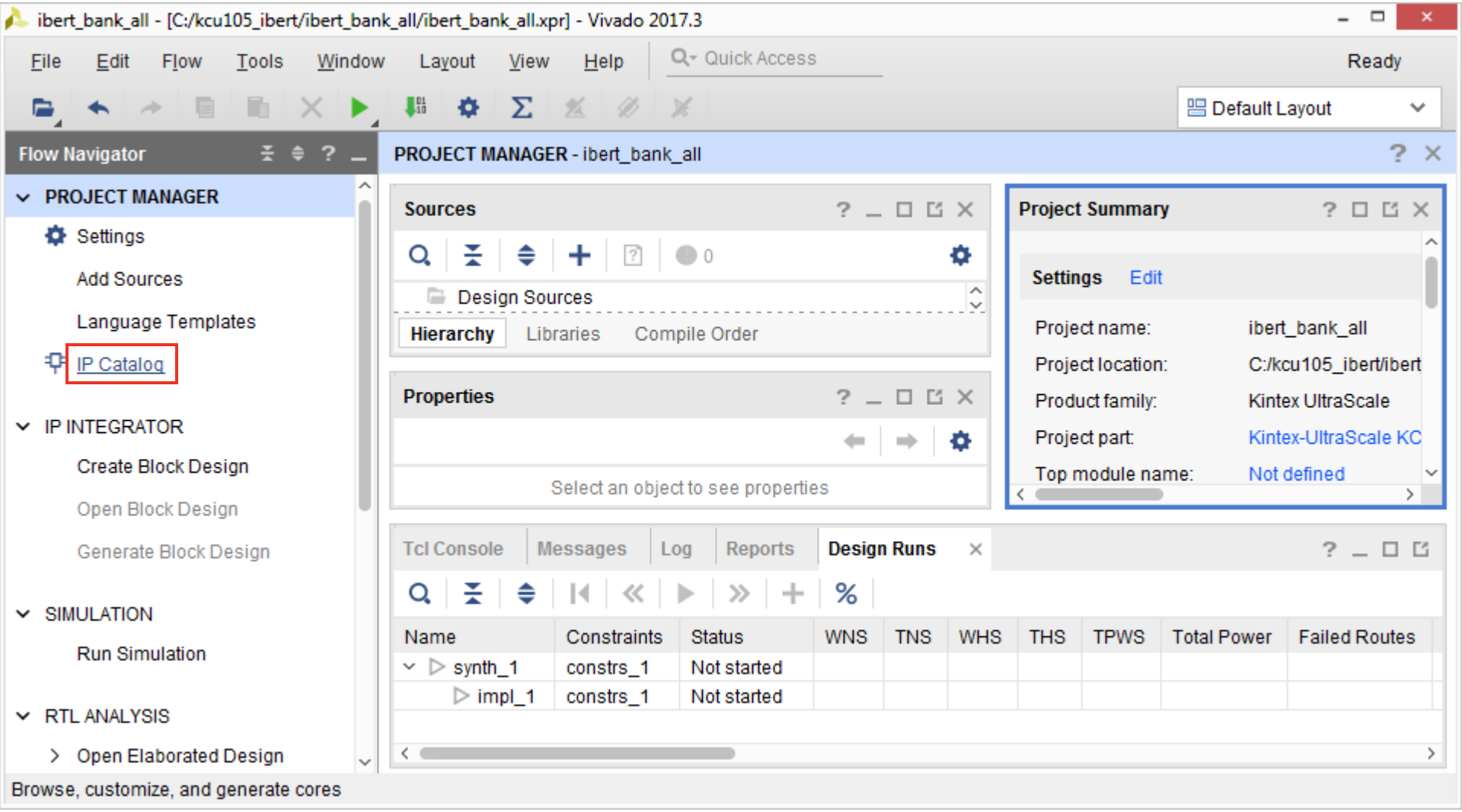
- Click **Finish**



Note: Presentation applies to the KCU105

Create IBERT Design for All Banks

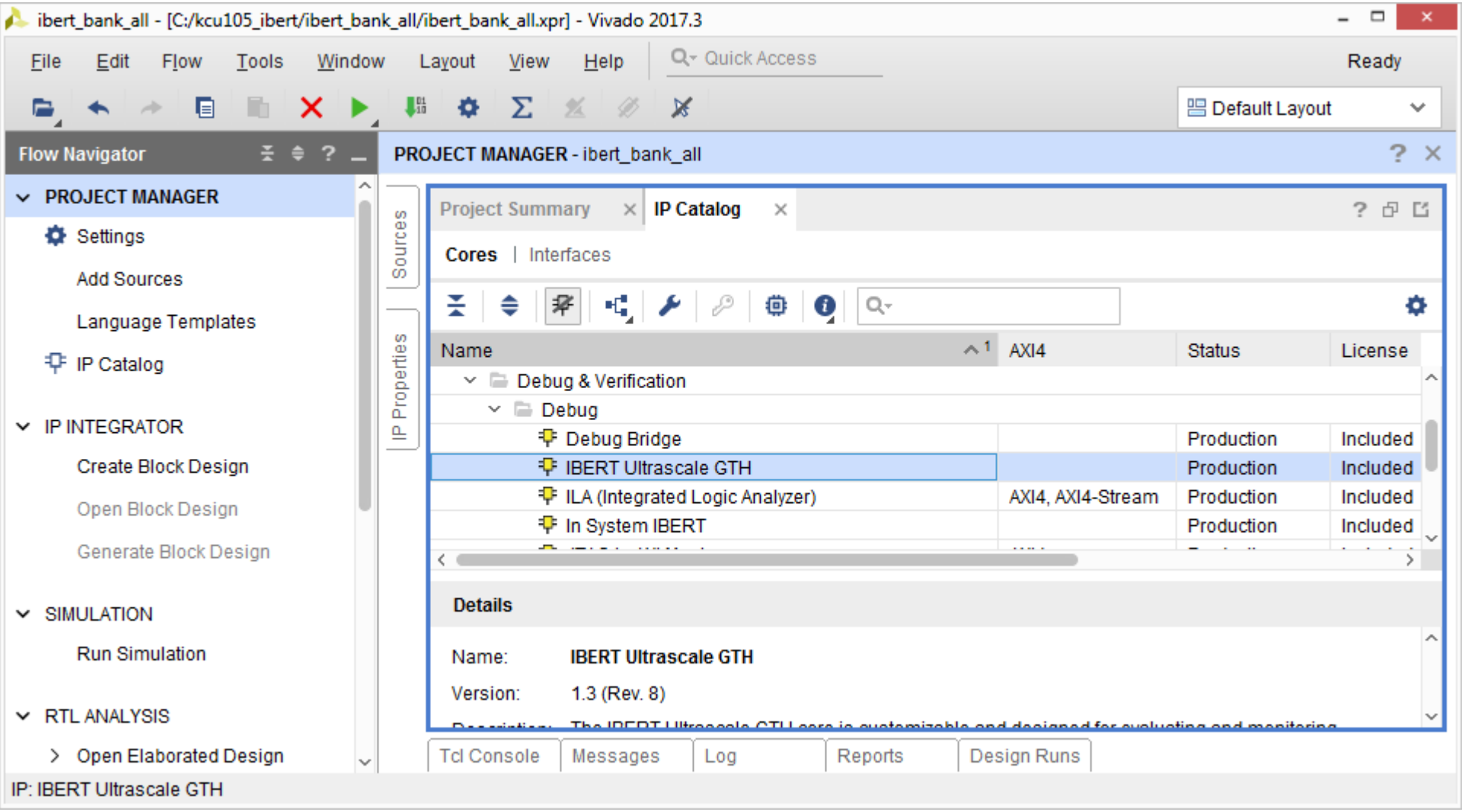
- Click on **IP Catalog**



Note: Presentation applies to the KCU105

Create IBERT Design for All Banks

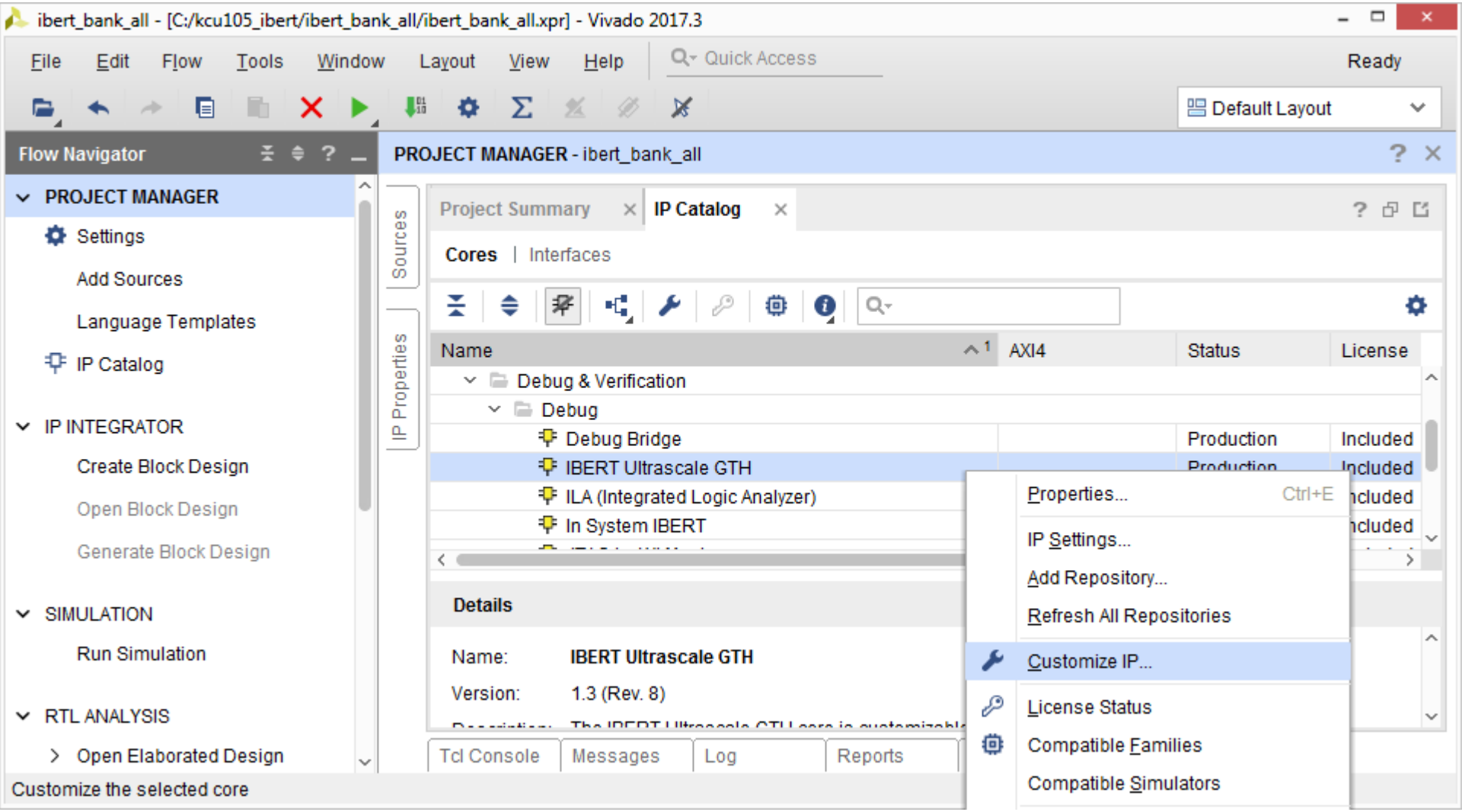
- Select **IBERT UltraScale GTH, v1.3** under Debug & Verification



Note: Presentation applies to the KCU105

Create IBERT Design for All Banks

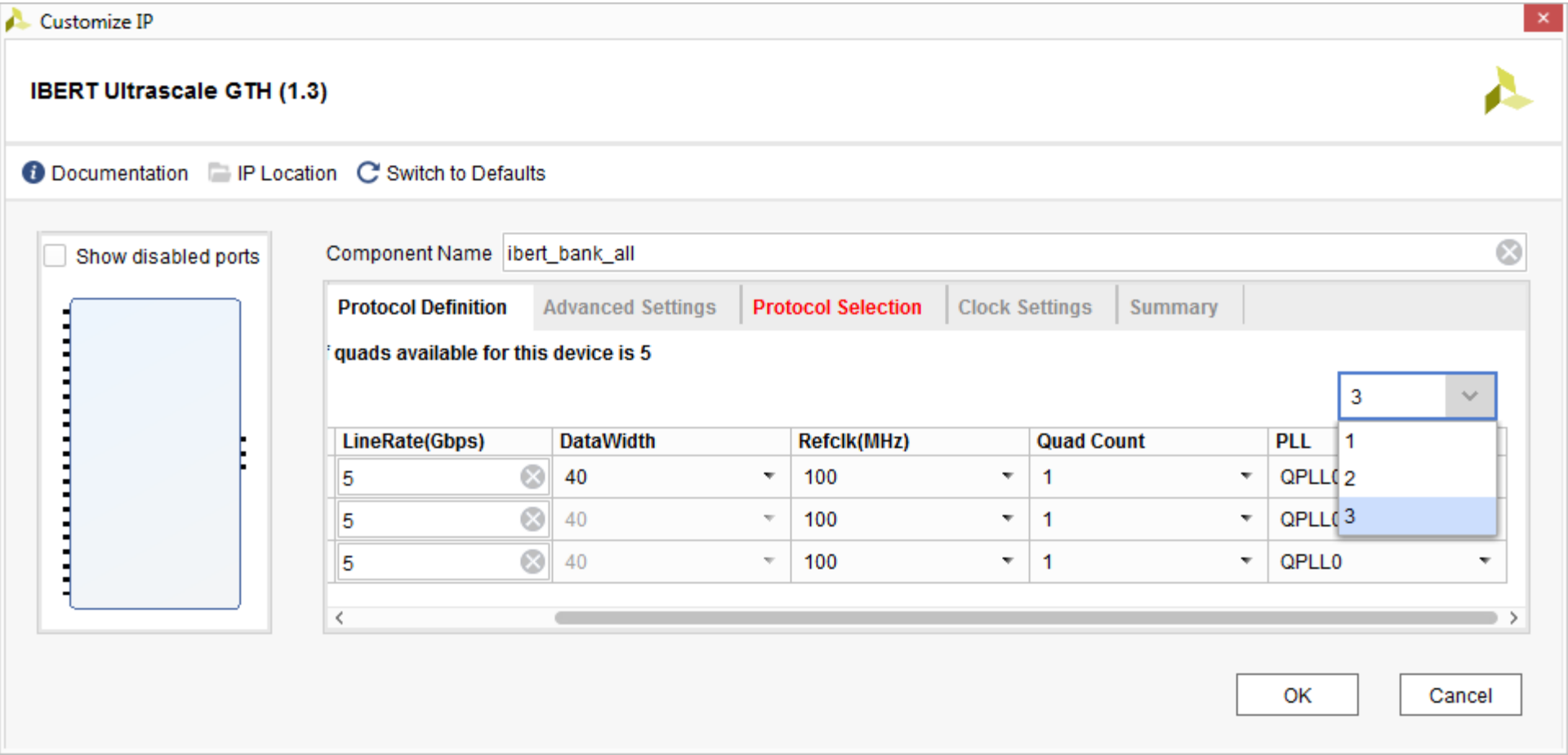
- Right click on **IBERT UltraScale GTH** and select **Customize IP…**



Note: Presentation applies to the KCU105

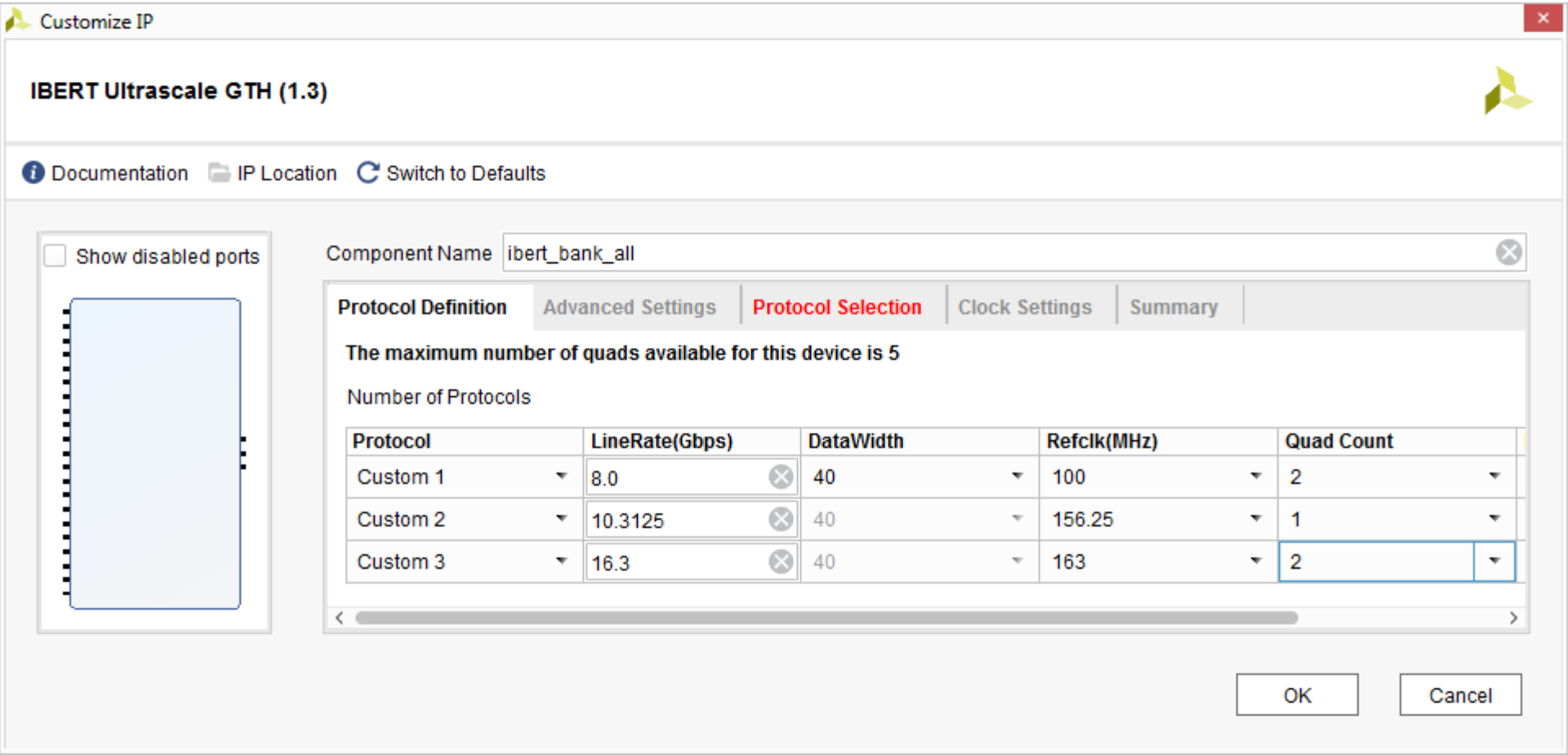
Create IBERT Design for All Banks

- Set the Component name: **ibert_bank_all**
- Under the **Protocol Definition** tab
  - Select **3** Protocols



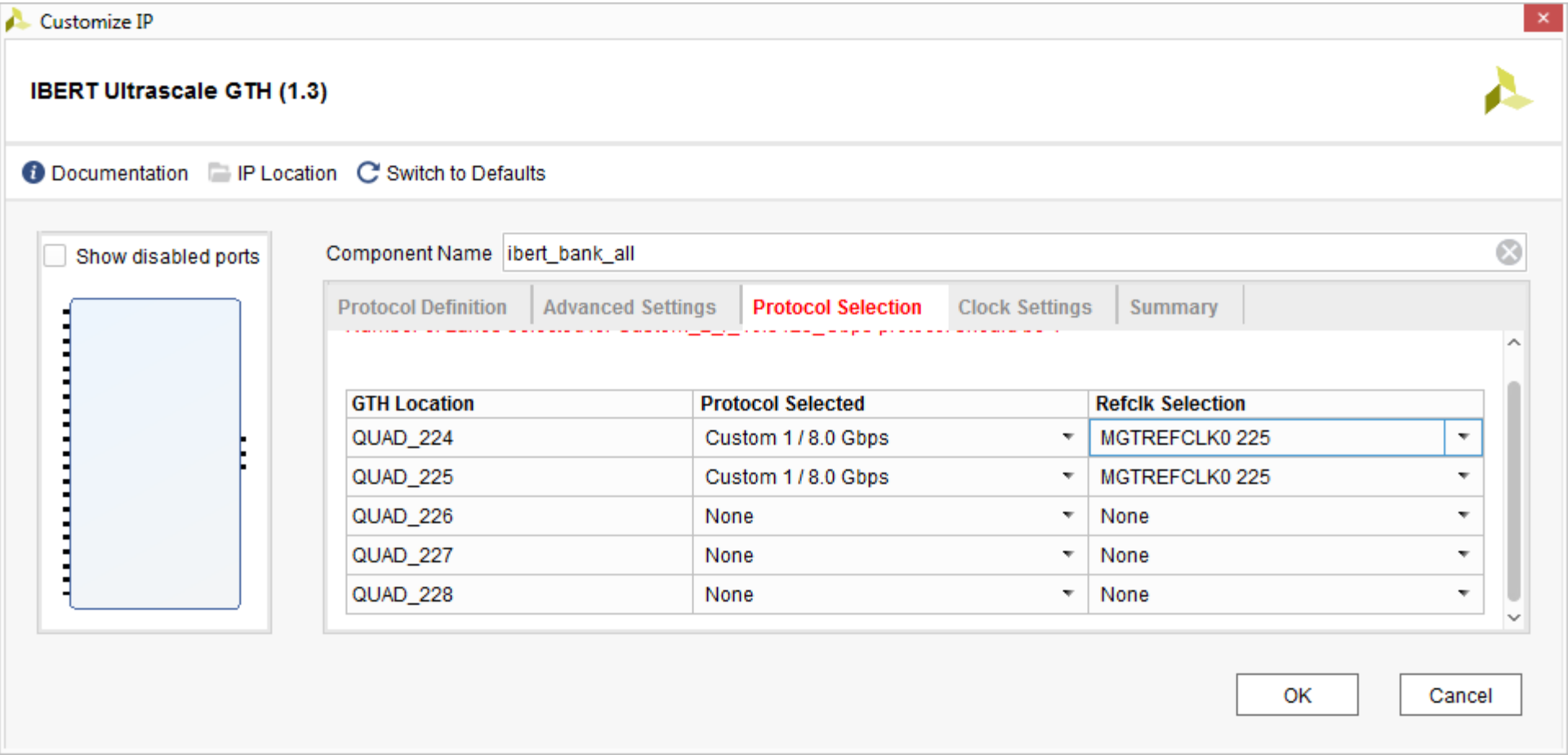
Create IBERT Design for All Banks

- Under the **Protocol Definition** tab
  - Protocol **Custom 1**: LineRate: **8.0**, Refclk: **100** Quad Count: **2**
  - Protocol **Custom 2**: LineRate: **10.3125**, Refclk: **156.25** Quad Count: **1**
  - Protocol **Custom 3**: LineRate: **16.3**, Refclk: **163** Quad Count: **2**



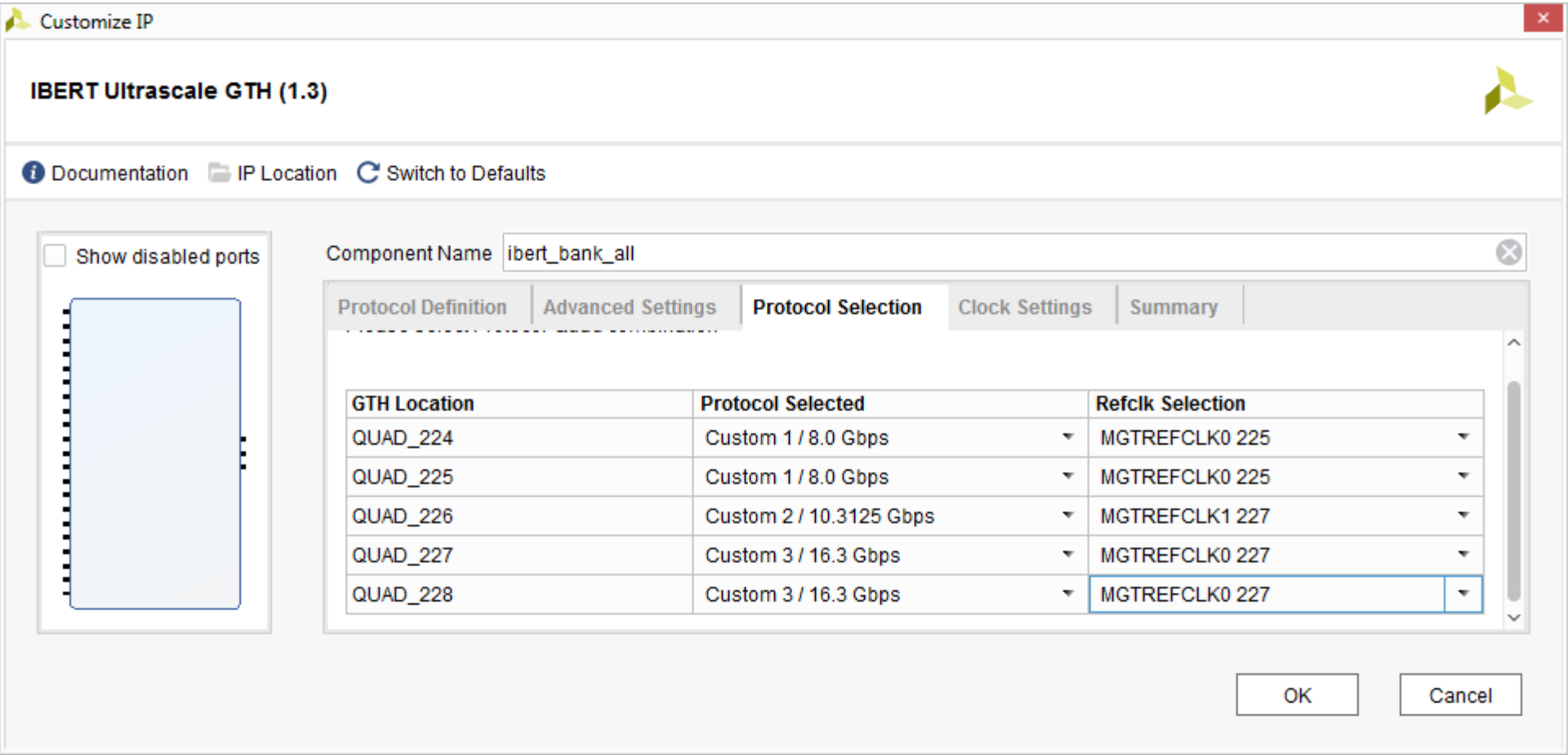
Create IBERT Design for All Banks

- Under the **Protocol Selection** tab
- Set **QUAD_224** and **QUAD_225** to
  - **Custom 1 / 8.0 Gbps**, and **MGTREFCLK0 225**



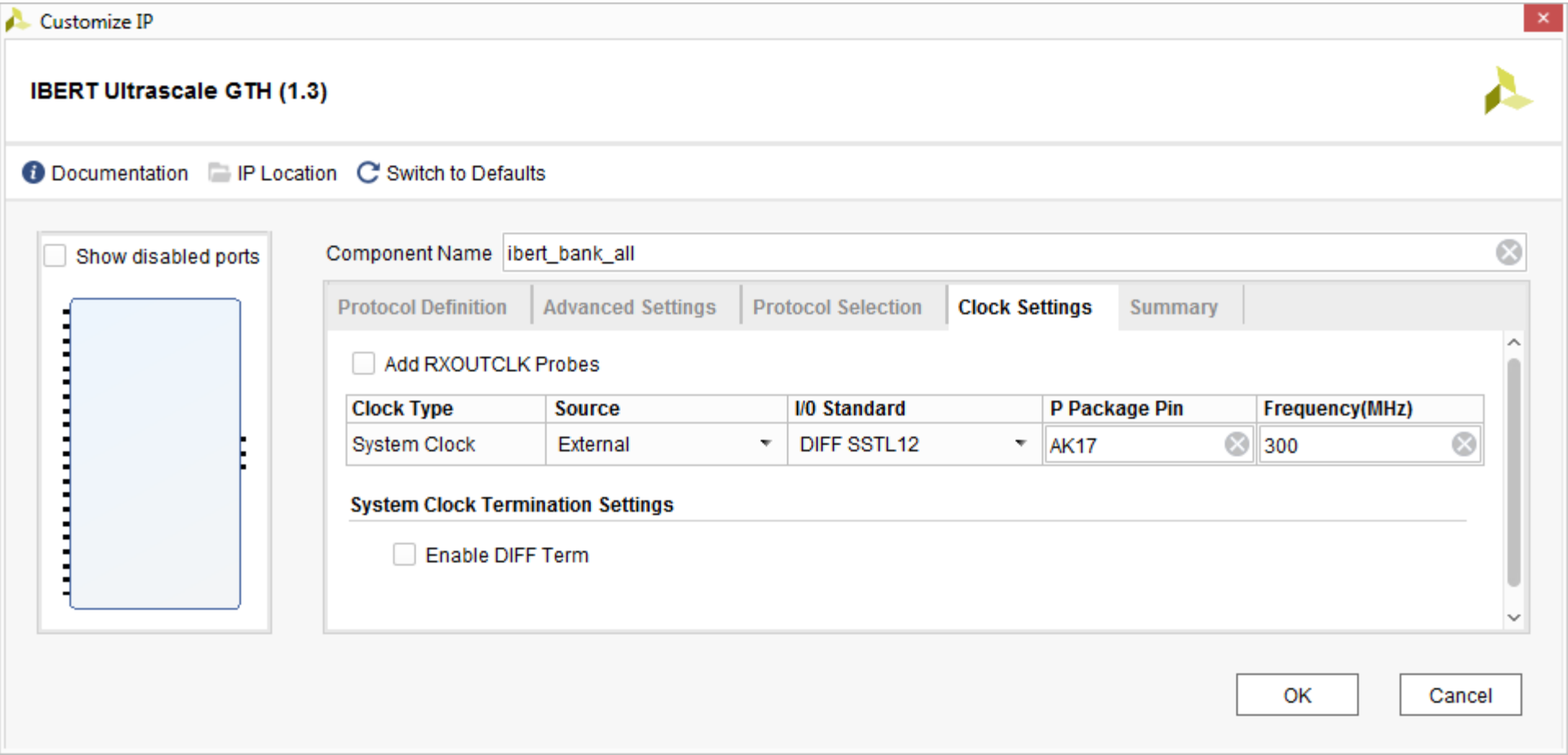
Create IBERT Design for All Banks

- Set **QUAD_226** to
  - **Custom 2 / 10.3125 Gbps**, and **MGTREFCLK1 227**
- Set **QUAD_227** and **QUAD_228** to
  - **Custom 3 / 16.3 Gbps**, and **MGTREFCLK0 227**



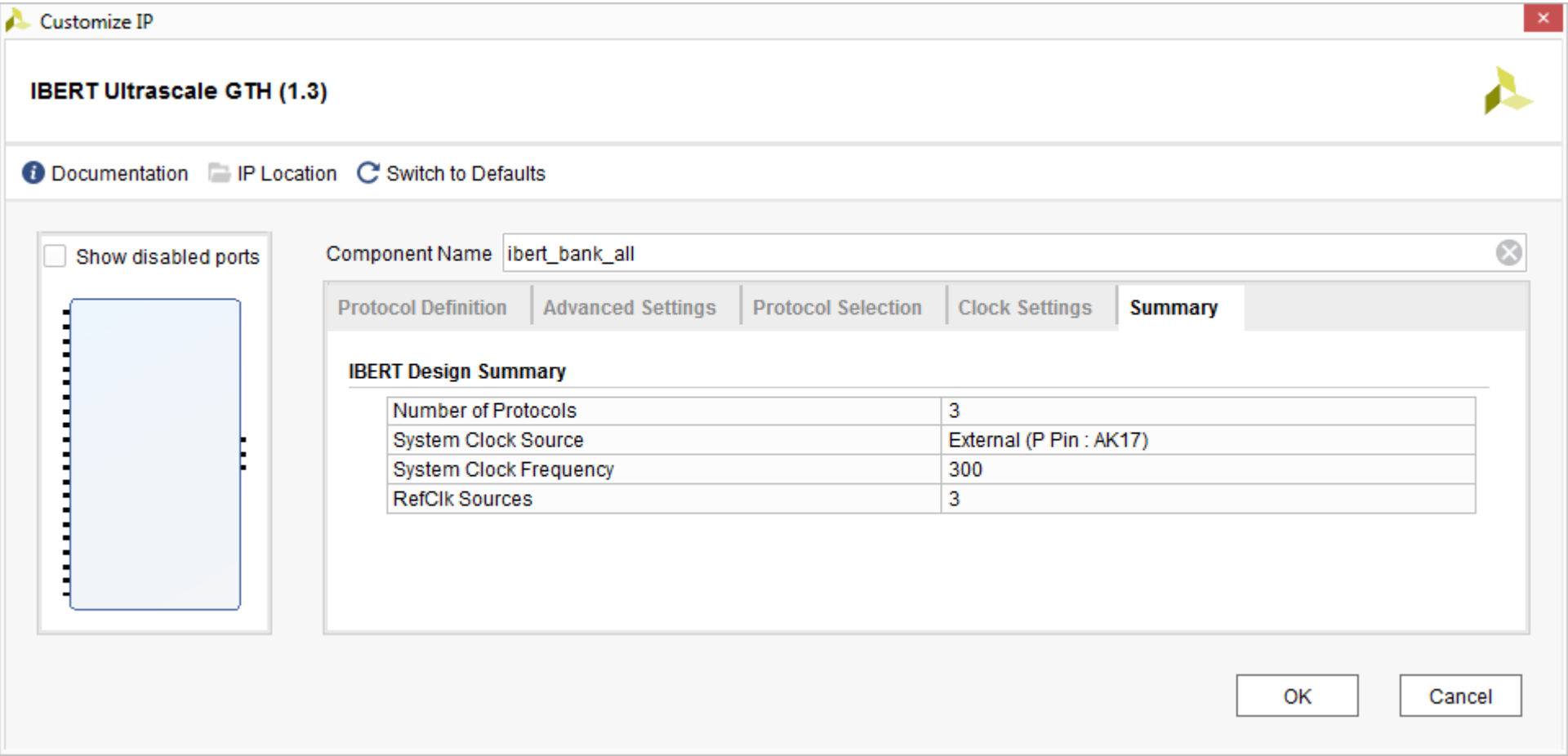
Create IBERT Design for All Banks

- Under the **Clock Settings** tab, set the System Clock:
  - **DIFF SSTL12**, P Package Pin: **AK17**, Frequency: **300**
  - Deselect **Enable DIFF Term**



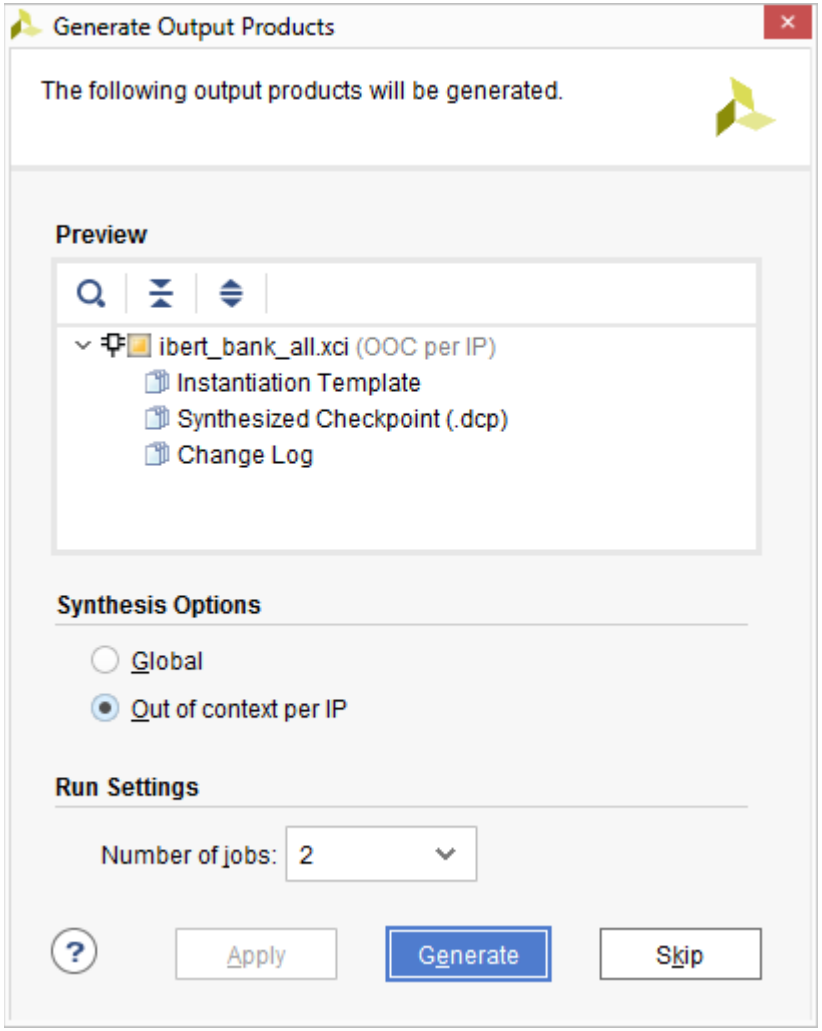
Create IBERT Design for All Banks

- Review the summary and click **OK**



Create IBERT Design for All Banks

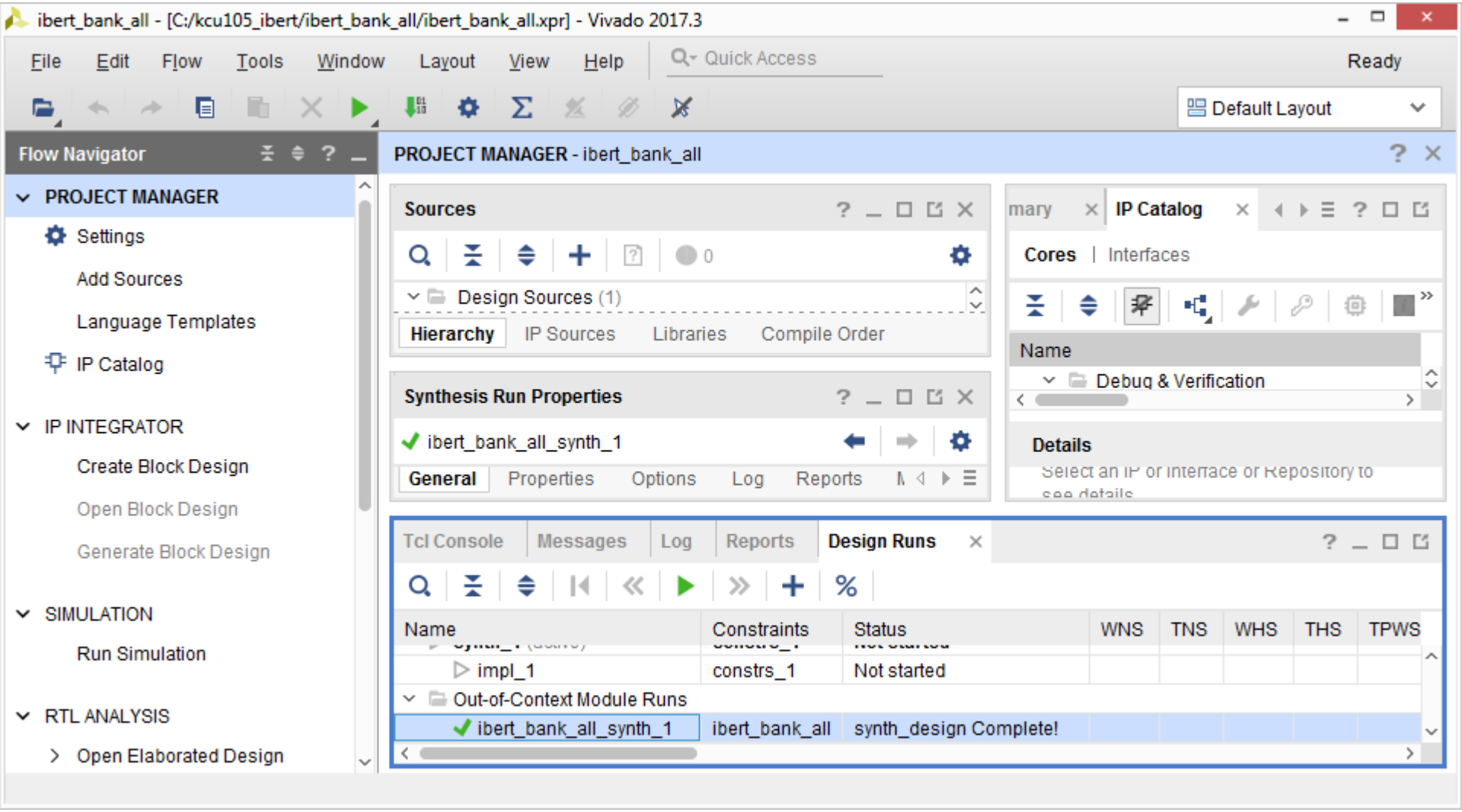
- Click **Generate**



Note: This step will take about 10 minutes

Create IBERT Design for All Banks

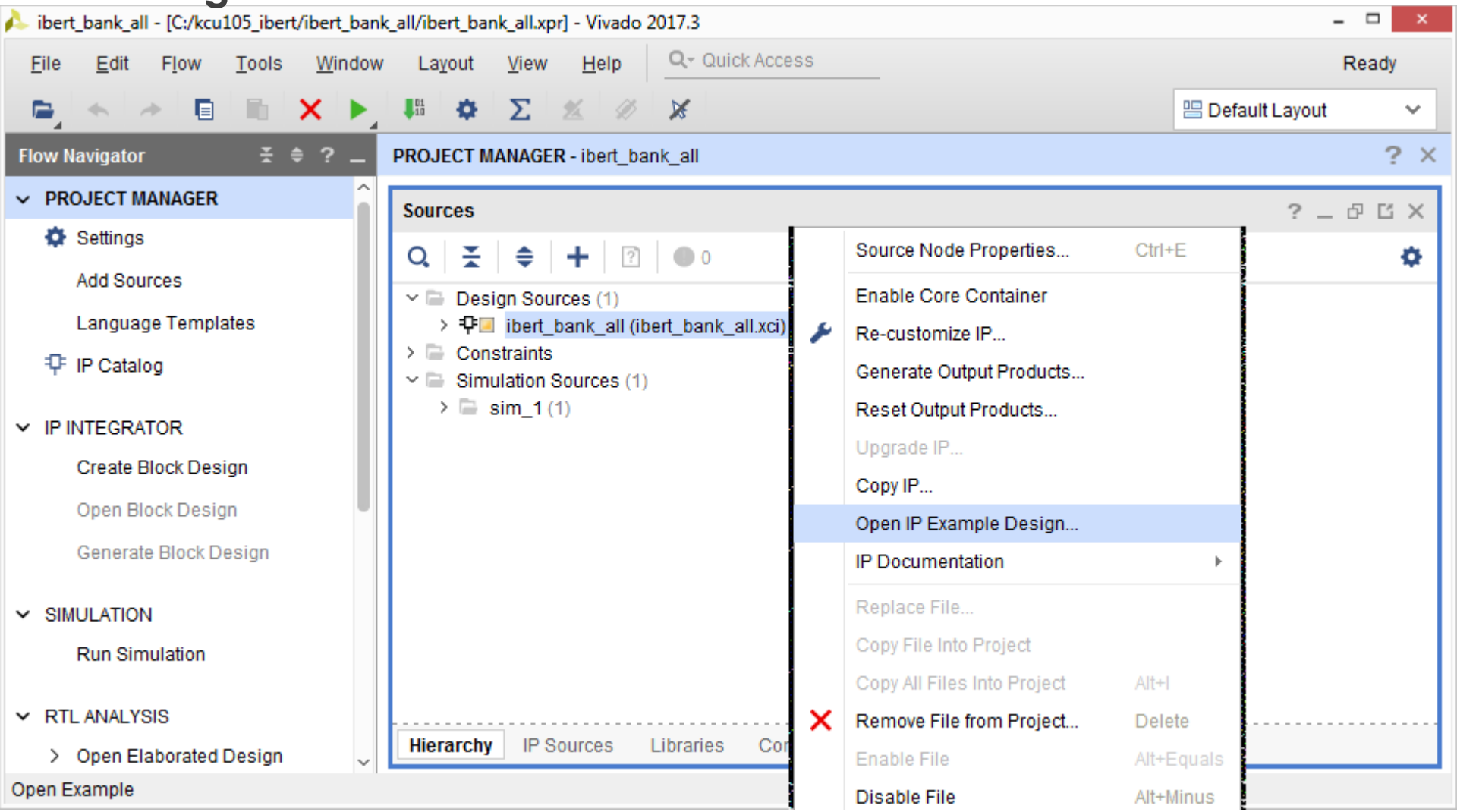
- The Generated IBERT IP appears in Design Sources
  - Wait until checkmark appears on **ibert_bank_all_synth_1**



Note: Presentation applies to the KCU105

Compile Example Design

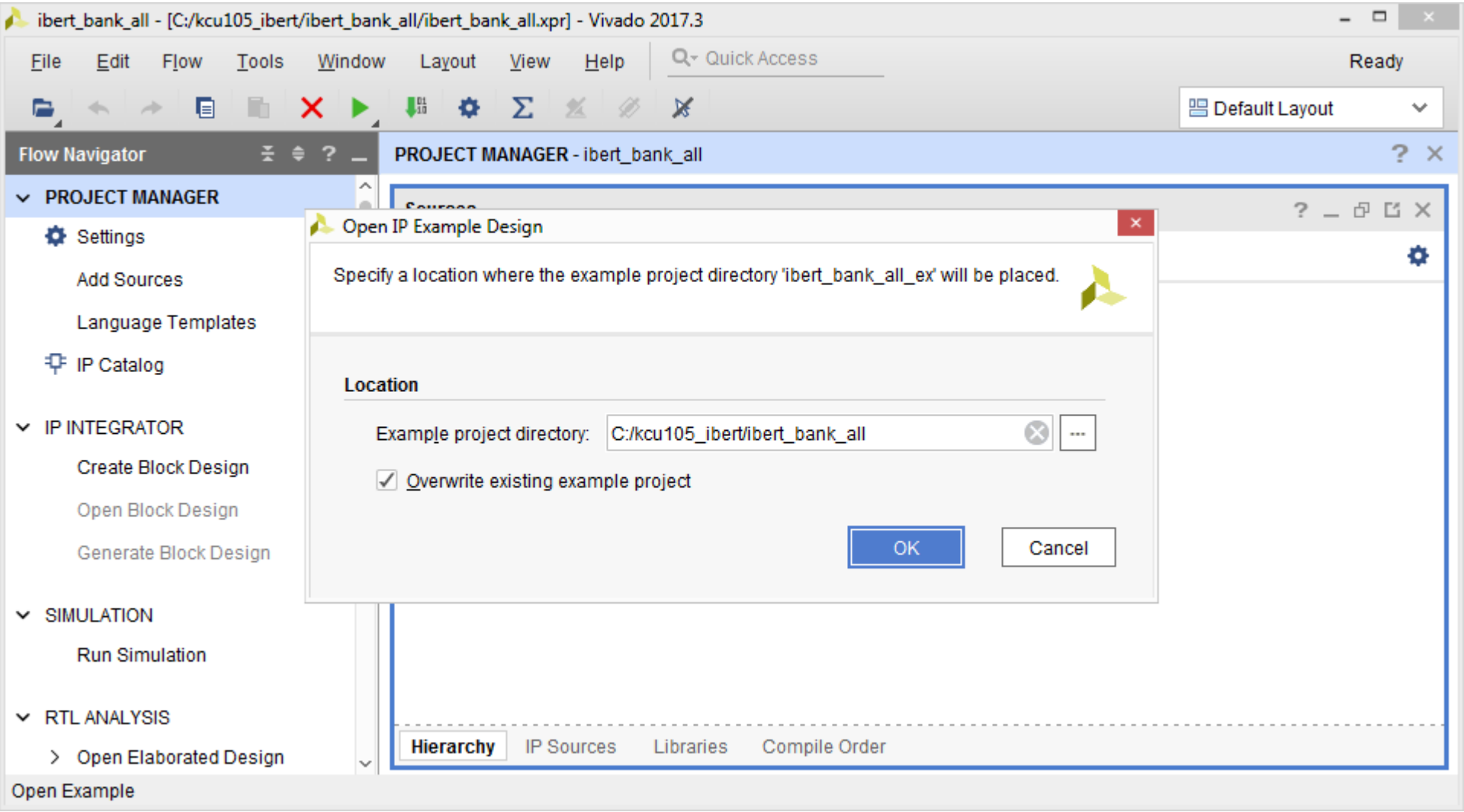
- Right click on **ibert_bank_all** and select **Open IP Example Design…**



Note: Presentation applies to the KCU105

Compile Example Design

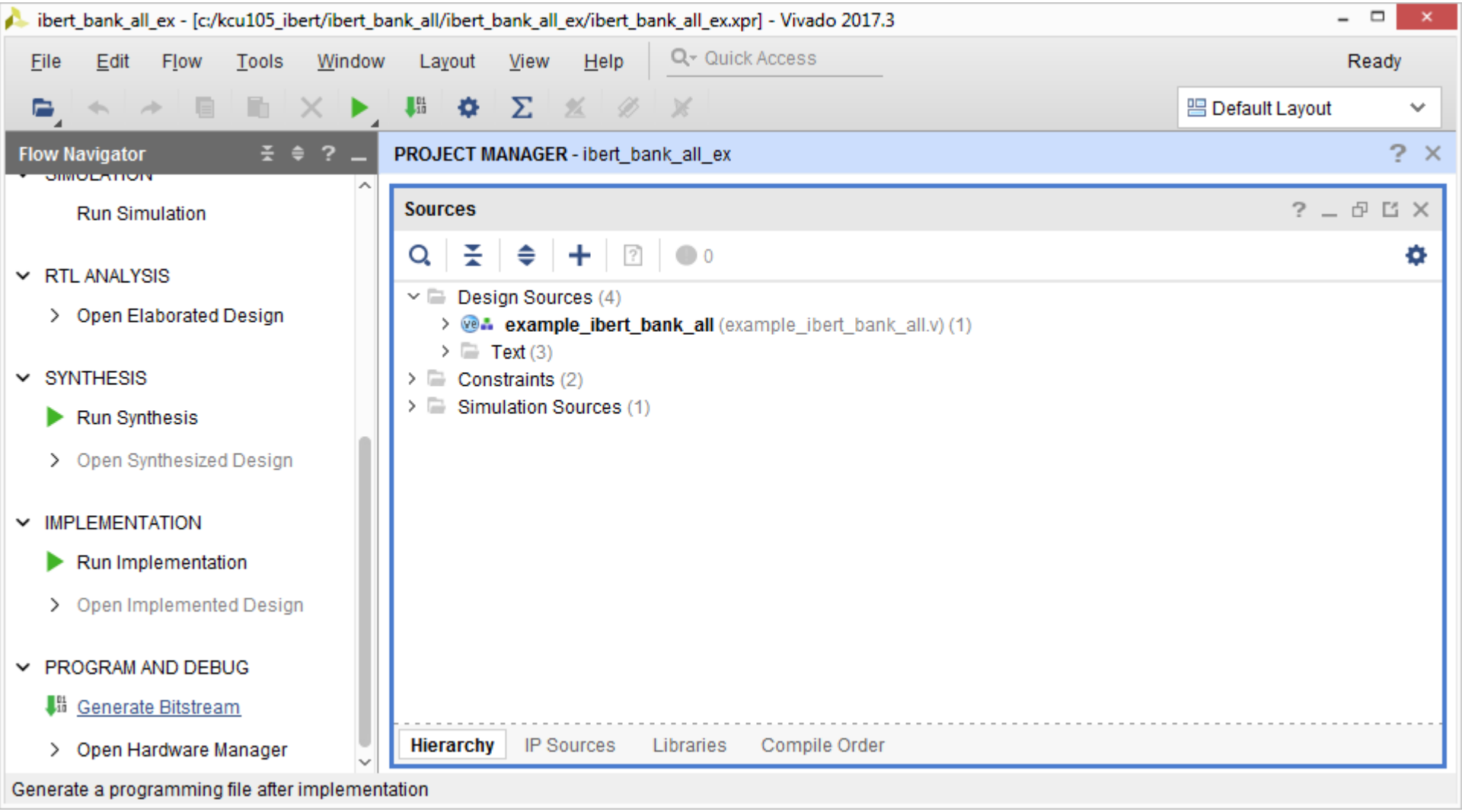
- Set the location to **C:/kcu105_ibert/ibert_bank_all** and click **OK**



Note: Presentation applies to the KCU105

Compile Example Design

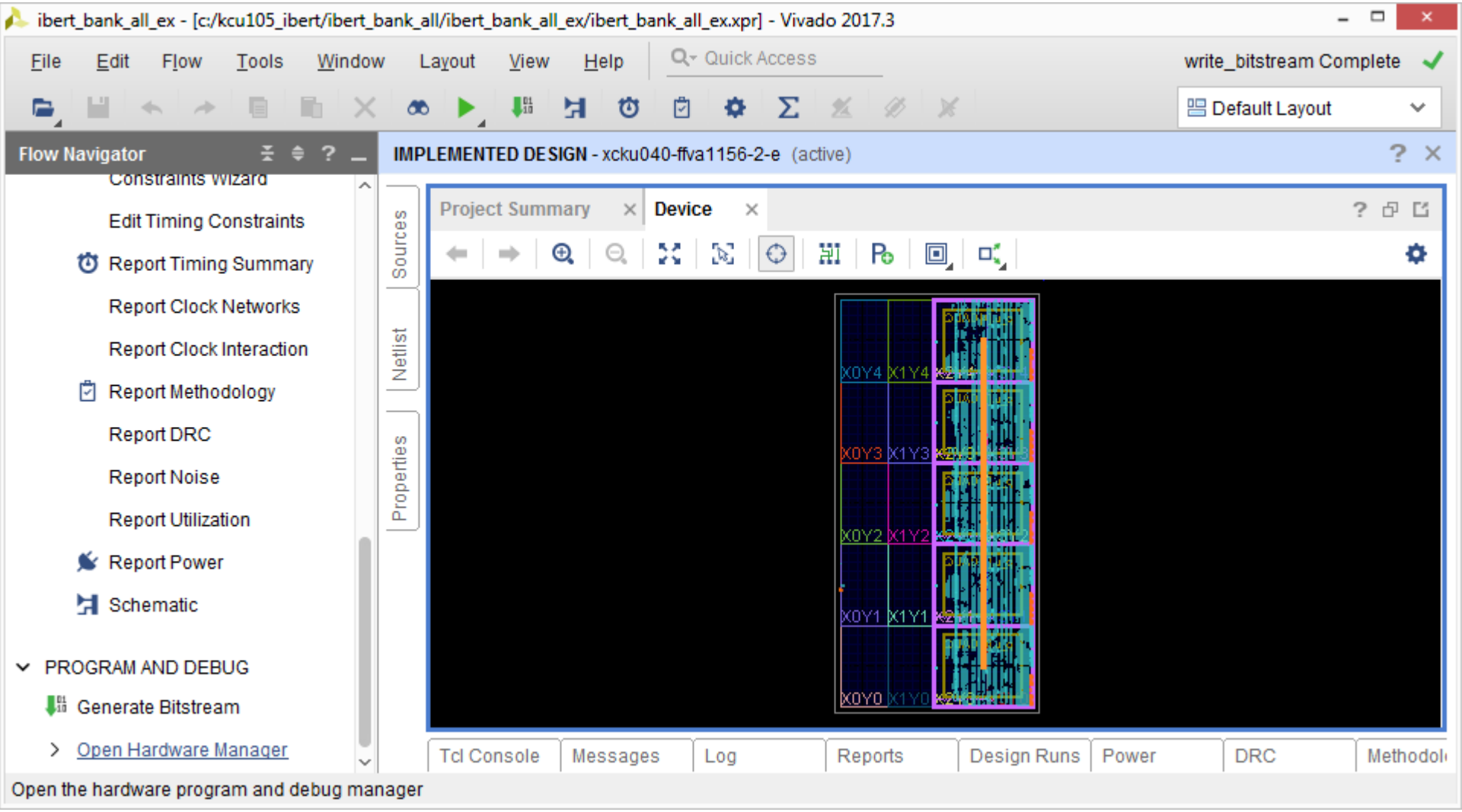
- A new project is created
- Click **Generate Bitstream**



Note: The original project window can be closed

Compile Example Design

- Open and view the Implemented Design
- Click **Open Hardware Manager**

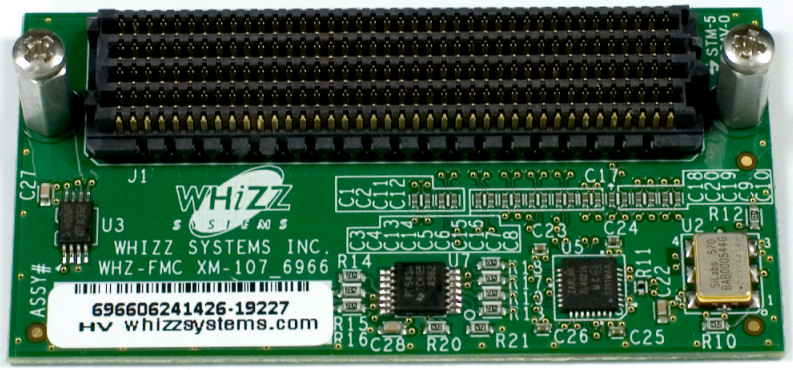


Note: Presentation applies to the KCU105

Testing All Banks with Optional User Provided Hardware

Hardware Setup with User Provided Hardware

- Attach a second XM107 to the LPC connector
  - Additional XM107 boards available through Whizz Systems



Note: Presentation applies to the KCU105

Hardware Setup with User Provided Hardware

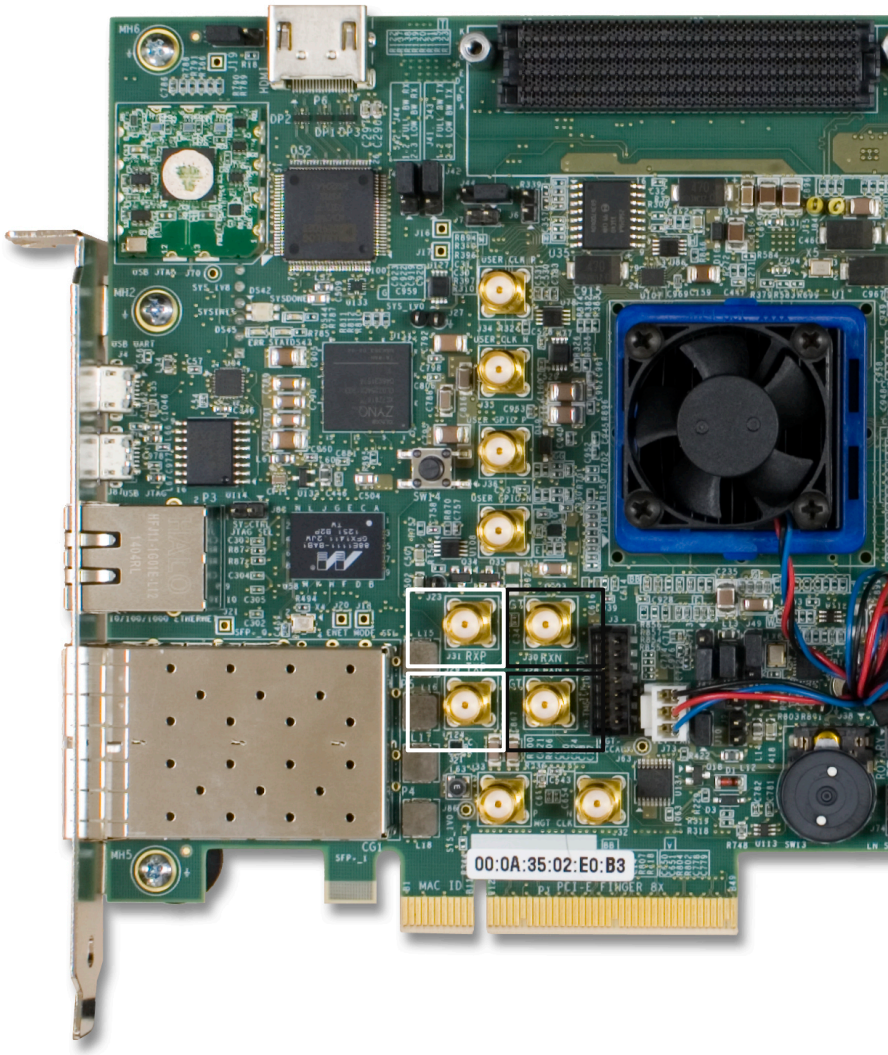
- Two SMA Cables
  - www.rosenbergerna.com
  - Part number: 72D-32S1-32S1-00610A

- Optional: SMA Quick connects
  - RADIALL
  - Part number: R125791501
  - Available here or here

Note: Presentation applies to the KCU105

Hardware Setup

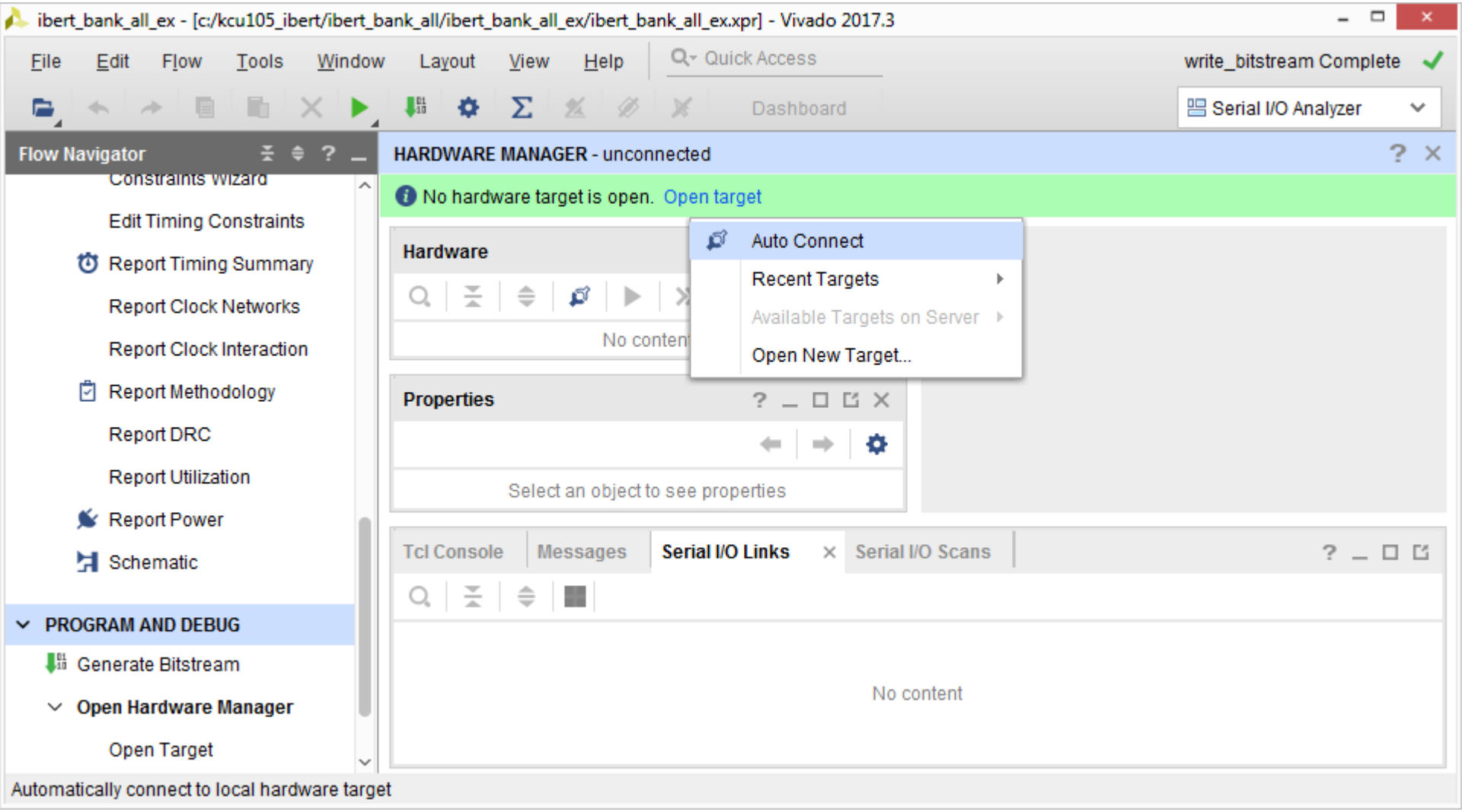
- Hook up the SMA cables as shown
- IBERT Test:
  - J29 to J31 (White)
  - J28 to J30 (Black)



Note: Presentation applies to the KCU105

Run IBERT Example Design

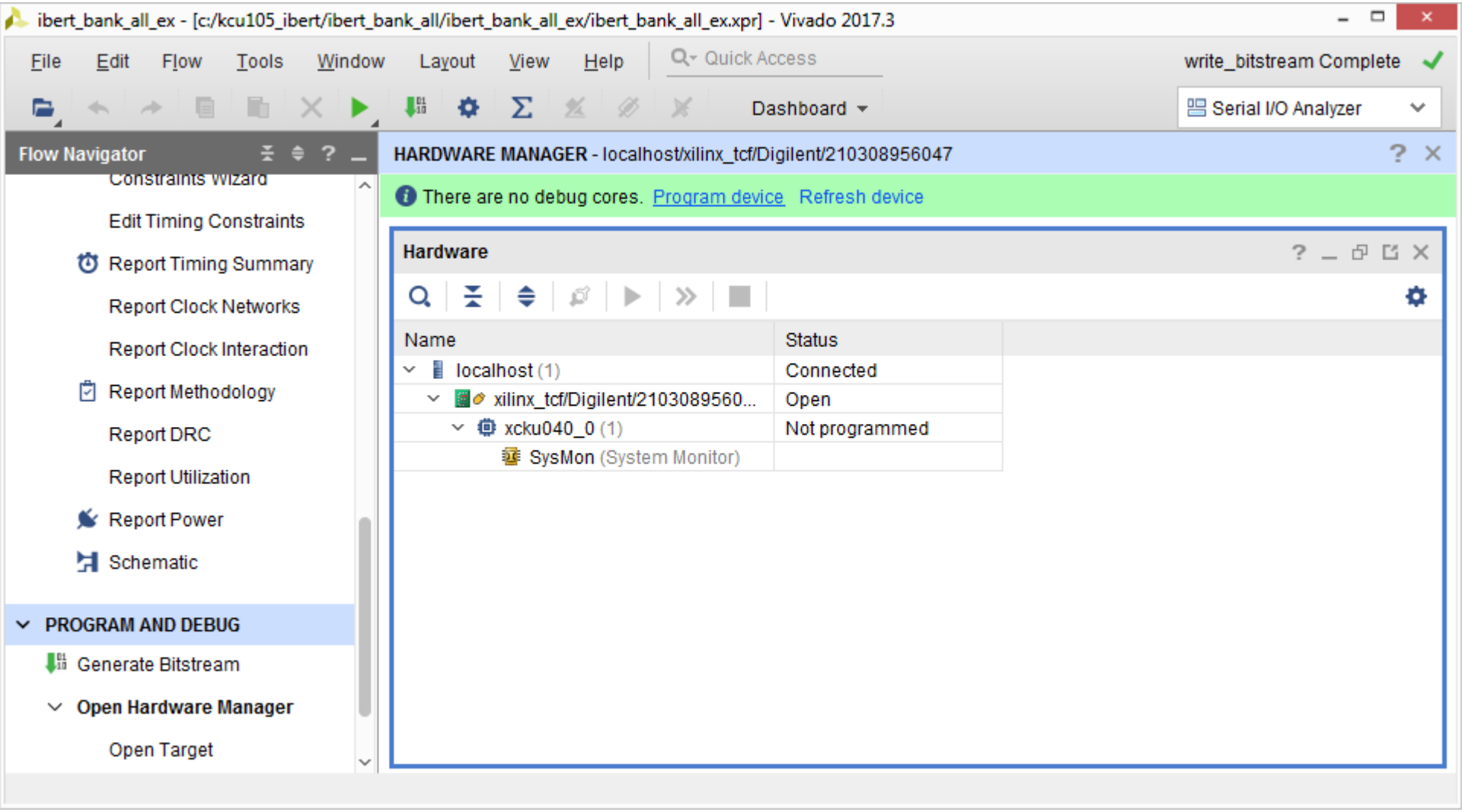
- Click **Open target** and select **Auto Connect**



Note: Presentation applies to the KCU105

Run IBERT Example Design

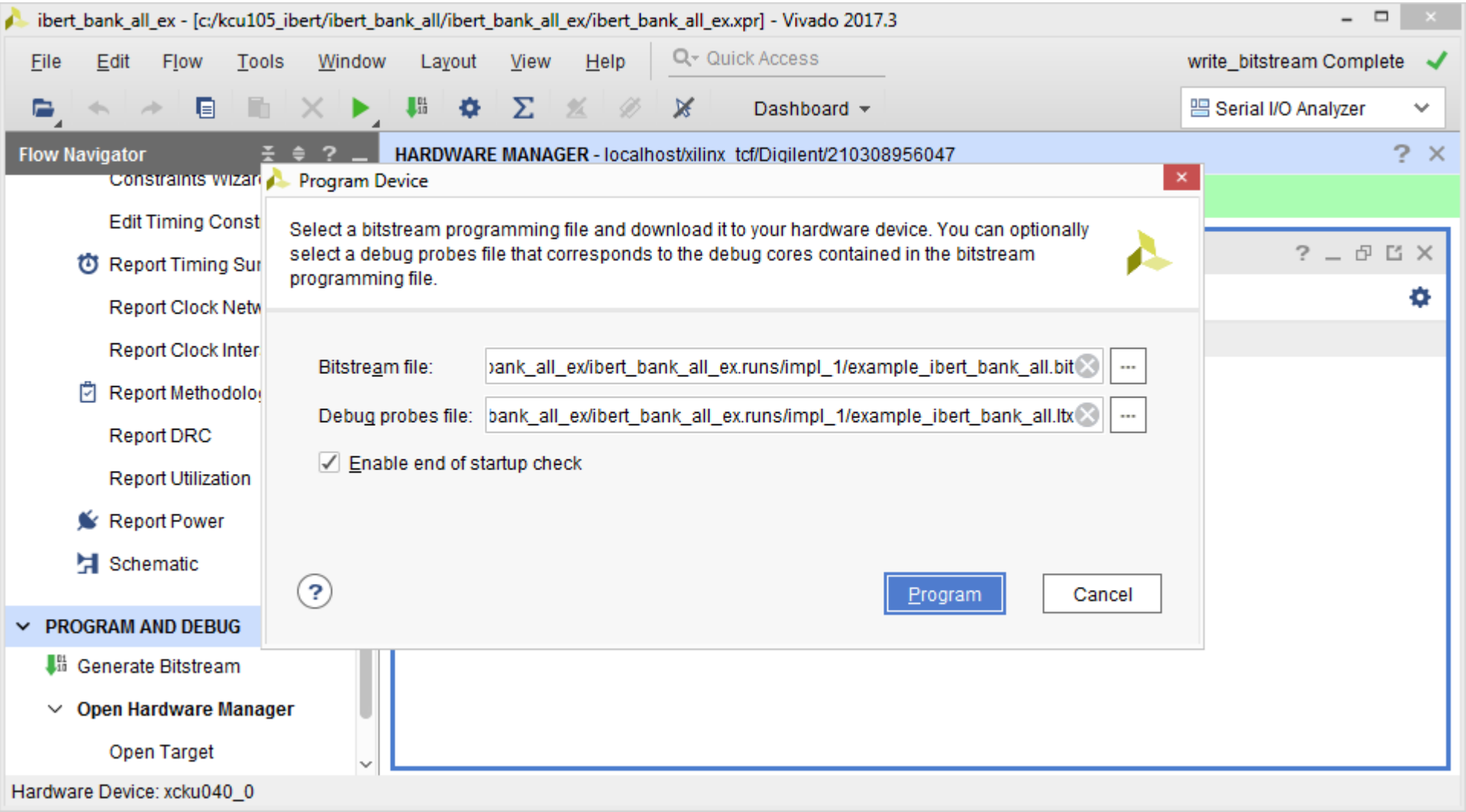
- Select **Program device**



Note: Presentation applies to the KCU105

Run IBERT Example Design

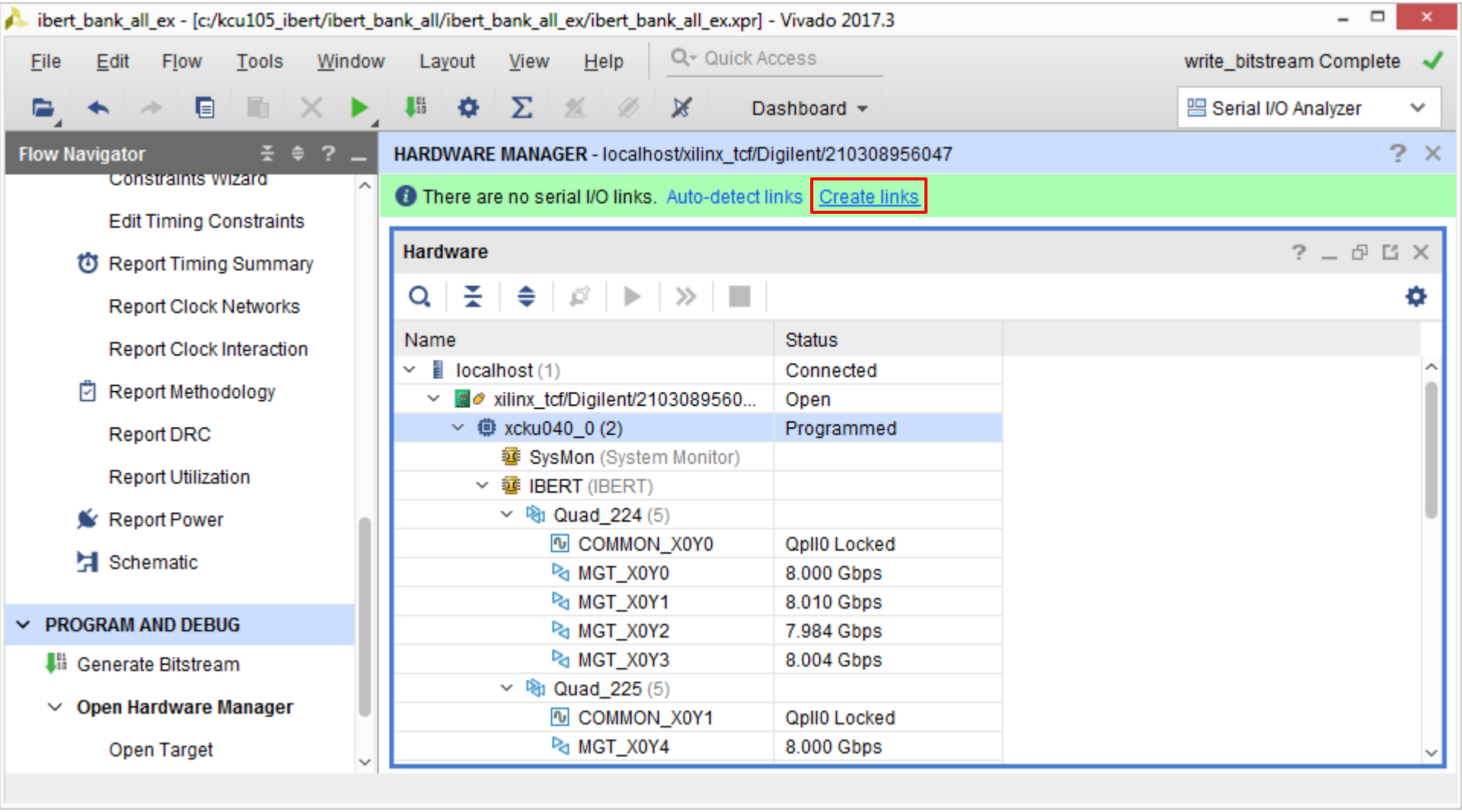
- The newly created bitstream and LTX files are set to the default
- Click **Program**



Note: Presentation applies to the KCU105

Run IBERT Example Design

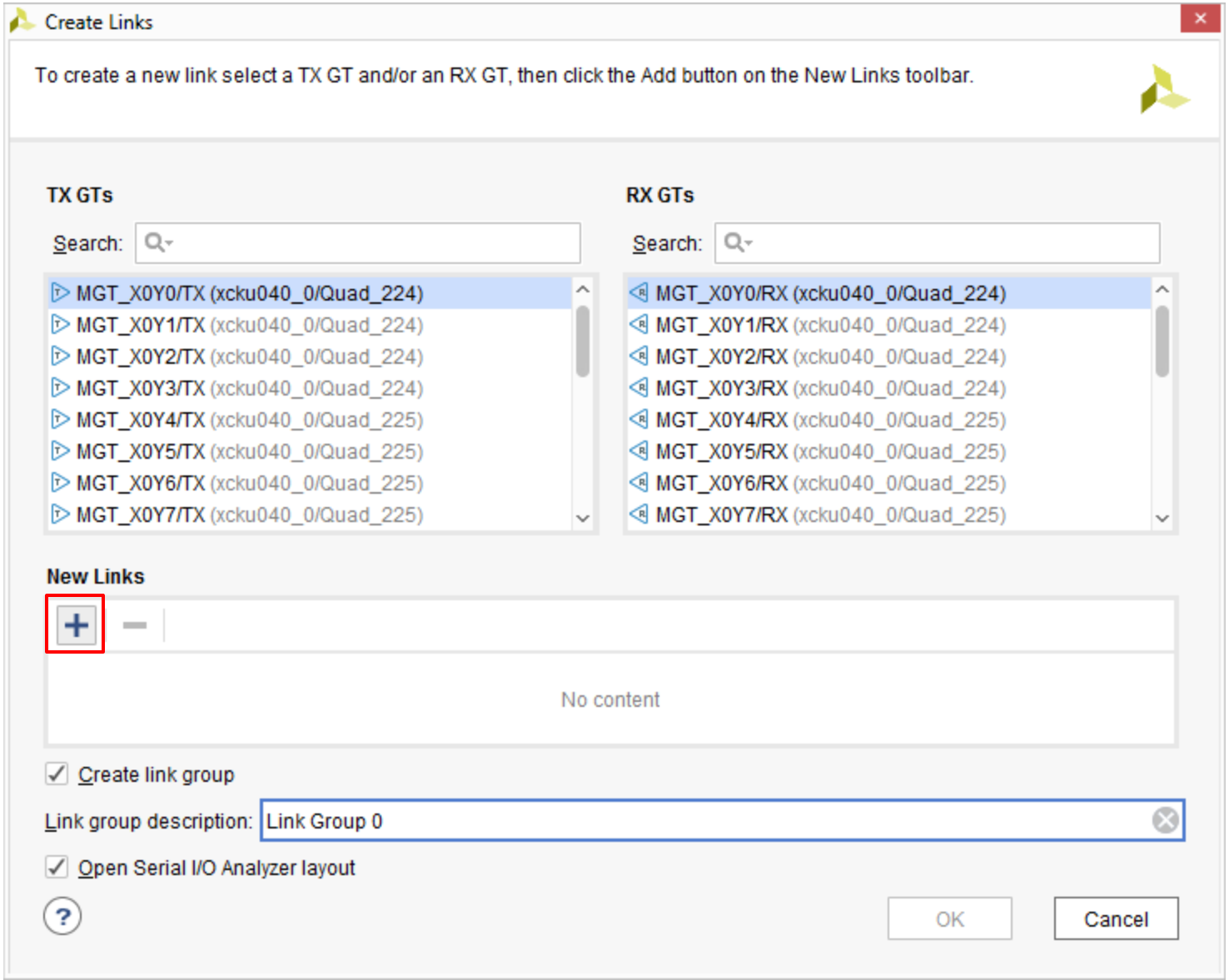
- Click **Create links**



Note: Si570 and Si5328 clocks must be set as per XTP352

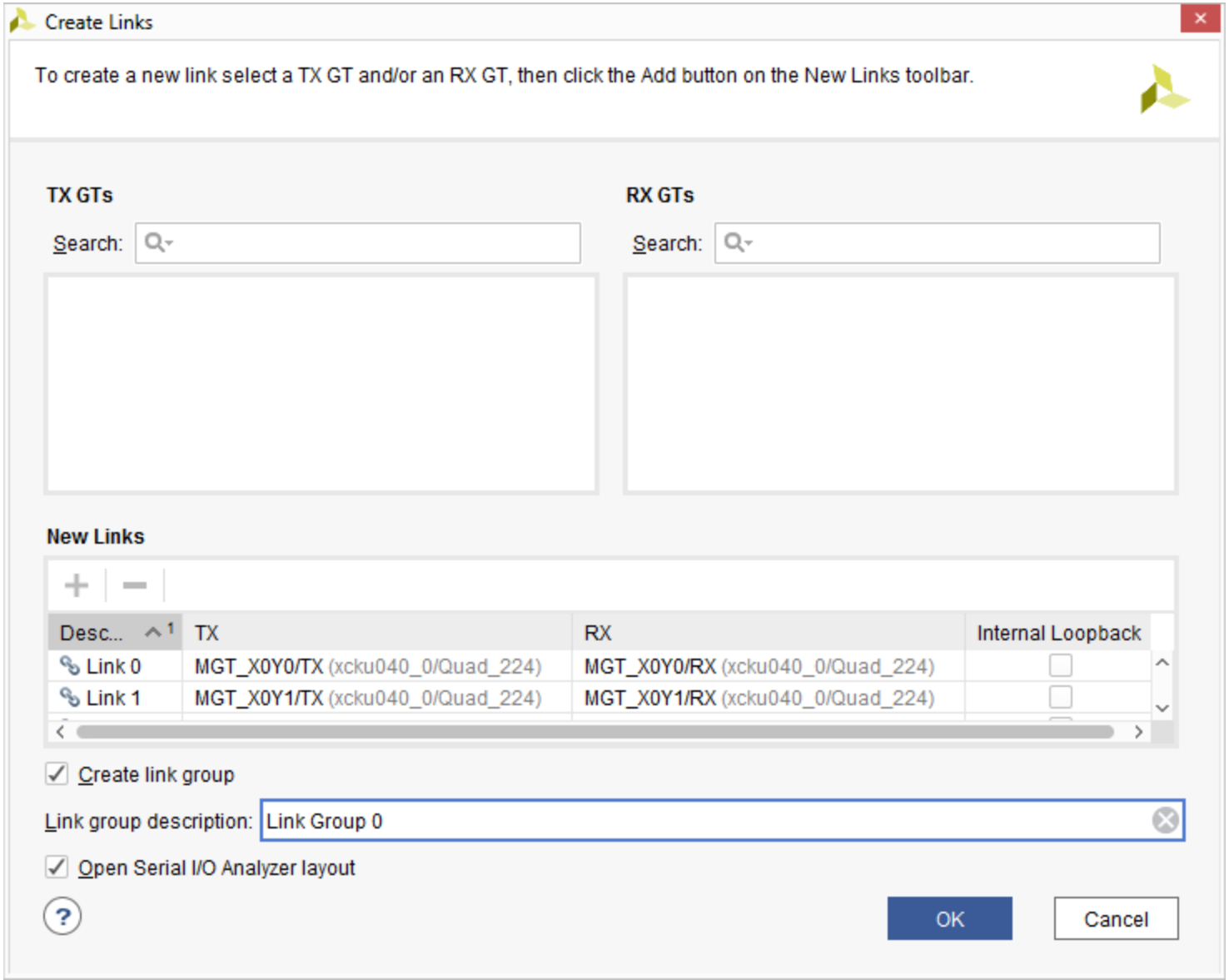
Run IBERT Example Design

- Click on the Add Link button



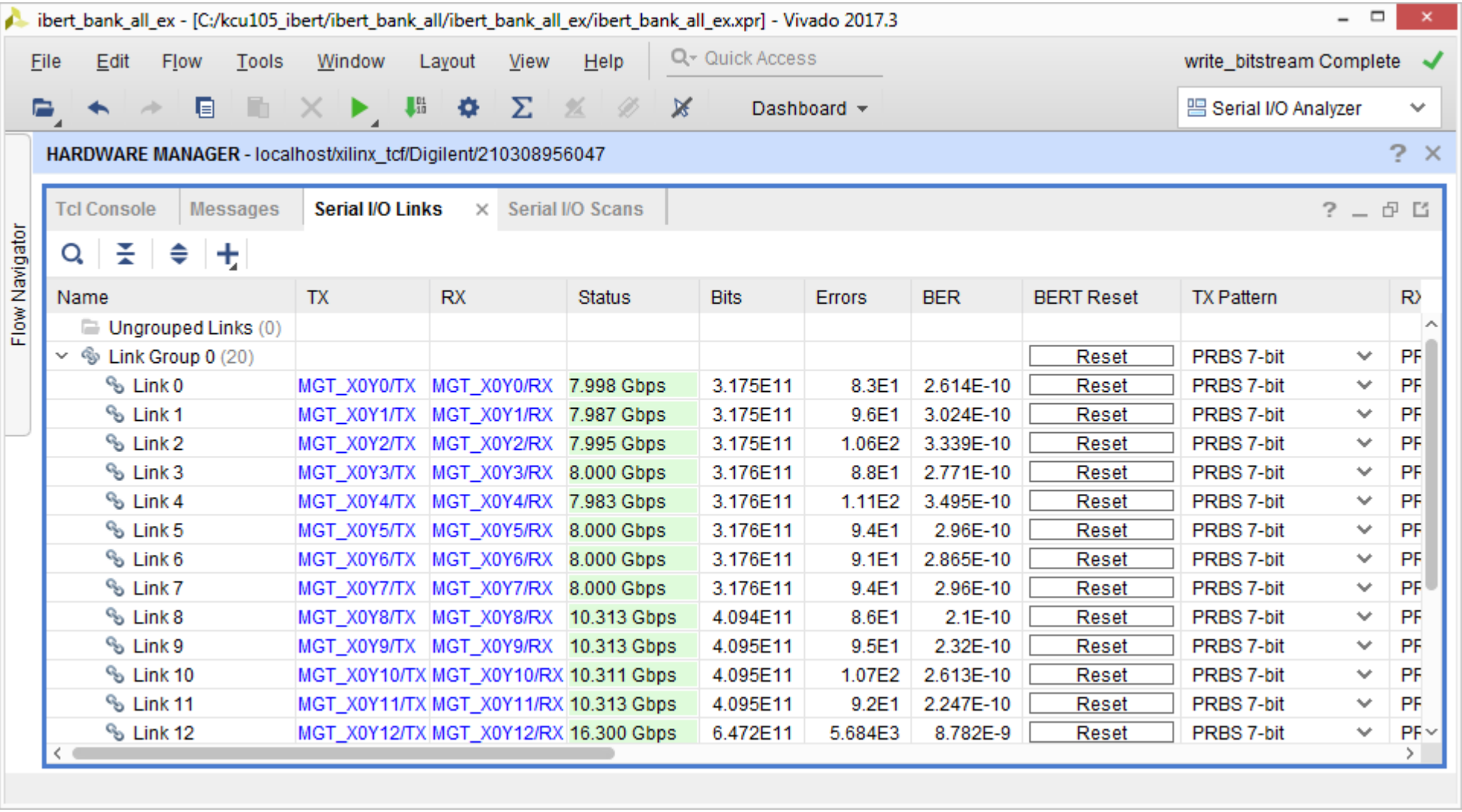
Run IBERT Example Design

- Add all the links and click **OK**



Run IBERT Example Design

- The links appear under the **Serial I/O Links** tab

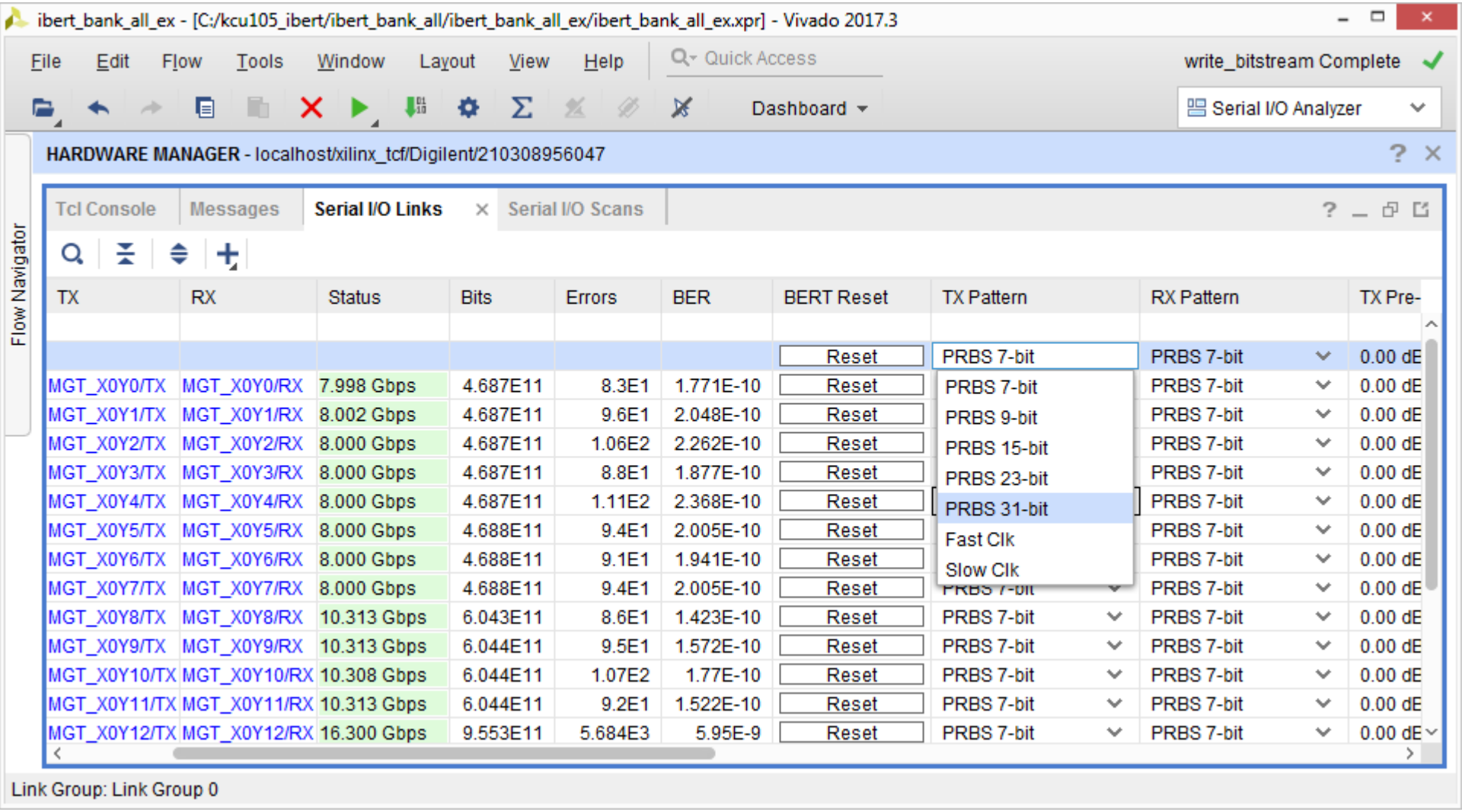


Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX
Ungrouped Links (0)									
Link Group 0 (20)							Reset	PRBS 7-bit	PF
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	7.998 Gbps	3.175E11	8.3E1	2.614E-10	Reset	PRBS 7-bit	PF
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	7.987 Gbps	3.175E11	9.6E1	3.024E-10	Reset	PRBS 7-bit	PF
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	7.995 Gbps	3.175E11	1.06E2	3.339E-10	Reset	PRBS 7-bit	PF
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	3.176E11	8.8E1	2.771E-10	Reset	PRBS 7-bit	PF
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	7.983 Gbps	3.176E11	1.11E2	3.495E-10	Reset	PRBS 7-bit	PF
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	8.000 Gbps	3.176E11	9.4E1	2.96E-10	Reset	PRBS 7-bit	PF
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	8.000 Gbps	3.176E11	9.1E1	2.865E-10	Reset	PRBS 7-bit	PF
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	8.000 Gbps	3.176E11	9.4E1	2.96E-10	Reset	PRBS 7-bit	PF
Link 8	MGT_X0Y8/TX	MGT_X0Y8/RX	10.313 Gbps	4.094E11	8.6E1	2.1E-10	Reset	PRBS 7-bit	PF
Link 9	MGT_X0Y9/TX	MGT_X0Y9/RX	10.313 Gbps	4.095E11	9.5E1	2.32E-10	Reset	PRBS 7-bit	PF
Link 10	MGT_X0Y10/TX	MGT_X0Y10/RX	10.311 Gbps	4.095E11	1.07E2	2.613E-10	Reset	PRBS 7-bit	PF
Link 11	MGT_X0Y11/TX	MGT_X0Y11/RX	10.313 Gbps	4.095E11	9.2E1	2.247E-10	Reset	PRBS 7-bit	PF
Link 12	MGT_X0Y12/TX	MGT_X0Y12/RX	16.300 Gbps	6.472E11	5.684E3	8.782E-9	Reset	PRBS 7-bit	PF

Note: Presentation applies to the KCU105

Run IBERT Example Design

- Set all TX and RX Patterns to **PRBS 31-bit**

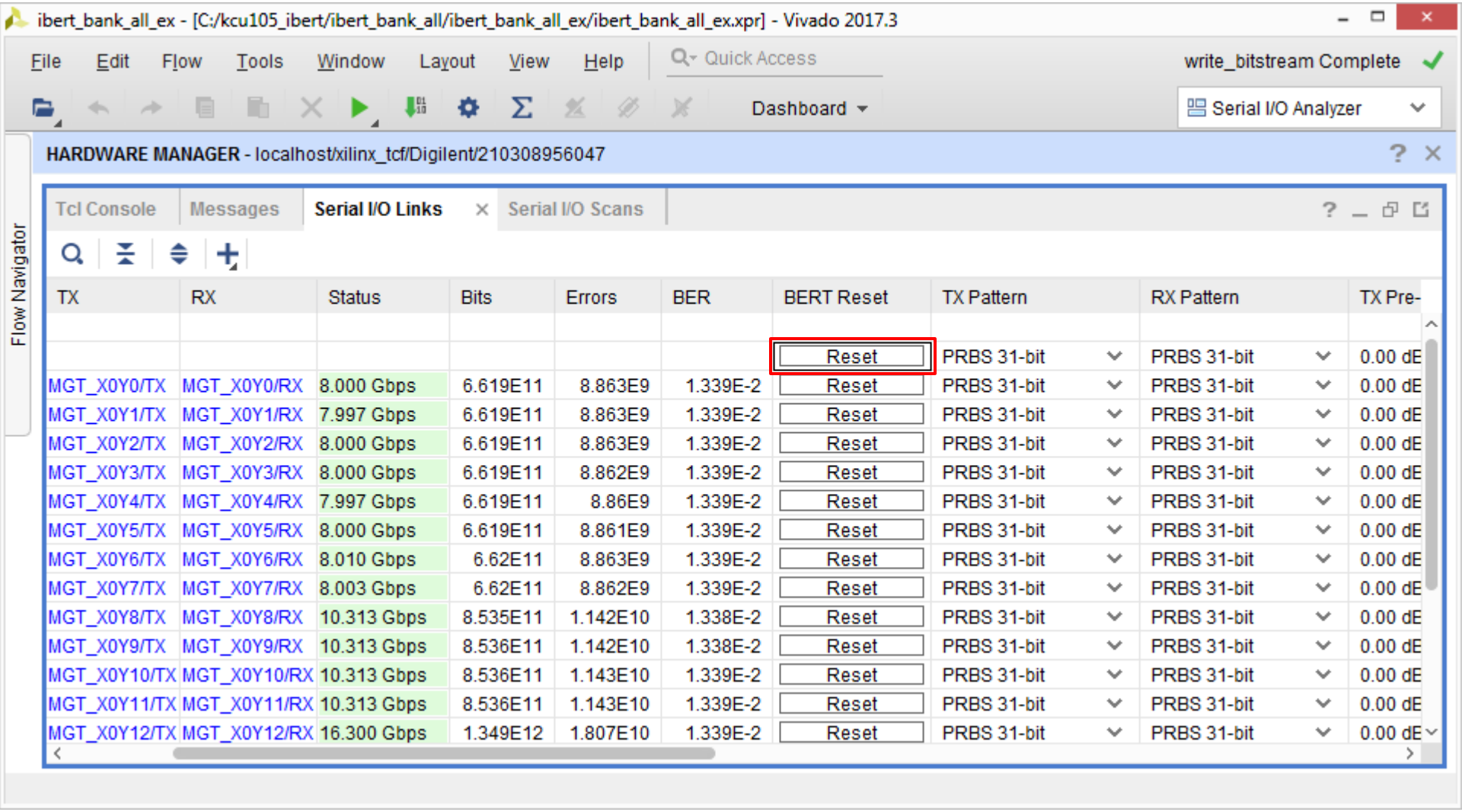


TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-
						Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y0/TX	MGT_X0Y0/RX	7.998 Gbps	4.687E11	8.3E1	1.771E-10	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y1/TX	MGT_X0Y1/RX	8.002 Gbps	4.687E11	9.6E1	2.048E-10	Reset	PRBS 9-bit	PRBS 7-bit	0.00 dE
MGT_X0Y2/TX	MGT_X0Y2/RX	8.000 Gbps	4.687E11	1.06E2	2.262E-10	Reset	PRBS 15-bit	PRBS 7-bit	0.00 dE
MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	4.687E11	8.8E1	1.877E-10	Reset	PRBS 23-bit	PRBS 7-bit	0.00 dE
MGT_X0Y4/TX	MGT_X0Y4/RX	8.000 Gbps	4.687E11	1.11E2	2.368E-10	Reset	PRBS 31-bit	PRBS 7-bit	0.00 dE
MGT_X0Y5/TX	MGT_X0Y5/RX	8.000 Gbps	4.688E11	9.4E1	2.005E-10	Reset	Fast Clk	PRBS 7-bit	0.00 dE
MGT_X0Y6/TX	MGT_X0Y6/RX	8.000 Gbps	4.688E11	9.1E1	1.941E-10	Reset	Slow Clk	PRBS 7-bit	0.00 dE
MGT_X0Y7/TX	MGT_X0Y7/RX	8.000 Gbps	4.688E11	9.4E1	2.005E-10	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y8/TX	MGT_X0Y8/RX	10.313 Gbps	6.043E11	8.6E1	1.423E-10	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y9/TX	MGT_X0Y9/RX	10.313 Gbps	6.044E11	9.5E1	1.572E-10	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y10/TX	MGT_X0Y10/RX	10.308 Gbps	6.044E11	1.07E2	1.77E-10	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y11/TX	MGT_X0Y11/RX	10.313 Gbps	6.044E11	9.2E1	1.522E-10	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y12/TX	MGT_X0Y12/RX	16.300 Gbps	9.553E11	5.684E3	5.95E-9	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE

Note: Presentation applies to the KCU105

Run IBERT Example Design

- Click the BERT Reset button to reset the link error counts

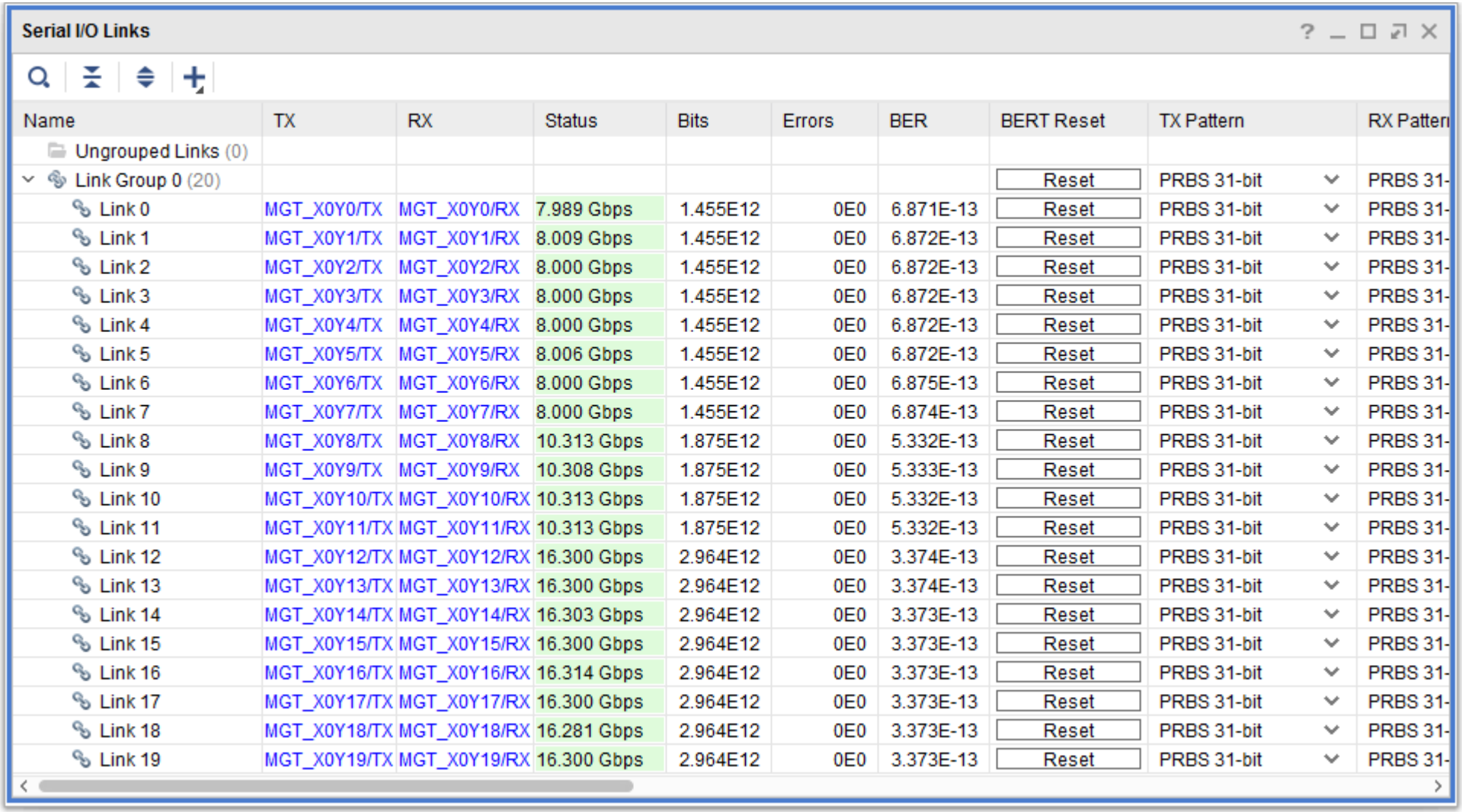


TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-
						Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y0/TX	MGT_X0Y0/RX	8.000 Gbps	6.619E11	8.863E9	1.339E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y1/TX	MGT_X0Y1/RX	7.997 Gbps	6.619E11	8.863E9	1.339E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y2/TX	MGT_X0Y2/RX	8.000 Gbps	6.619E11	8.863E9	1.339E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	6.619E11	8.862E9	1.339E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y4/TX	MGT_X0Y4/RX	7.997 Gbps	6.619E11	8.86E9	1.339E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y5/TX	MGT_X0Y5/RX	8.000 Gbps	6.619E11	8.861E9	1.339E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y6/TX	MGT_X0Y6/RX	8.010 Gbps	6.62E11	8.863E9	1.339E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y7/TX	MGT_X0Y7/RX	8.003 Gbps	6.62E11	8.862E9	1.339E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y8/TX	MGT_X0Y8/RX	10.313 Gbps	8.535E11	1.142E10	1.338E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y9/TX	MGT_X0Y9/RX	10.313 Gbps	8.536E11	1.142E10	1.338E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y10/TX	MGT_X0Y10/RX	10.313 Gbps	8.536E11	1.143E10	1.339E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y11/TX	MGT_X0Y11/RX	10.313 Gbps	8.536E11	1.143E10	1.339E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y12/TX	MGT_X0Y12/RX	16.300 Gbps	1.349E12	1.807E10	1.339E-2	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dE

Note: Presentation applies to the KCU105

Run IBERT Example Design

- All links are showing no errors



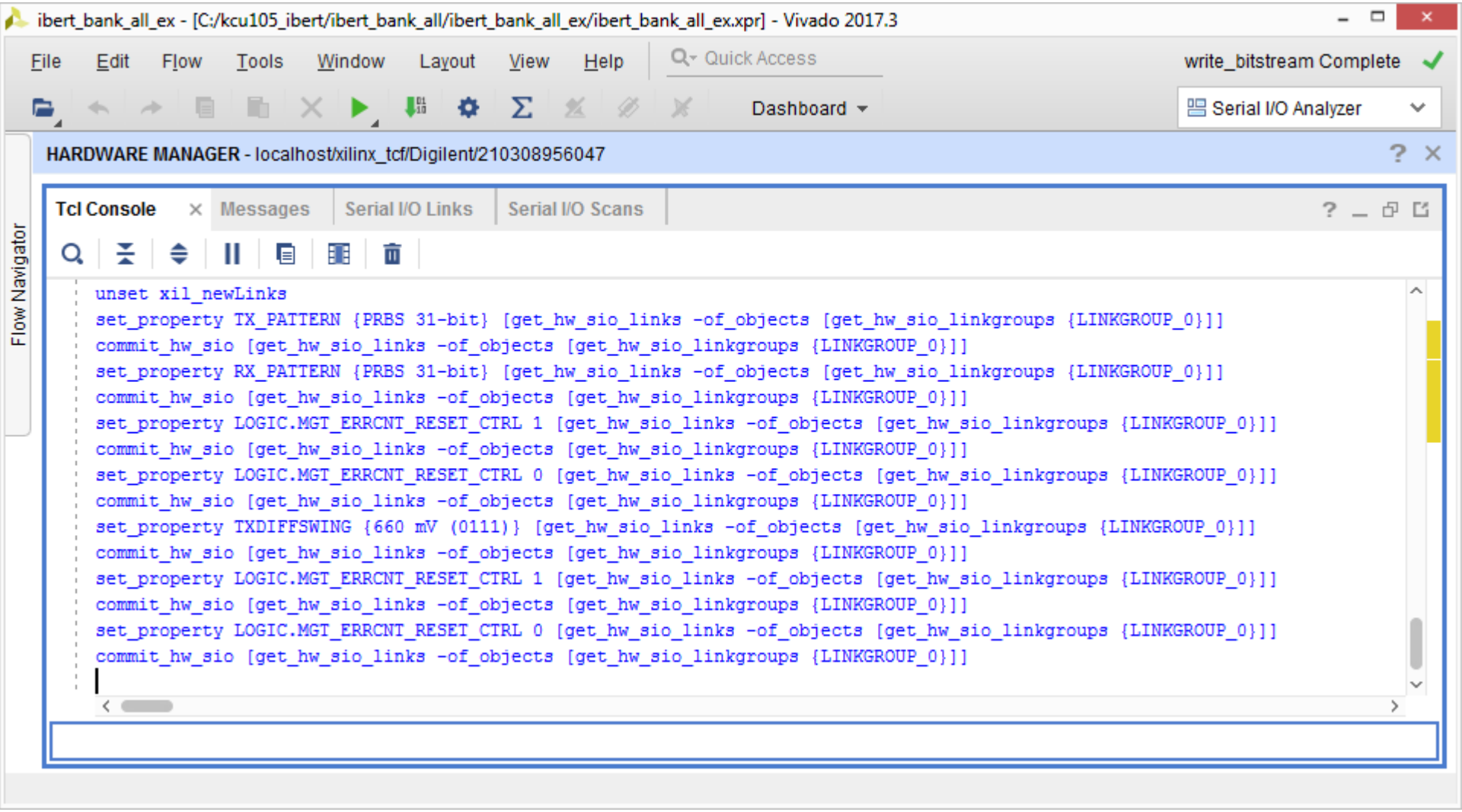
Serial I/O Links

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Patter
Ungrouped Links (0)									
Link Group 0 (20)							Reset	PRBS 31-bit	PRBS 31-
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	7.989 Gbps	1.455E12	0E0	6.871E-13	Reset	PRBS 31-bit	PRBS 31-
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	8.009 Gbps	1.455E12	0E0	6.872E-13	Reset	PRBS 31-bit	PRBS 31-
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	8.000 Gbps	1.455E12	0E0	6.872E-13	Reset	PRBS 31-bit	PRBS 31-
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	1.455E12	0E0	6.872E-13	Reset	PRBS 31-bit	PRBS 31-
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	8.000 Gbps	1.455E12	0E0	6.872E-13	Reset	PRBS 31-bit	PRBS 31-
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	8.006 Gbps	1.455E12	0E0	6.872E-13	Reset	PRBS 31-bit	PRBS 31-
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	8.000 Gbps	1.455E12	0E0	6.875E-13	Reset	PRBS 31-bit	PRBS 31-
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	8.000 Gbps	1.455E12	0E0	6.874E-13	Reset	PRBS 31-bit	PRBS 31-
Link 8	MGT_X0Y8/TX	MGT_X0Y8/RX	10.313 Gbps	1.875E12	0E0	5.332E-13	Reset	PRBS 31-bit	PRBS 31-
Link 9	MGT_X0Y9/TX	MGT_X0Y9/RX	10.308 Gbps	1.875E12	0E0	5.333E-13	Reset	PRBS 31-bit	PRBS 31-
Link 10	MGT_X0Y10/TX	MGT_X0Y10/RX	10.313 Gbps	1.875E12	0E0	5.332E-13	Reset	PRBS 31-bit	PRBS 31-
Link 11	MGT_X0Y11/TX	MGT_X0Y11/RX	10.313 Gbps	1.875E12	0E0	5.332E-13	Reset	PRBS 31-bit	PRBS 31-
Link 12	MGT_X0Y12/TX	MGT_X0Y12/RX	16.300 Gbps	2.964E12	0E0	3.374E-13	Reset	PRBS 31-bit	PRBS 31-
Link 13	MGT_X0Y13/TX	MGT_X0Y13/RX	16.300 Gbps	2.964E12	0E0	3.374E-13	Reset	PRBS 31-bit	PRBS 31-
Link 14	MGT_X0Y14/TX	MGT_X0Y14/RX	16.303 Gbps	2.964E12	0E0	3.373E-13	Reset	PRBS 31-bit	PRBS 31-
Link 15	MGT_X0Y15/TX	MGT_X0Y15/RX	16.300 Gbps	2.964E12	0E0	3.373E-13	Reset	PRBS 31-bit	PRBS 31-
Link 16	MGT_X0Y16/TX	MGT_X0Y16/RX	16.314 Gbps	2.964E12	0E0	3.373E-13	Reset	PRBS 31-bit	PRBS 31-
Link 17	MGT_X0Y17/TX	MGT_X0Y17/RX	16.300 Gbps	2.964E12	0E0	3.373E-13	Reset	PRBS 31-bit	PRBS 31-
Link 18	MGT_X0Y18/TX	MGT_X0Y18/RX	16.281 Gbps	2.964E12	0E0	3.373E-13	Reset	PRBS 31-bit	PRBS 31-
Link 19	MGT_X0Y19/TX	MGT_X0Y19/RX	16.300 Gbps	2.964E12	0E0	3.373E-13	Reset	PRBS 31-bit	PRBS 31-

Note: If FMC HPC shows errors, set TXDIFFSWING to 660 mV

Run IBERT Example Design

- Tcl console commands can be saved as TCL file for later playback



Note: Presentation applies to the KCU105

References

References

- IBERT IP
  - LogiCORE IP Integrated Bit Error Ratio Tester for UltraScale GTH – PG173
    - https://www.xilinx.com/support/documentation/ip_documentation/ibert_ultrascale_gth/v1_3/pg173-ibert-ultrascale-gth.pdf
- Vivado Release Notes
  - Vivado Design Suite User Guide - Release Notes – UG973
    - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_3/ug973-vivado-release-notes-install-license.pdf
  - Vivado Design Suite 2017 - Vivado Known Issues
    - https://www.xilinx.com/support/answers/68923.html
- Vivado Programming and Debugging
  - Vivado Design Suite Programming and Debugging User Guide – UG908
    - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_3/ug908-vivado-programming-debugging.pdf

Documentation

Documentation

- Kintex UltraScale
  - Kintex UltraScale FPGA Family
    - https://www.xilinx.com/products/silicon-devices/fpga/kintex-ultrascale.html
- KCU105 Documentation
  - Kintex UltraScale FPGA KCU105 Evaluation Kit
    - https://www.xilinx.com/products/boards-and-kits/kcu105.html
  - KCU105 Board User Guide – UG917
    - https://www.xilinx.com/support/documentation/boards_and_kits/kcu105/ug917-kcu105-eval-bd.pdf
  - KCU105 Evaluation Kit Quick Start Guide User Guide – XTP391
    - https://www.xilinx.com/support/documentation/boards_and_kits/kcu105/xtp391-kcu105-quickstart.pdf
  - KCU105 - Known Issues Master Answer Record
    - https://www.xilinx.com/support/answers/63175.html