

ALL PROGRAMMABLE

ANY MEDIA

5G

4K/8K

ANY STANDARD

ANY MACHINE

ANY NETWORK

5G Wireless • Embedded Vision • Industrial IoT • Cloud Computing



KCU105 GTH IBERT Design Creation

October 2017

Revision History

Date	Version	Description
10/09/17	12.0	Updated for 2017.3.
06/20/17	11.0	Updated for 2017.2.
04/19/17	10.0	Updated for 2017.1.
12/19/16	9.0	Updated for 2016.4.
10/13/16	8.0	Updated for 2016.3.
06/08/16	7.0	Updated for 2016.2.
04/13/16	6.0	Updated for 2016.1
11/24/15	5.0	Updated for 2015.4.
10/06/15	4.0	Updated for 2015.3.
06/30/15	3.0	Updated for 2015.2.
04/30/15	2.0	Updated for 2015.1.
03/06/15	1.0	Initial version. Added AR63771.

© Copyright 2017 Xilinx, Inc. Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

NOTICE OF DISCLAIMER: The information disclosed to you hereunder (the "Information") is provided "AS-IS" with no warranty of any kind, express or implied. Xilinx does not assume any liability arising from your use of the Information. You are responsible for obtaining any rights you may require for your use of this Information. Xilinx reserves the right to make changes, at any time, to the Information without notice and at its sole discretion. Xilinx assumes no obligation to correct any errors contained in the Information or to advise you of any corrections or updates. Xilinx expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE INFORMATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS.

KCU105 IBERT Overview

- Xilinx KCU105 Board
- KCU105 Software Install and Board Setup
- Setup for the KCU105 IBERT Design
- IBERT Testing
 - FMC HPC (Bank 227 & 228)
 - FMC LPC (Bank 226)
 - SFP (Bank 226)
 - PCIe (Bank 224 & 225)
- Create IBERT Design for All Banks
 - Testing All Banks with Optional User Provided Hardware
- References

KCU105 IBERT Overview

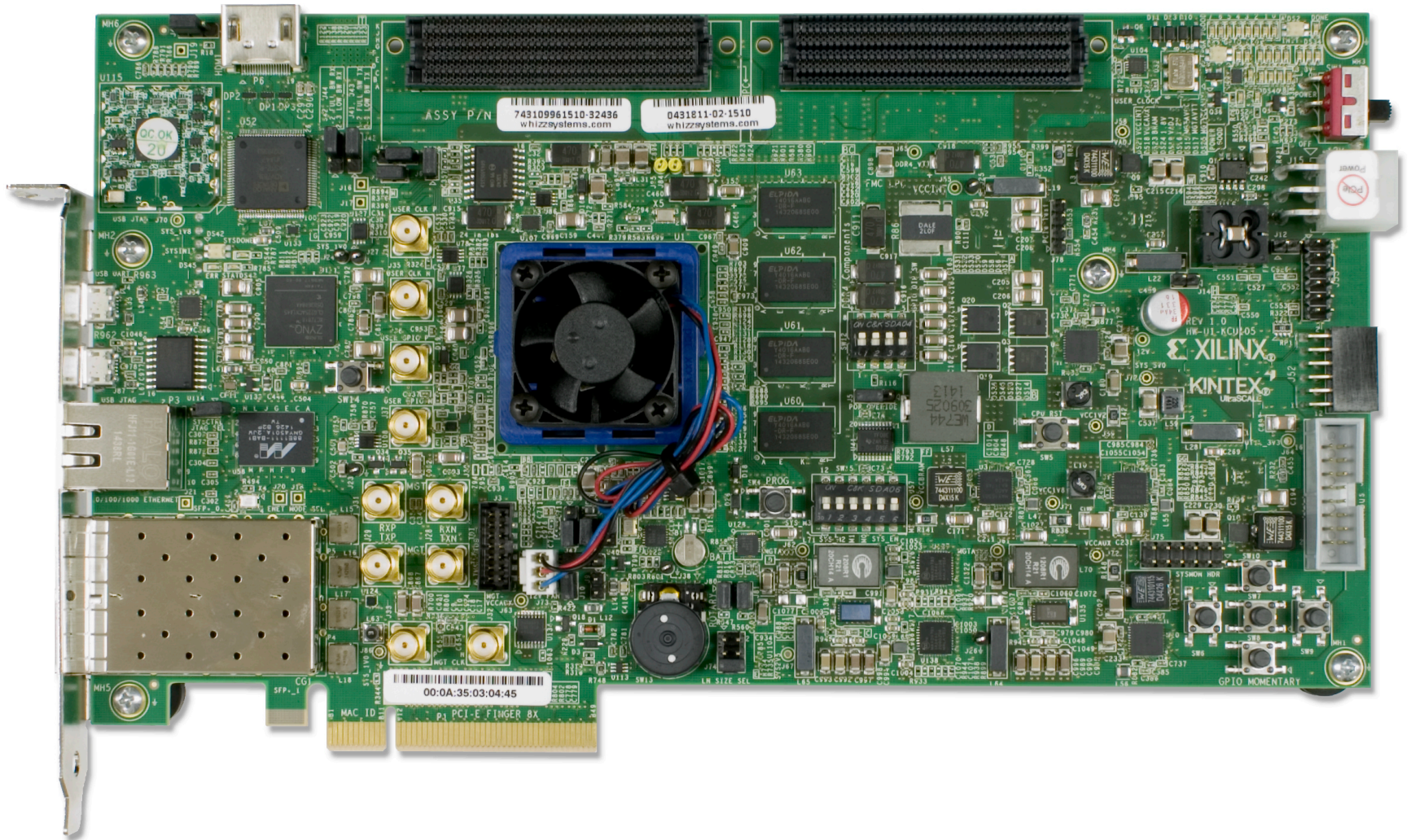
➤ Description

- The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the UltraScale Kintex GTH transceivers. A graphical user interface is provided through the Vivado Hardware Manager.

➤ Reference Design IP

- LogiCORE UltraScale IBERT GTH Example Designs

Xilinx KCU105 Board



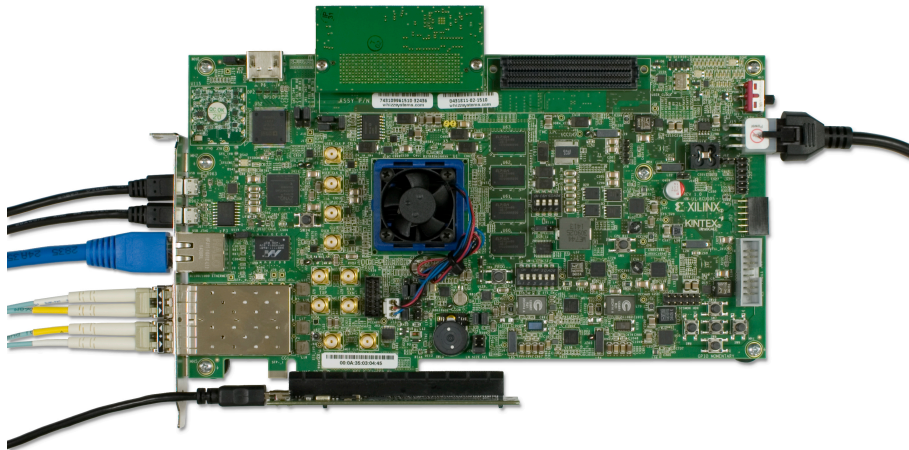
Note: Presentation applies to the KCU105

XILINX ALL PROGRAMMABLE

KCU105 Software Install and Board Setup

➤ Refer to XTP352 – KCU105 Software Install and Board Setup for details on:

- Software Requirements
- KCU105 Board Setup
- Clock Setup
- Optional Hardware Setup

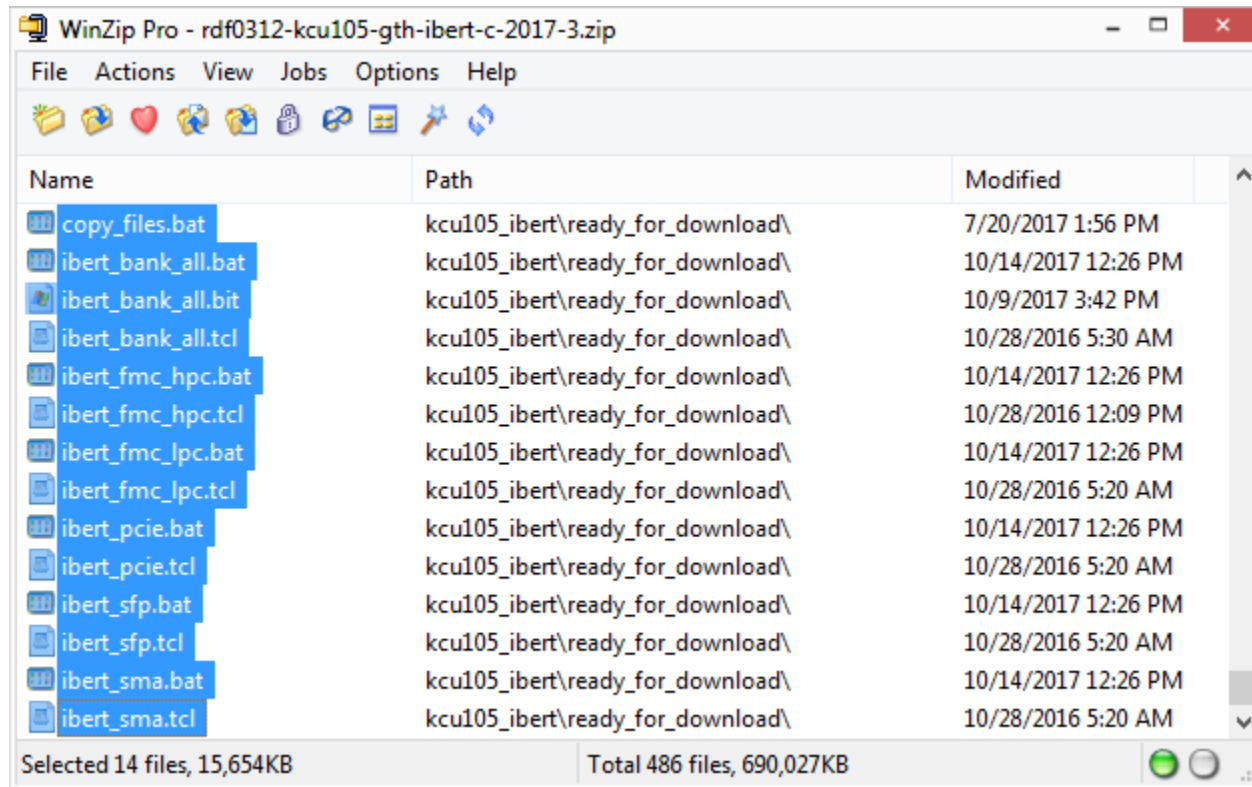


Note: The Clock Setup is required for this tutorial

Setup for the KCU105 IBERT Design

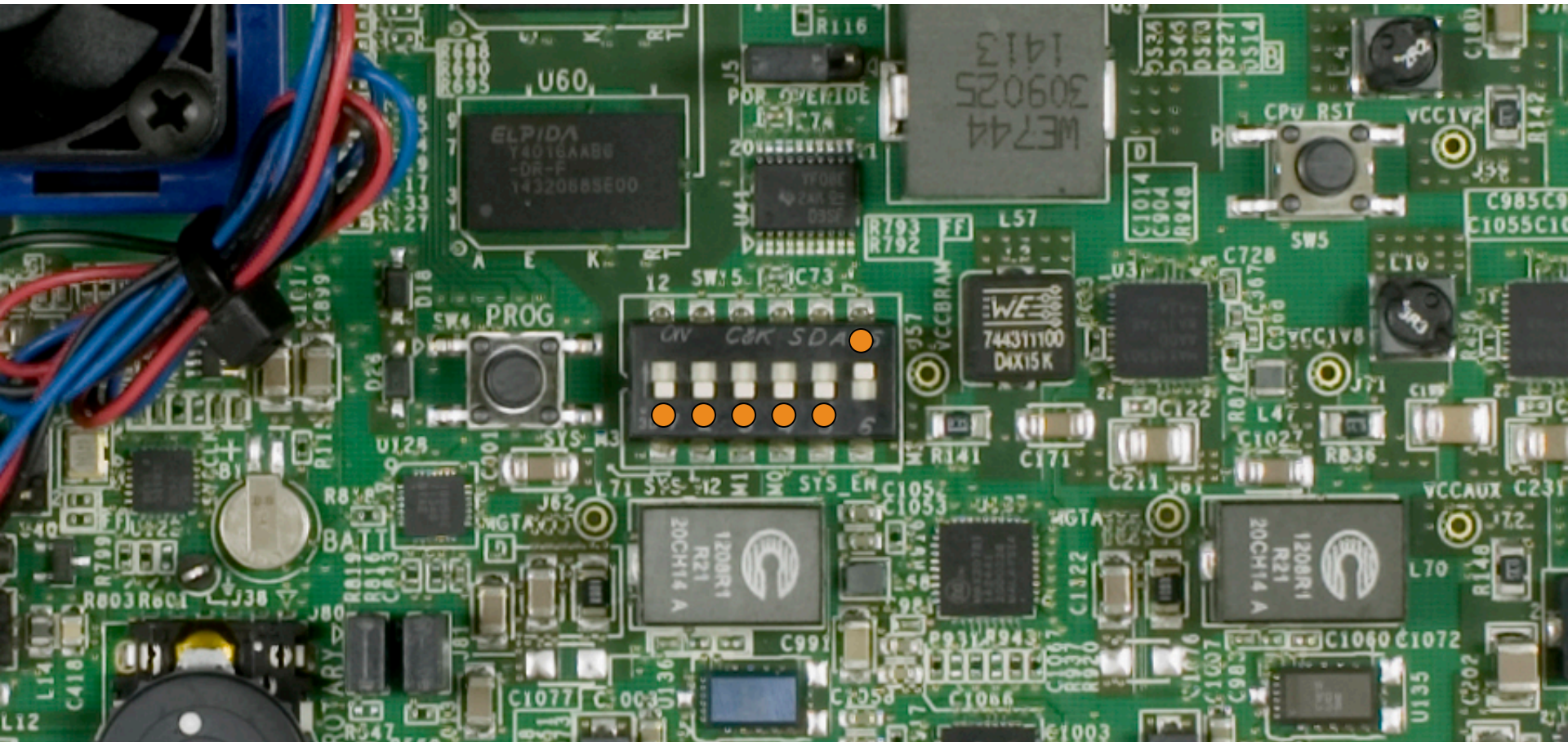
Setup for the KCU105 IBERT Design

- Open the RDF0312 - KCU105 GTH IBERT Design Files (2017.3 C) ZIP file, and extract these files to your C:\ drive:
 - kcu105_ibert\ready_for_download*



Setup for the KCU105 IBERT Design

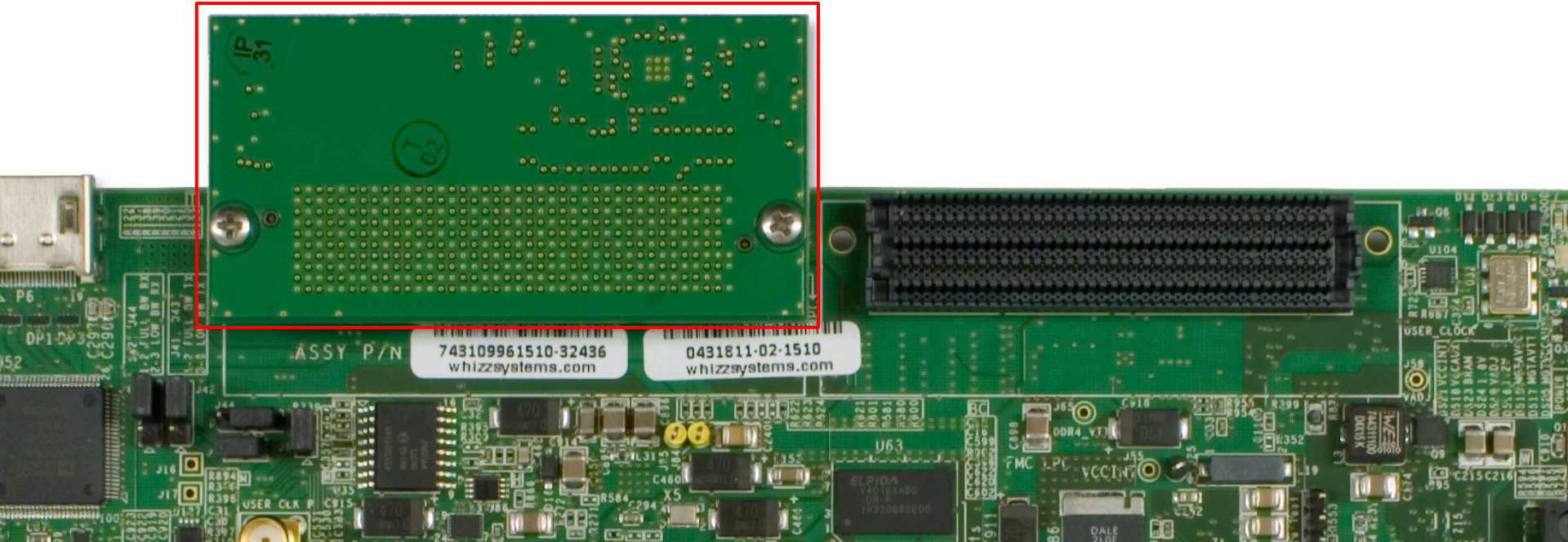
- Set SW15 to 000001 (1 = on, Position 1 → Position 6)
 - This enables JTAG configuration



Testing FMC HPC IBERT

Testing FMC HPC IBERT

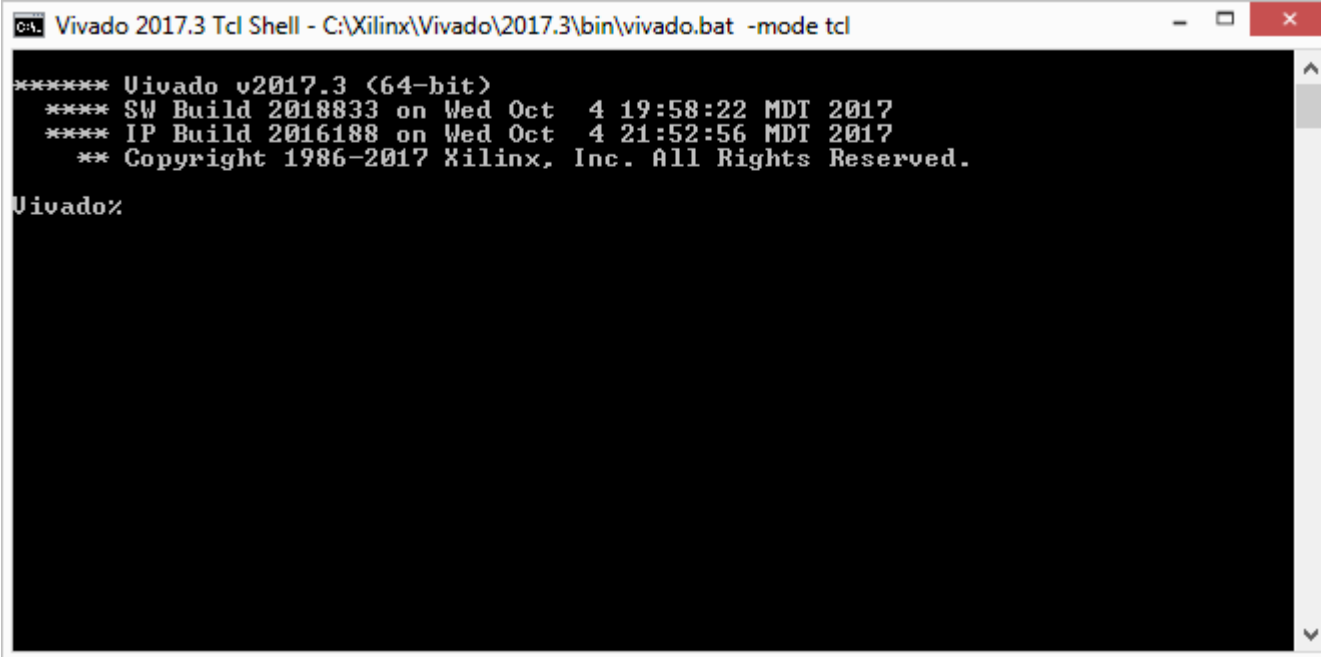
- As noted in the Setup Guide, XTP352, attach the FMC XM107 board to the FMC HPC connector



Testing FMC HPC IBERT

➤ Open a Vivado Tcl Shell:

Start → All Programs → Xilinx Design Tools → Vivado 2017.3 → Vivado 2017.3 Tcl Shell



```
C:\> Vivado 2017.3 Tcl Shell - C:\Xilinx\Vivado\2017.3\bin\vivado.bat -mode tcl

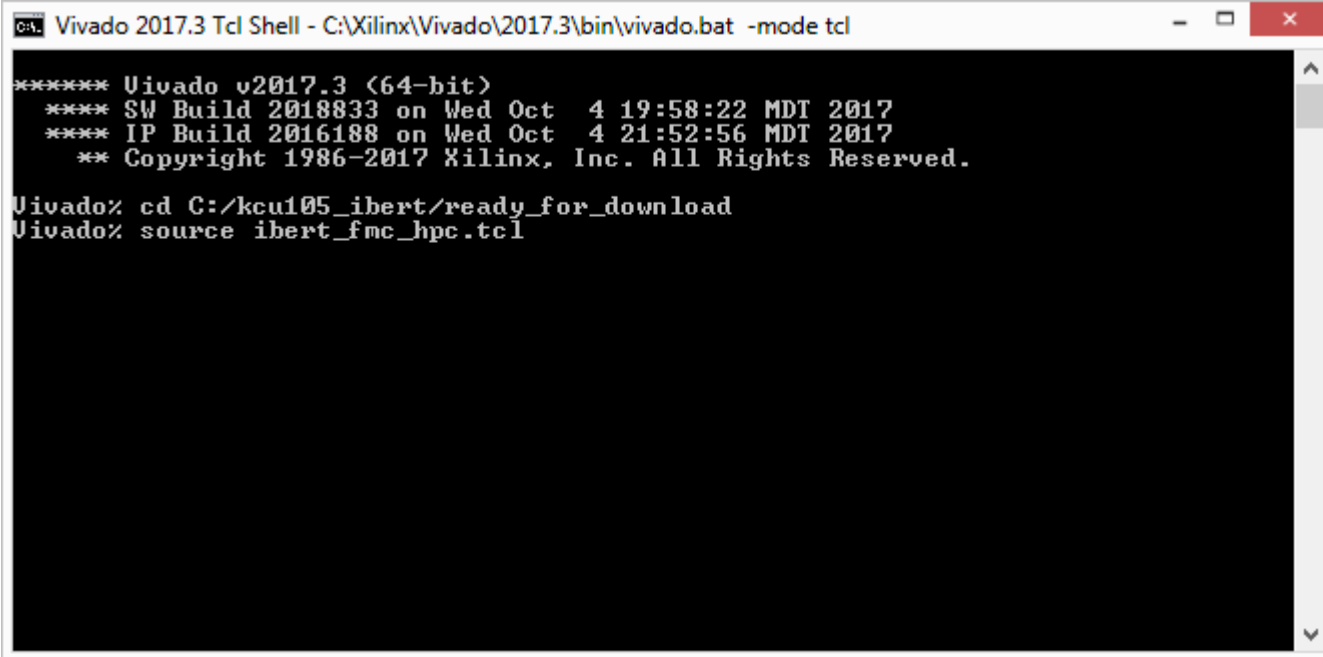
***** Vivado v2017.3 (64-bit)
***** SW Build 2018833 on Wed Oct  4 19:58:22 MDT 2017
***** IP Build 2016188 on Wed Oct  4 21:52:56 MDT 2017
***** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

Vivado%
```

Testing FMC HPC IBERT

➤ In a Vivado Tcl Shell type:

```
cd C:/kcu105_ibert/ready_for_download  
source ibert_fmc_hpc.tcl
```



```
C:\Xilinx\Vivado\2017.3\bin\vivado.bat -mode tcl  
***** Vivado v2017.3 (64-bit)  
***** SW Build 2018833 on Wed Oct  4 19:58:22 MDT 2017  
***** IP Build 2016188 on Wed Oct  4 21:52:56 MDT 2017  
***** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.  
  
Vivado% cd C:/kcu105_ibert/ready_for_download  
Vivado% source ibert_fmc_hpc.tcl
```

Testing FMC HPC IBERT

➤ If needed, set Vivado GUI layout to Serial I/O Analyzer

The screenshot displays the Vivado 2017.3 software interface. The top menu bar includes File, Edit, Tools, Window, Layout, View, and Help. A search bar for 'Quick Access' is present. Below the menu bar is a toolbar with various icons. The main workspace is titled 'HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210308956047'. On the left, there are panels for 'Hardware' and 'Properties'. A dropdown menu is open, showing layout options: 'Default Layout', 'Logic Analyzer', 'Serial I/O Analyzer' (which is highlighted), 'Save As New Layout...', and 'Reset Layout' (with a keyboard shortcut 'F5'). At the bottom, the 'Tcl Console' is active, showing a series of commands:

```
# commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
# set_property LOGIC.MGT_ERRCNT_RESET_CTRL 1 [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
# commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
# set_property LOGIC.MGT_ERRCNT_RESET_CTRL 0 [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
# commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
```

Testing FMC HPC IBERT

- FMC HPC line rate is 16.3 Gbps
- Close Vivado GUI after finished viewing

Vivado 2017.3

File Edit Tools Window Layout View Help | Quick Access

Dashboard | Default Layout

HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210308956047

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

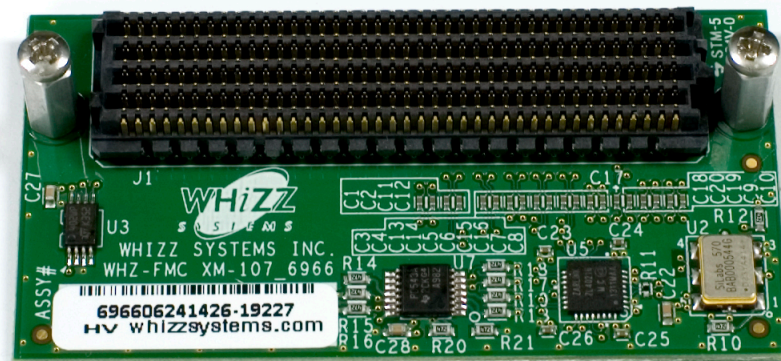
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
FMC HPC (8)									
Link 0	MGT_X0Y12/TX	MGT_X0Y12/RX	16.300 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 1	MGT_X0Y13/TX	MGT_X0Y13/RX	16.278 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 2	MGT_X0Y14/TX	MGT_X0Y14/RX	16.300 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 3	MGT_X0Y15/TX	MGT_X0Y15/RX	16.269 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 4	MGT_X0Y16/TX	MGT_X0Y16/RX	16.300 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 5	MGT_X0Y17/TX	MGT_X0Y17/RX	16.300 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 6	MGT_X0Y18/TX	MGT_X0Y18/RX	16.321 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 7	MGT_X0Y19/TX	MGT_X0Y19/RX	16.300 Gbps	3.748E12	0E0	2.668E-13	Reset	PRBS 31-bit	PRBS 31-bit

Note: User Si570 should be set to 163 MHz as per XTP352

Testing FMC LPC IBERT

Testing FMC LPC IBERT

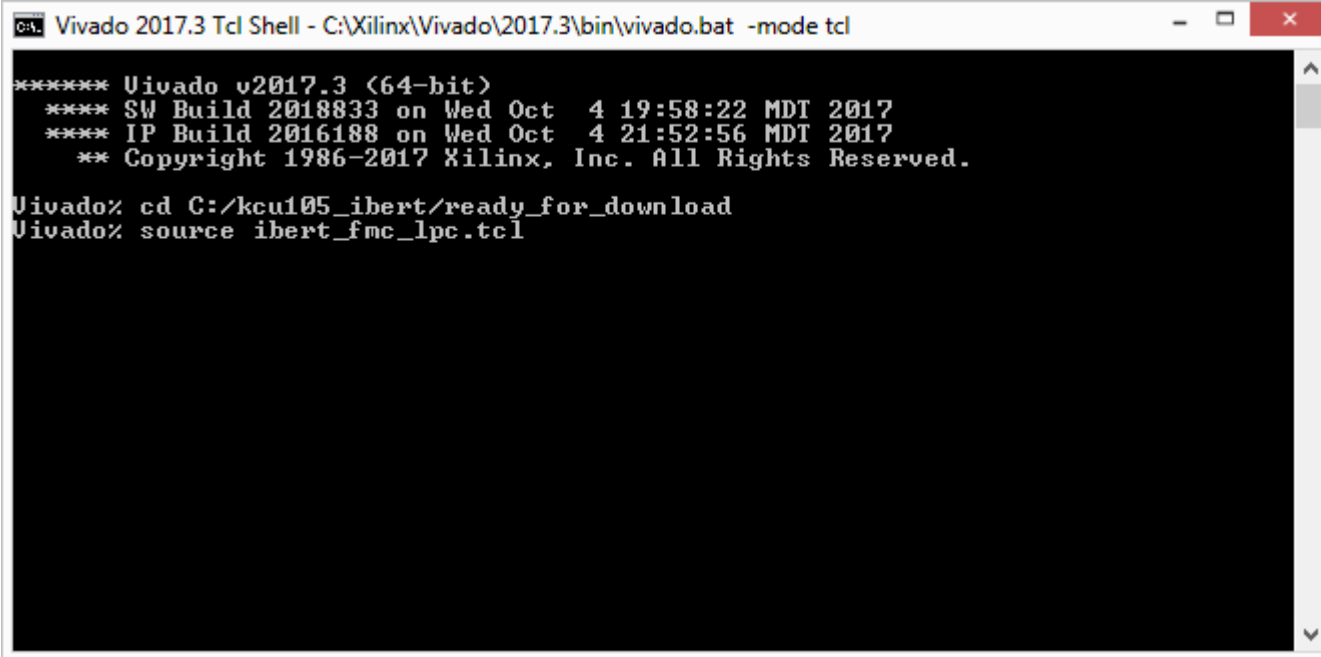
- Move the FMC XM107 board to the FMC LPC connector



Testing FMC LPC IBERT

➤ In a Vivado Tcl Shell type:

```
cd C:/kcu105_ibert/ready_for_download  
source ibert_fmc_lpc.tcl
```



```
C:\ Vivado 2017.3 Tcl Shell - C:\Xilinx\Vivado\2017.3\bin\vivado.bat -mode tcl  
***** Vivado v2017.3 (64-bit)  
**** SW Build 2018833 on Wed Oct  4 19:58:22 MDT 2017  
**** IP Build 2016188 on Wed Oct  4 21:52:56 MDT 2017  
** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.  
  
Vivado% cd C:/kcu105_ibert/ready_for_download  
Vivado% source ibert_fmc_lpc.tcl
```

Testing FMC LPC IBERT

- FMC LPC line rate is 10.3125 Gbps
- Close Vivado GUI after finished viewing

Vivado 2017.3

File Edit Tools Window Layout View Help | Quick Access

Dashboard ▾ Default Layout ▾

HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210308956047

Tcl Console Messages **Serial I/O Links** x Serial I/O Scans

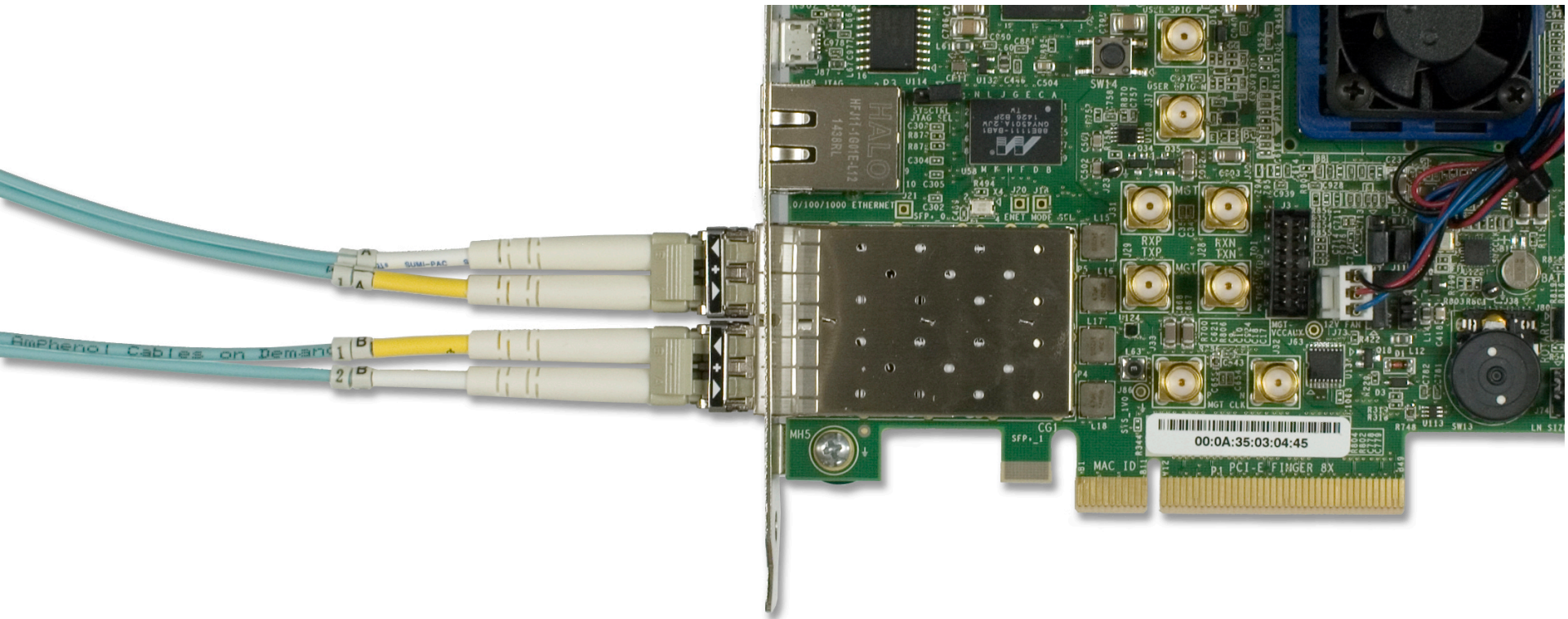
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
▼ FMC LPC (1)							<input type="button" value="Reset"/>	PRBS 31-bit ▾	PRBS 31-bit
Link 0	MGT_X0Y8/TX	MGT_X0Y8/RX	10.308 Gbps	1.218E12	0E0	8.21E-13	<input type="button" value="Reset"/>	PRBS 31-bit ▾	PRBS 31-bit

Note: Presentation applies to the KCU105

Testing SFP IBERT

Testing SFP IBERT

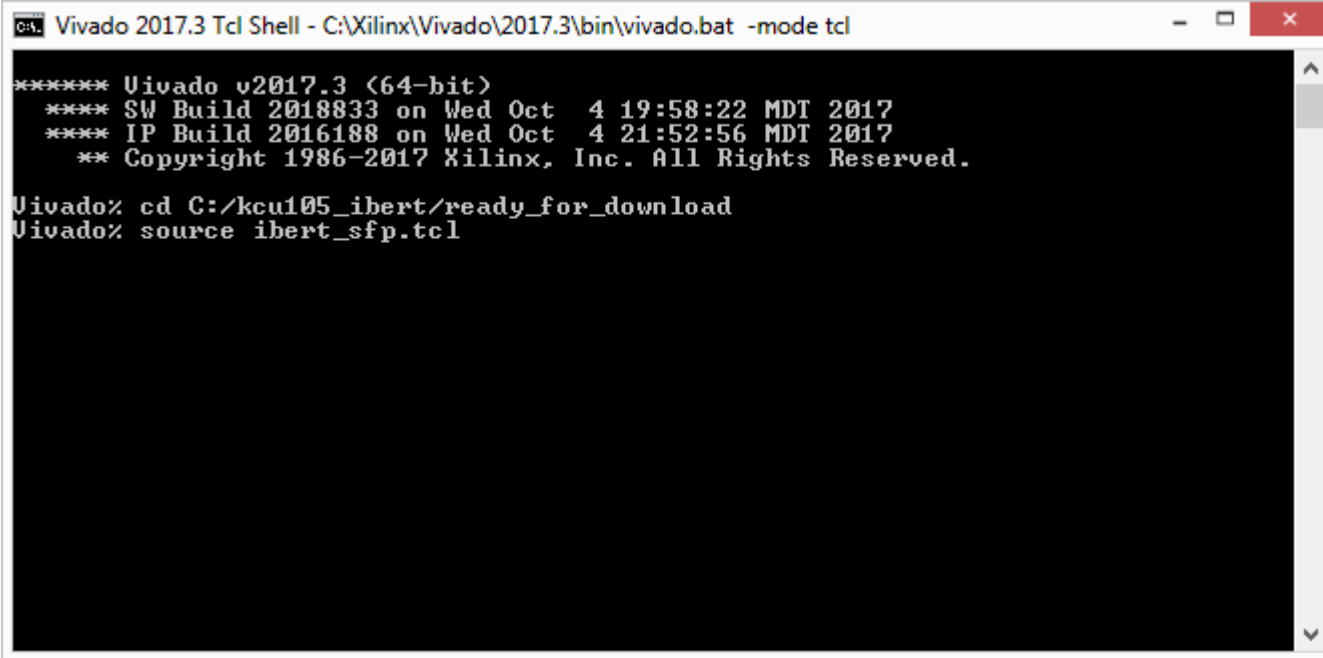
- As noted in the Setup Guide, XTP352, The Optical modules and Fiber optic cable should be attached for this test



Testing SFP IBERT

➤ In the Vivado Tcl Shell type:

```
cd C:/kcu105_ibert/ready_for_download
source ibert_sfp.tcl
```



```
C:\ Vivado 2017.3 Tcl Shell - C:\Xilinx\Vivado\2017.3\bin\vivado.bat -mode tcl

***** Vivado v2017.3 (64-bit)
**** SW Build 2018833 on Wed Oct  4 19:58:22 MDT 2017
**** IP Build 2016188 on Wed Oct  4 21:52:56 MDT 2017
** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

Vivado% cd C:/kcu105_ibert/ready_for_download
Vivado% source ibert_sfp.tcl
```

Testing SFP IBERT

- SFP line rate is 10.3125 Gbps
- Close Vivado GUI after finished viewing

The screenshot shows the Vivado 2017.3 Hardware Manager interface. The 'Serial I/O Links' tab is active, displaying a table of SFP links. The table has columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, and RX Pattern. Two links are listed: Link 0 and Link 1, both showing a line rate of 10.313 Gbps. Each link has a 'Reset' button next to the BERT Reset column.

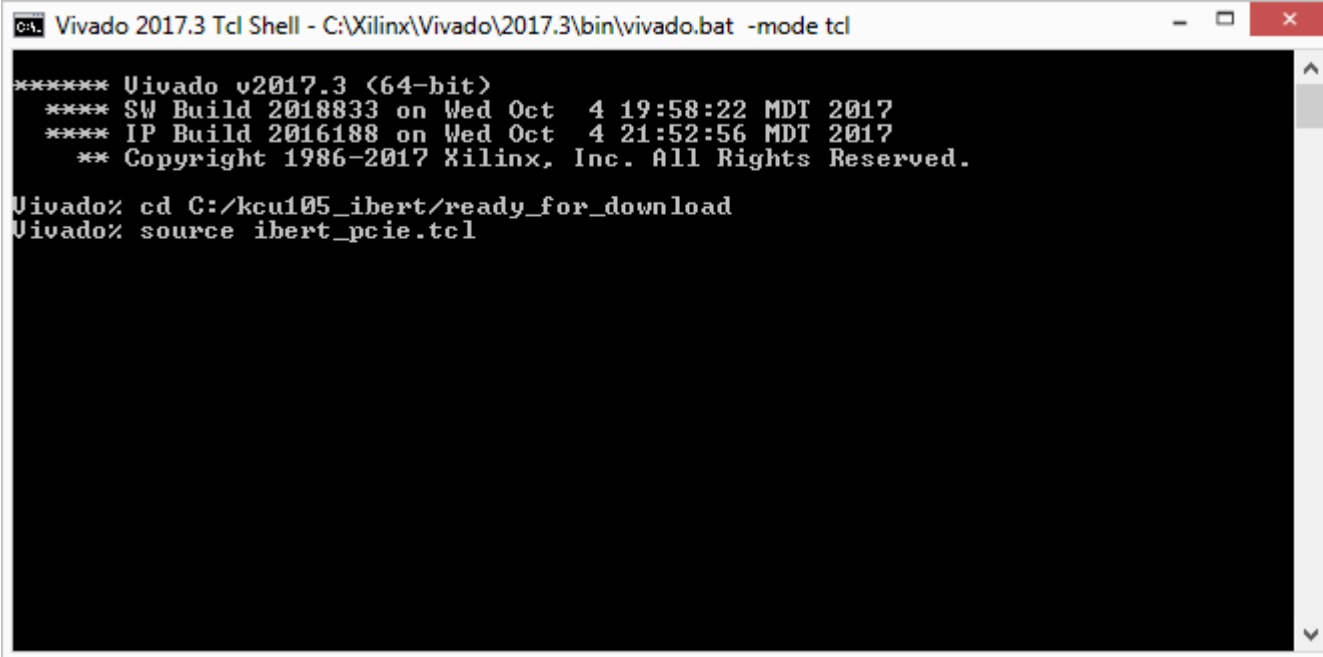
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
SFP (2)							Reset	PRBS 31-bit	PRBS 31-bit
Link 0	MGT_X0Y9/TX	MGT_X0Y9/RX	10.313 Gbps	4.067E12	0E0	2.459E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 1	MGT_X0Y10/TX	MGT_X0Y10/RX	10.313 Gbps	4.067E12	0E0	2.459E-13	Reset	PRBS 31-bit	PRBS 31-bit

Testing PCIe IBERT

Testing PCIe IBERT

➤ In a Vivado Tcl Shell type:

```
cd C:/kcu105_ibert/ready_for_download
source ibert_pcie.tcl
```



```
C:\ Vivado 2017.3 Tcl Shell - C:\Xilinx\Vivado\2017.3\bin\vivado.bat -mode tcl

***** Vivado v2017.3 (64-bit)
***** SW Build 2018833 on Wed Oct  4 19:58:22 MDT 2017
***** IP Build 2016188 on Wed Oct  4 21:52:56 MDT 2017
***** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

Vivado% cd C:/kcu105_ibert/ready_for_download
Vivado% source ibert_pcie.tcl
```

Testing PCIe IBERT

- PCIe line rate is 8 Gbps
- Close Vivado GUI after finished viewing

The screenshot shows the Vivado 2017.3 Hardware Manager interface. The main window displays the 'Serial I/O Links' tab, which contains a table of PCIe links. The table has columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, and RX Pattern. There are 8 links listed, all with a status of 8.000 Gbps and 0E0 errors. Each link has a 'Reset' button in the BERT Reset column. The TX and RX patterns are all PRBS 31-bit.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
PCIe (8)									
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	8.000 Gbps	1.156E12	0E0	8.652E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	8.004 Gbps	1.156E12	0E0	8.652E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	8.003 Gbps	1.156E12	0E0	8.652E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	1.156E12	0E0	8.651E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	8.000 Gbps	1.156E12	0E0	8.651E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	8.000 Gbps	1.156E12	0E0	8.651E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	8.003 Gbps	1.156E12	0E0	8.651E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	8.000 Gbps	1.156E12	0E0	8.651E-13	Reset	PRBS 31-bit	PRBS 31-bit

Note: Presentation applies to the KCU105

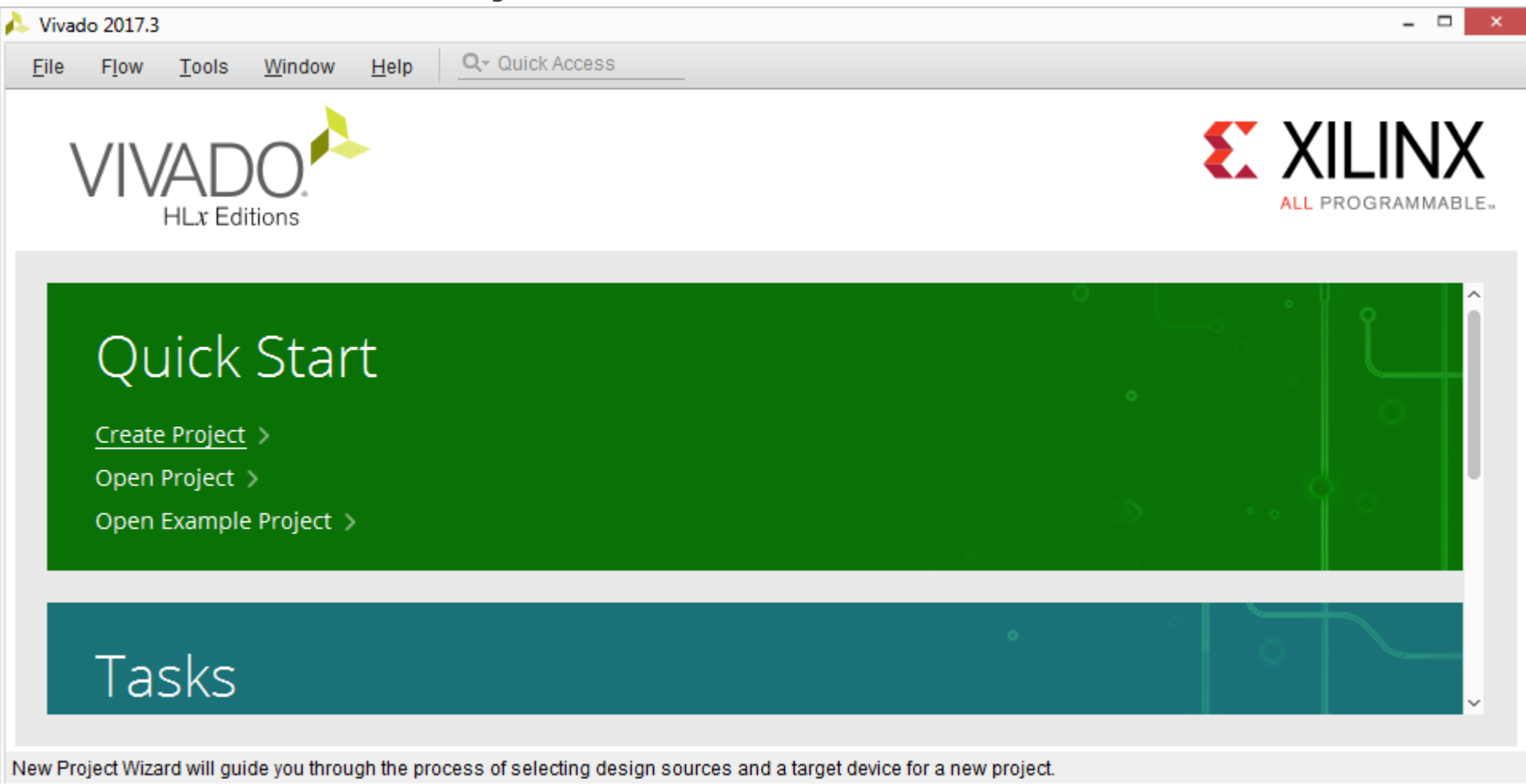
Create IBERT Design for All Banks

Create IBERT Design for All Banks

➤ Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2017.3 → Vivado

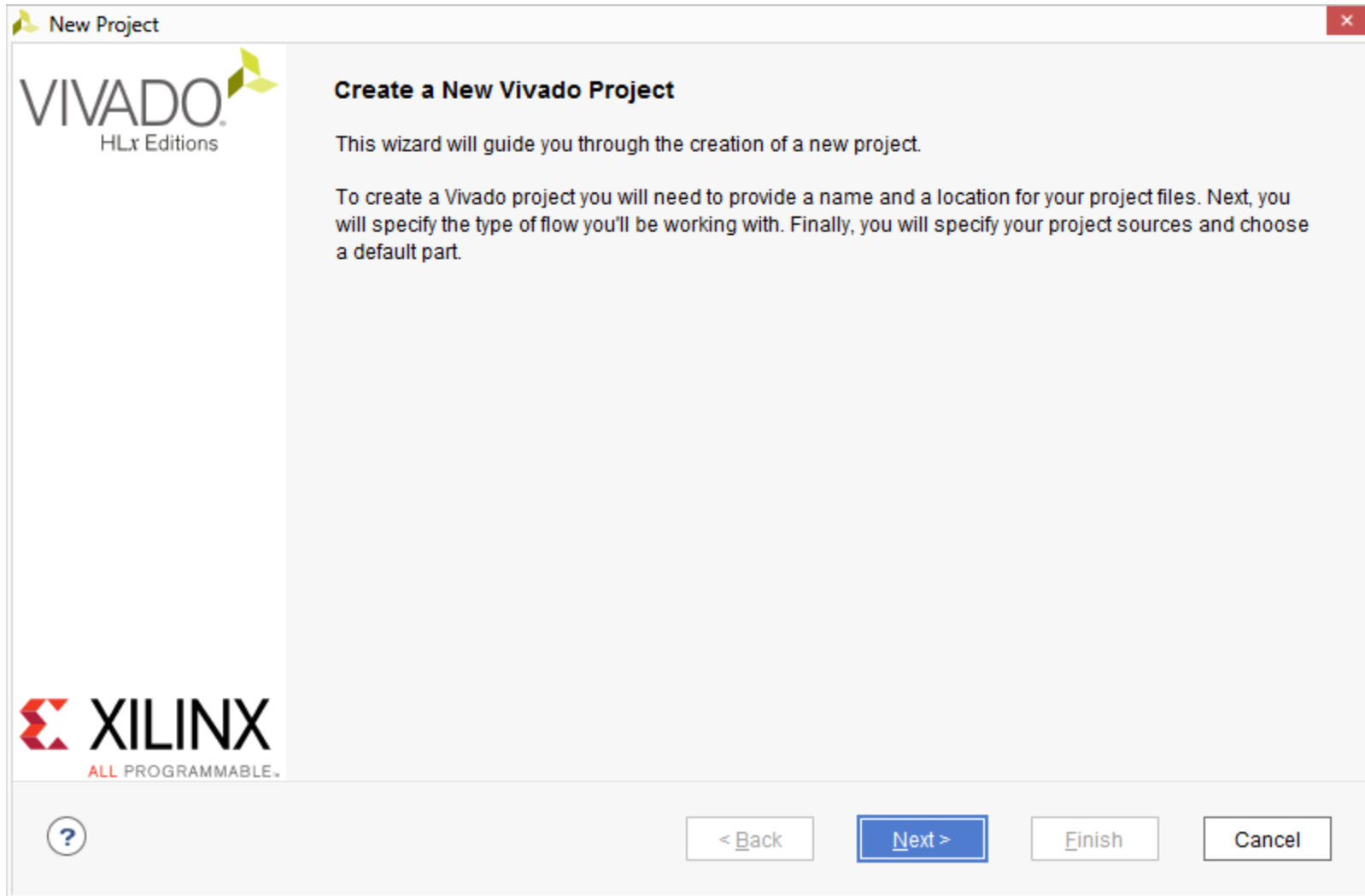
➤ **Select Create Project**



Note: Presentation applies to the KCU105

Create IBERT Design for All Banks

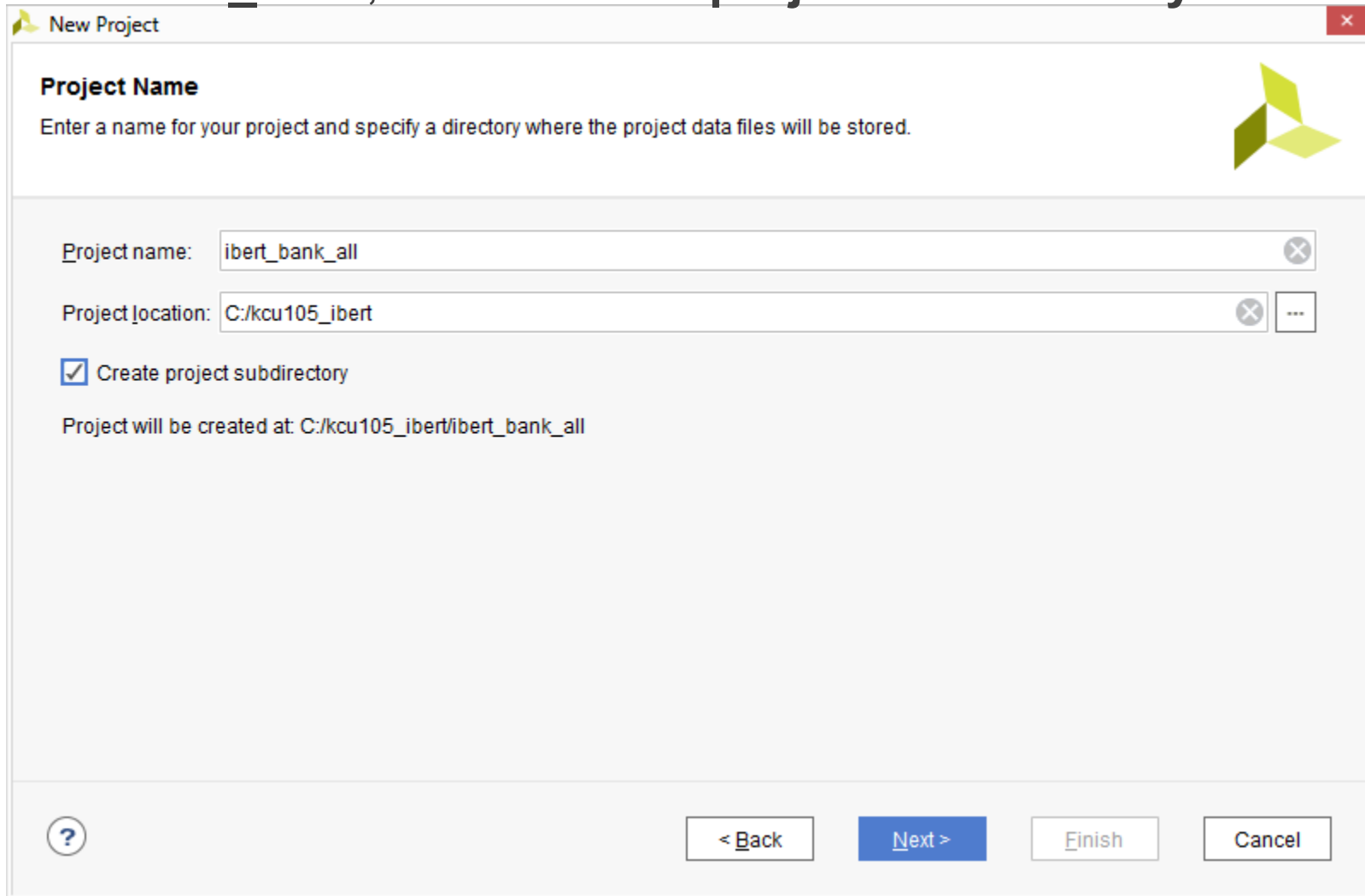
➤ Click **Next**



Note: Presentation applies to the KCU105

Create IBERT Design for All Banks

- Set the Project name and location to **ibert_bank_all** and **C:/kcu105_ibert**; check **Create project subdirectory**



New Project

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

Create project subdirectory

Project will be created at: C:/kcu105_ibert/ibert_bank_all

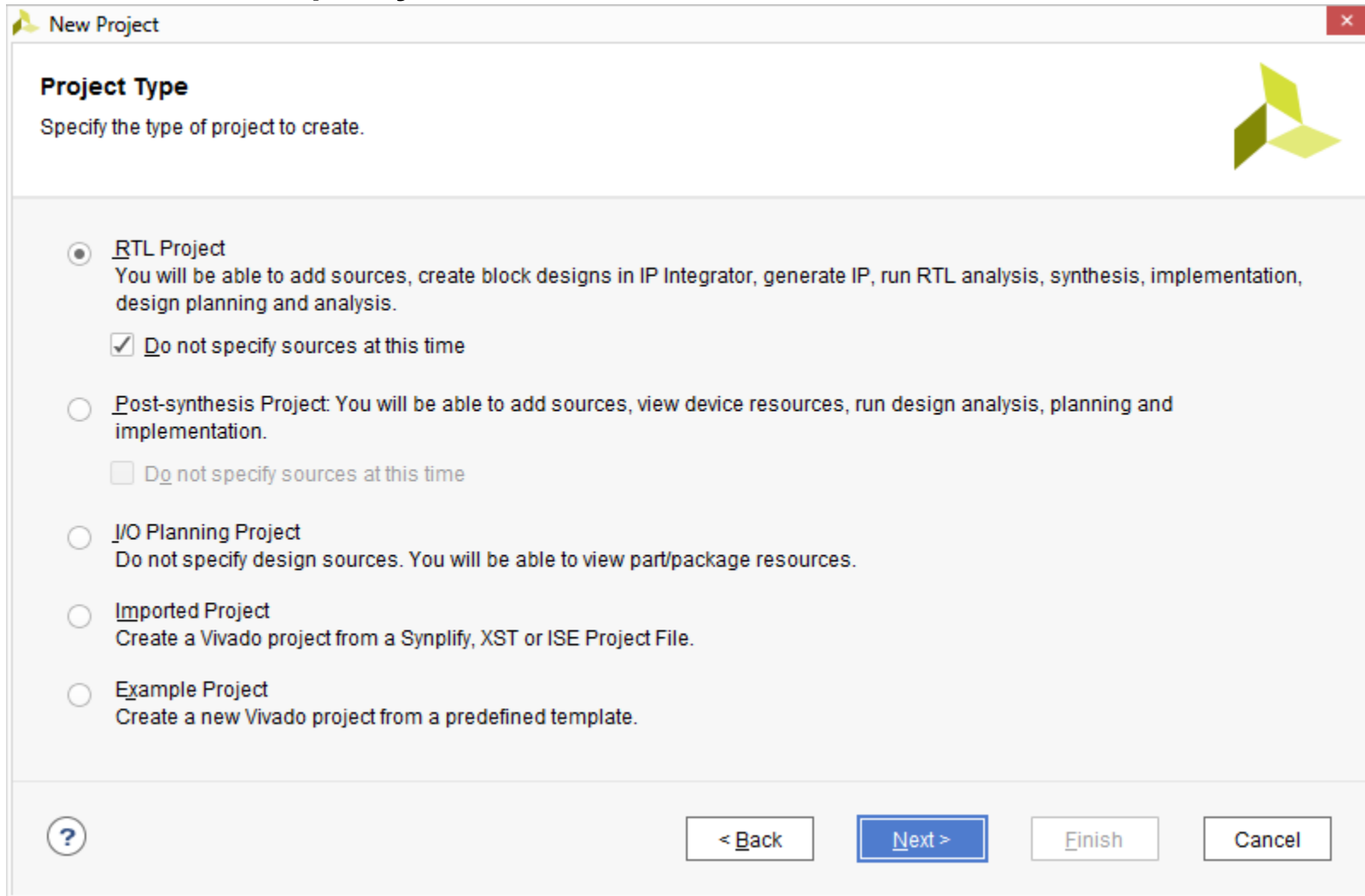
? < Back Next > Finish Cancel

Note: Vivado generally requires forward slashes in paths

Create IBERT Design for All Banks

➤ Select RTL Project

– Select **Do not specify sources at this time**



New Project

Project Type
Specify the type of project to create.

- RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
 Do not specify sources at this time
- Post-synthesis Project**. You will be able to add sources, view device resources, run design analysis, planning and implementation.
 Do not specify sources at this time
- I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.
- Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.
- Example Project**
Create a new Vivado project from a predefined template.

? < Back Next > Finish Cancel

Create IBERT Design for All Banks

➤ Under Boards, select the **KCU105 Evaluation Platform**

New Project ✕

Default Part
Choose a default Xilinx part or board for your project. This can be changed later.

Select: Parts Boards







Filter/Preview

Vendor: All

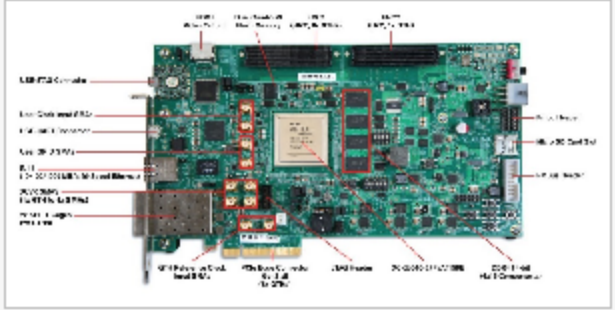
Display Name: All

Board Rev: Latest

Search:

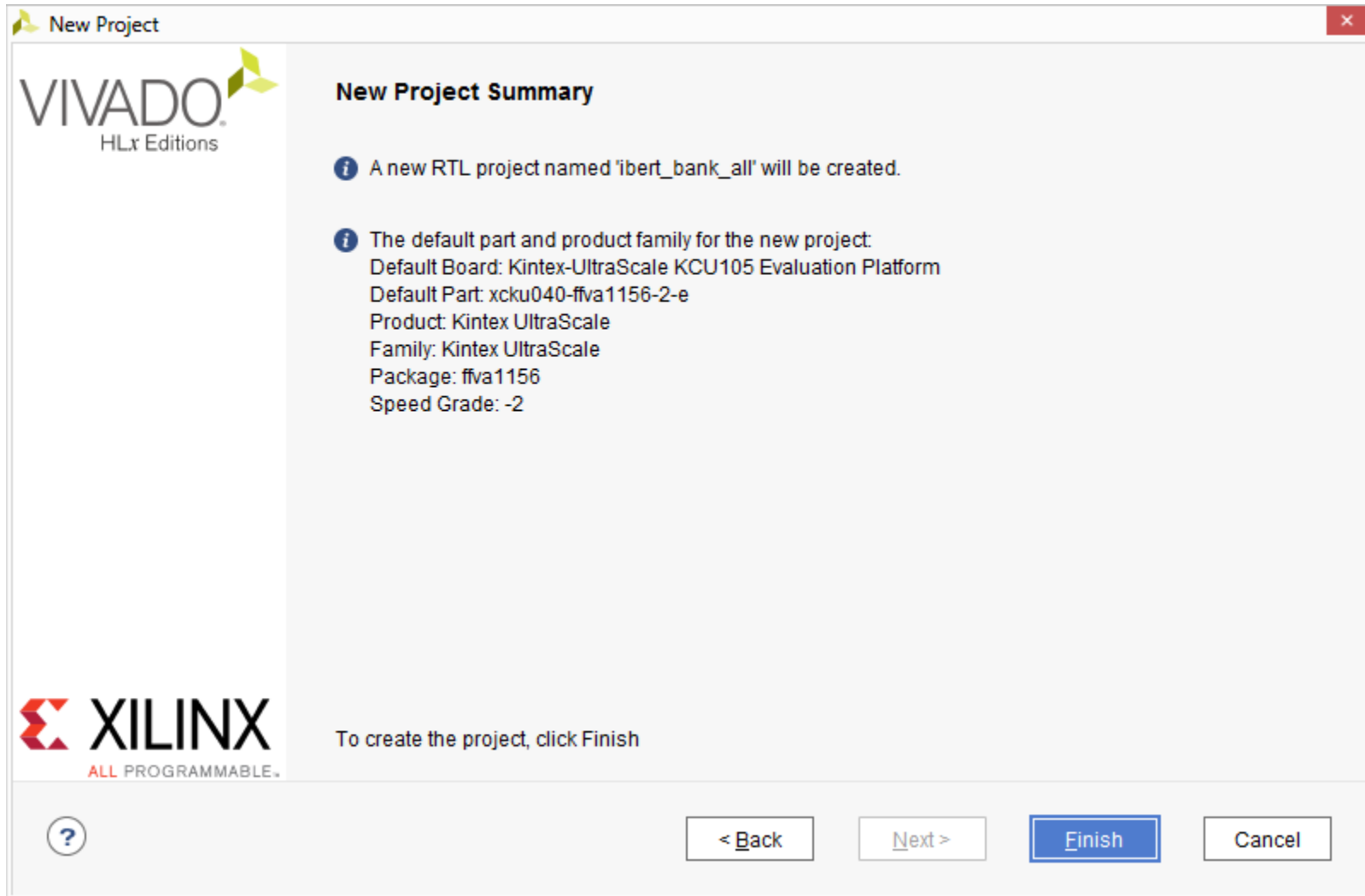
Display Name	Vendor	Board Rev	Part
 Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	 xc7k325tffg900-2
 Kintex-UltraScale KCU105 Evaluation Platform	xilinx.com	1.0	 xcku040-ffva1156-2-e
 Kintex UltraScale+ KCU116 Evaluation Platform	xilinx.com	1.0	 xcku5n-ffvh676-2-e

Board Connectors Target Connections



Create IBERT Design for All Banks

➤ Click **Finish**



Note: Presentation applies to the KCU105

Create IBERT Design for All Banks

➤ Click on **IP Catalog**

The screenshot shows the Vivado 2017.3 interface for a project named 'ibert_bank_all'. The 'Flow Navigator' on the left has 'IP Catalog' highlighted with a red box. The 'PROJECT MANAGER' window shows the 'Sources' tab with 'Design Sources' and 'Hierarchy' options. The 'Properties' window is empty, showing 'Select an object to see properties'. The 'Project Summary' window displays the following information:

Field	Value
Project name:	ibert_bank_all
Project location:	C:/kcu105_ibert/ibert
Product family:	Kintex UltraScale
Project part:	Kintex-UltraScale KC
Top module name:	Not defined

The 'Design Runs' window at the bottom shows a table with the following data:

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes
synth_1	constrs_1	Not started							
impl_1	constrs_1	Not started							

Note: Presentation applies to the KCU105

Create IBERT Design for All Banks

➤ Select **IBERT UltraScale GTH, v1.3** under Debug & Verification

The screenshot shows the Vivado 2017.3 IP Catalog window. The 'IP Catalog' tab is active, displaying a table of IP cores. The 'IBERT Ultrascale GTH' core is highlighted in blue. The table columns are Name, AXI4, Status, and License. Below the table, the 'Details' section shows the Name as 'IBERT Ultrascale GTH' and the Version as '1.3 (Rev. 8)'. The 'Flow Navigator' on the left shows the 'IP Catalog' option selected under the 'PROJECT MANAGER' section.

Name	AXI4	Status	License
Debug & Verification			
Debug			
Debug Bridge		Production	Included
IBERT Ultrascale GTH		Production	Included
ILA (Integrated Logic Analyzer)	AXI4, AXI4-Stream	Production	Included
In System IBERT		Production	Included

Details

Name: **IBERT Ultrascale GTH**

Version: 1.3 (Rev. 8)

Description: The IBERT Ultrascale GTH Core is customizable and designed for evaluating and monitoring

Note: Presentation applies to the KCU105

XILINX ➤ ALL PROGRAMMABLE™

Create IBERT Design for All Banks

➤ Right click on **IBERT UltraScale GTH** and select **Customize IP...**

The screenshot shows the Vivado 2017.3 interface. The 'PROJECT MANAGER - ibert_bank_all' window is open, displaying the 'IP Catalog' tab. The 'Cores' section is active, and the 'IBERT Ultrascale GTH' core is selected. A context menu is open over the core, with 'Customize IP...' highlighted. The 'Details' section for the selected core shows:

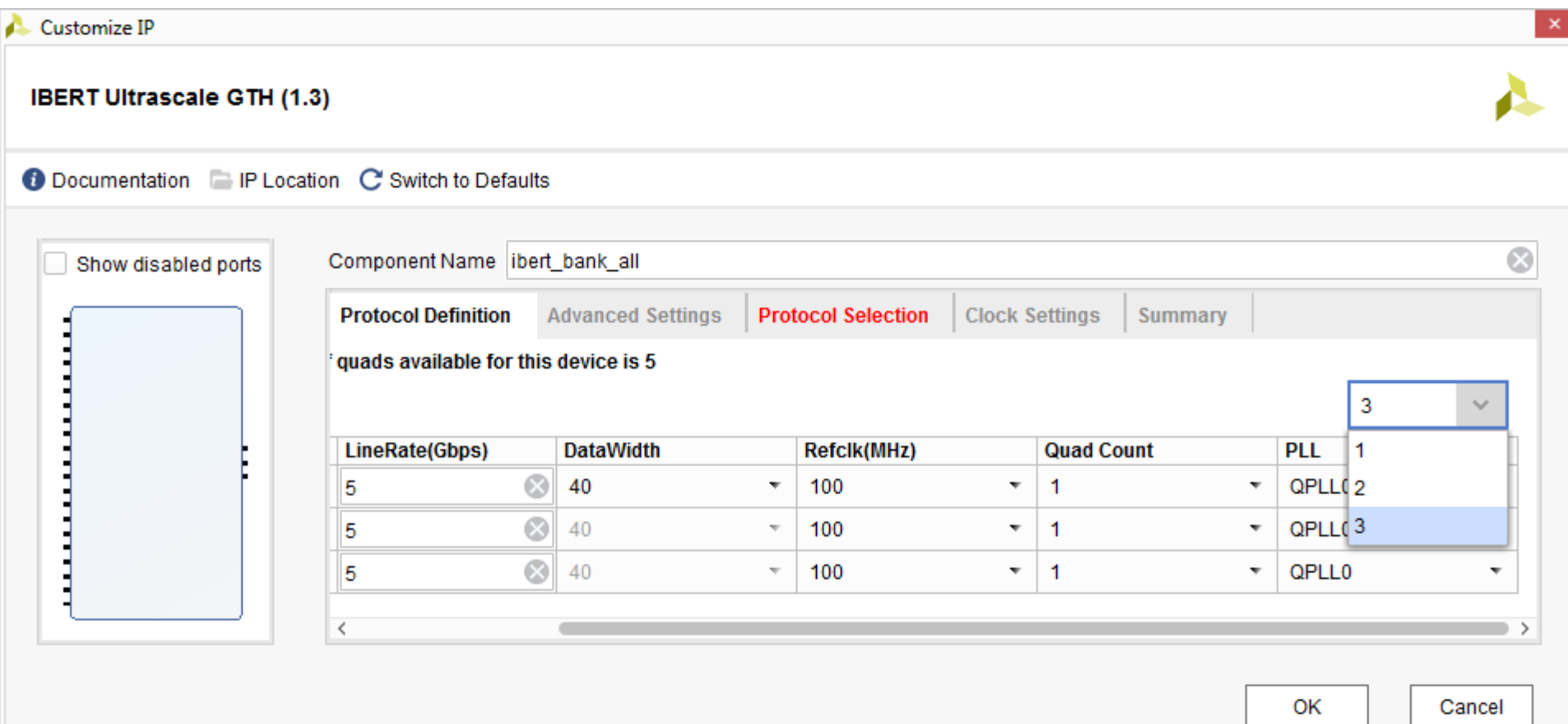
Name	AXI4	Status	License
Debug & Verification			
Debug			
Debug Bridge		Production	Included
IBERT Ultrascale GTH		Production	Included
ILA (Integrated Logic Analyzer)			Included
In System IBERT			

Details for IBERT Ultrascale GTH:
Name: IBERT Ultrascale GTH
Version: 1.3 (Rev. 8)
Description: The IBERT Ultrascale GTH Core is customizable

Note: Presentation applies to the KCU105

Create IBERT Design for All Banks

- Set the Component name: **ibert_bank_all**
- Under the **Protocol Definition** tab
 - Select **3** Protocols



Customize IP

IBERT Ultrascale GTH (1.3)

Documentation IP Location Switch to Defaults

Component Name

Protocol Definition Advanced Settings Protocol Selection Clock Settings Summary

quads available for this device is 5

LineRate(Gbps)	DataWidth	Refclk(MHz)	Quad Count	PLL
5	40	100	1	QPLL0
5	40	100	1	QPLL1
5	40	100	1	QPLL2

3

OK Cancel

Create IBERT Design for All Banks

► Under the **Protocol Definition** tab

- Protocol **Custom 1**: LineRate: **8.0**, Refclk: **100** Quad Count: **2**
- Protocol **Custom 2**: LineRate: **10.3125**, Refclk: **156.25** Quad Count: **1**
- Protocol **Custom 3**: LineRate: **16.3**, Refclk: **163** Quad Count: **2**

Customize IP

IBERT Ultrascale GTH (1.3)

Documentation IP Location Switch to Defaults

Component Name

Protocol Definition | **Advanced Settings** | **Protocol Selection** | Clock Settings | Summary

The maximum number of quads available for this device is 5

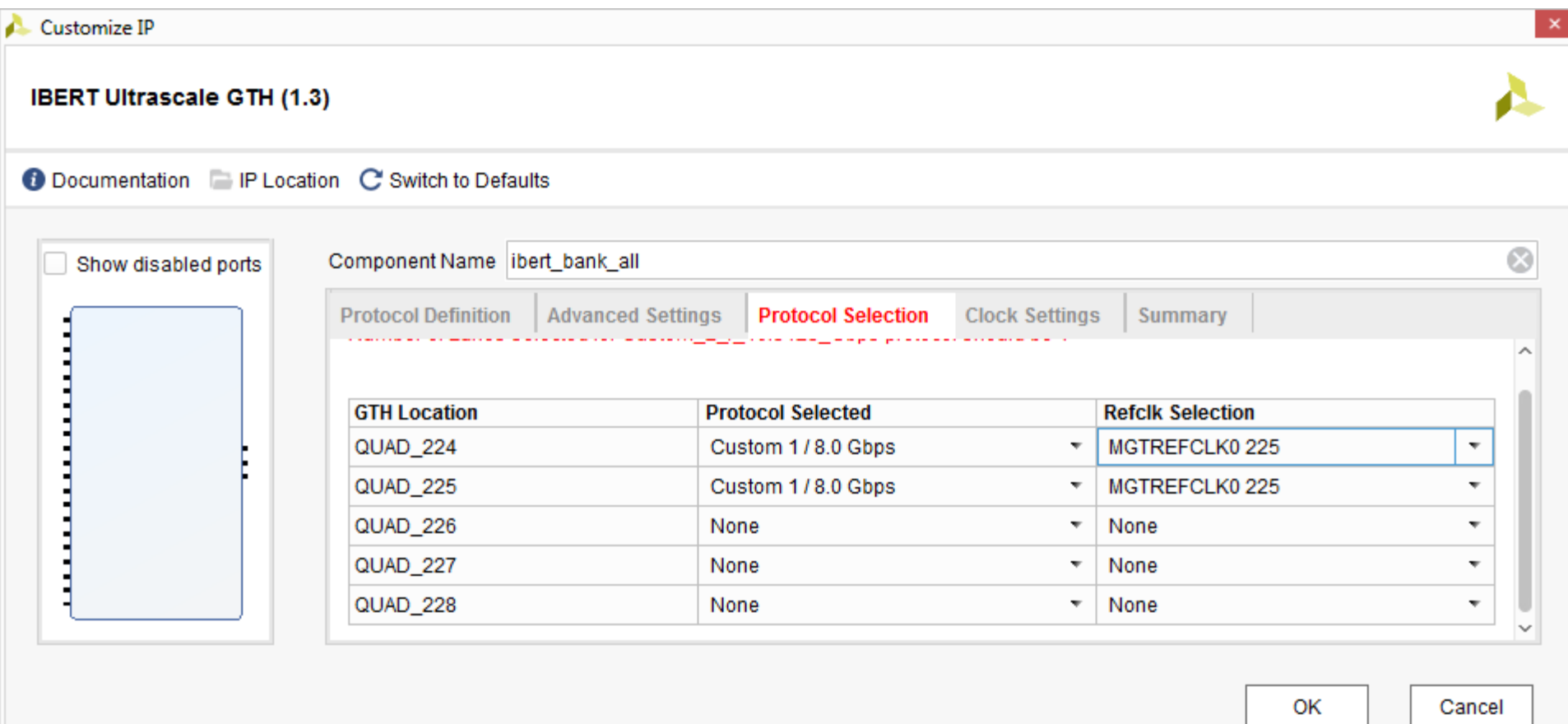
Number of Protocols

Protocol	LineRate(Gbps)	DataWidth	Refclk(MHz)	Quad Count
Custom 1	8.0	40	100	2
Custom 2	10.3125	40	156.25	1
Custom 3	16.3	40	163	2

OK Cancel

Create IBERT Design for All Banks

- Under the **Protocol Selection** tab
- Set **QUAD_224** and **QUAD_225** to
 - **Custom 1 / 8.0 Gbps**, and **MGTREFCLK0 225**



The screenshot shows the 'Customize IP' dialog for 'IBERT Ultrascale GTH (1.3)'. The 'Protocol Selection' tab is active, displaying a table of GTH locations and their configurations. The 'Component Name' is 'ibert_bank_all'. The table lists GTH locations from QUAD_224 to QUAD_228. QUAD_224 and QUAD_225 are configured with 'Custom 1 / 8.0 Gbps' and 'MGTREFCLK0 225'. QUAD_226, QUAD_227, and QUAD_228 are set to 'None'.

Component Name:

Protocol Definition | Advanced Settings | **Protocol Selection** | Clock Settings | Summary

GTH Location	Protocol Selected	Refclk Selection
QUAD_224	Custom 1 / 8.0 Gbps	MGTREFCLK0 225
QUAD_225	Custom 1 / 8.0 Gbps	MGTREFCLK0 225
QUAD_226	None	None
QUAD_227	None	None
QUAD_228	None	None

Buttons: OK, Cancel

Create IBERT Design for All Banks

- Set **QUAD_226** to
 - **Custom 2 / 10.3125 Gbps**, and **MGTREFCLK1 227**
- Set **QUAD_227** and **QUAD_228** to
 - **Custom 3 / 16.3 Gbps**, and **MGTREFCLK0 227**

Customize IP

IBERT Ultrascale GTH (1.3)

Documentation IP Location Switch to Defaults

Component Name

Protocol Definition Advanced Settings **Protocol Selection** Clock Settings Summary

GTH Location	Protocol Selected	Refclk Selection
QUAD_224	Custom 1 / 8.0 Gbps	MGTREFCLK0 225
QUAD_225	Custom 1 / 8.0 Gbps	MGTREFCLK0 225
QUAD_226	Custom 2 / 10.3125 Gbps	MGTREFCLK1 227
QUAD_227	Custom 3 / 16.3 Gbps	MGTREFCLK0 227
QUAD_228	Custom 3 / 16.3 Gbps	MGTREFCLK0 227

OK Cancel

Create IBERT Design for All Banks

► Under the **Clock Settings** tab, set the System Clock:

- **DIFF SSTL12**, P Package Pin: **AK17**, Frequency: **300**
- Deselect **Enable DIFF Term**

Customize IP

IBERT Ultrascale GTH (1.3)

Documentation IP Location Switch to Defaults

Component Name

Show disabled ports

Add RXOUTCLK Probes

Clock Type	Source	I/O Standard	P Package Pin	Frequency(MHz)
System Clock	External	DIFF SSTL12	AK17	300

System Clock Termination Settings

Enable DIFF Term

OK Cancel

Create IBERT Design for All Banks

➤ Review the summary and click **OK**

Customize IP

IBERT Ultrascale GTH (1.3)

[Documentation](#) [IP Location](#) [Switch to Defaults](#)

Show disabled ports

Component Name:

Protocol Definition | Advanced Settings | Protocol Selection | Clock Settings | **Summary**

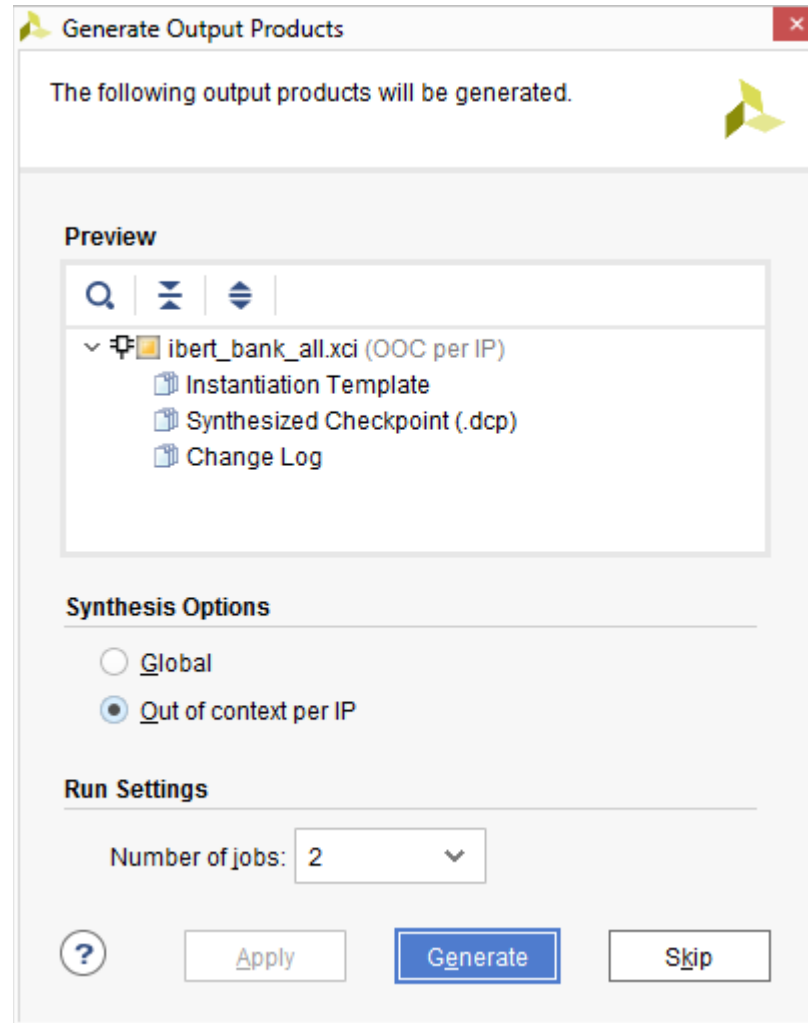
IBERT Design Summary

Number of Protocols	3
System Clock Source	External (P Pin : AK17)
System Clock Frequency	300
RefClk Sources	3

OK Cancel

Create IBERT Design for All Banks

➤ Click **Generate**



Note: This step will take about 10 minutes

Create IBERT Design for All Banks

➤ The Generated IBERT IP appears in Design Sources

– Wait until checkmark appears on **ibert_bank_all_synth_1**

The screenshot shows the Vivado 2017.3 interface. The Project Manager window is open, displaying the Sources panel with a tree view of Design Sources (1). The Synthesis Run Properties panel shows a green checkmark next to 'ibert_bank_all_synth_1'. The Design Runs panel at the bottom shows a table of synthesis runs.

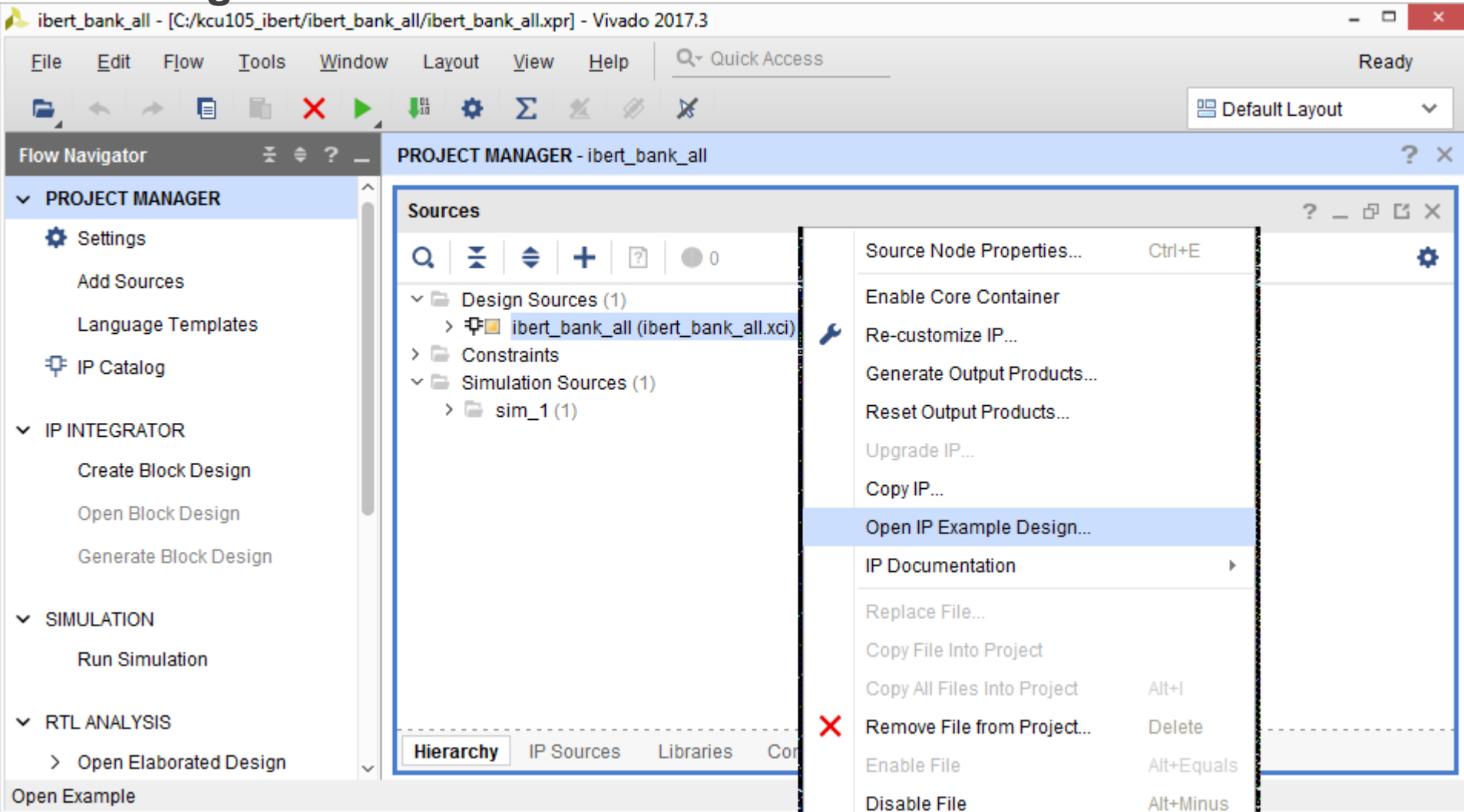
Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS
synth_1 (auto)	constrs_1	Not started					
▶ impl_1	constrs_1	Not started					
Out-of-Context Module Runs							
✔ ibert_bank_all_synth_1	ibert_bank_all	synth_design Complete!					

Note: Presentation applies to the KCU105

XILINX ➤ ALL PROGRAMMABLE™

Compile Example Design

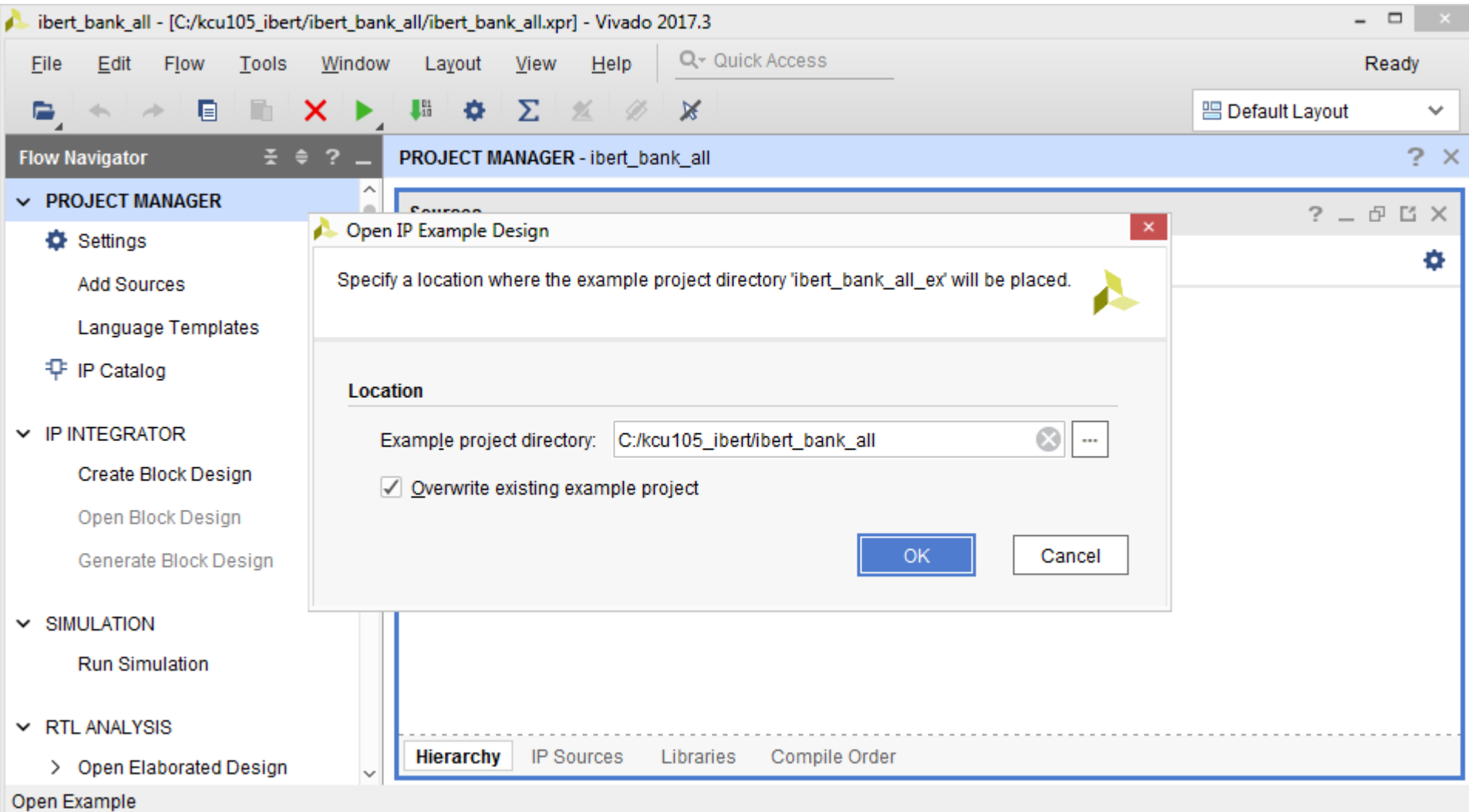
➤ Right click on **ibert_bank_all** and select **Open IP Example Design...**



Note: Presentation applies to the KCU105

Compile Example Design

➤ Set the location to **C:/kcu105_ibert/ibert_bank_all** and click **OK**



Compile Example Design

- A new project is created
- Click **Generate Bitstream**

The screenshot shows the Vivado 2017.3 Project Manager interface for a project named 'ibert_bank_all_ex'. The 'Flow Navigator' on the left lists the project stages: SIMULATION, RTL ANALYSIS, SYNTHESIS, IMPLEMENTATION, and PROGRAM AND DEBUG. The 'Generate Bitstream' option is highlighted under the PROGRAM AND DEBUG stage. The main 'PROJECT MANAGER' window shows the 'Sources' tab, which lists the design sources: Design Sources (4), including 'example_ibert_bank_all (example_ibert_bank_all.v) (1)', Text (3), Constraints (2), and Simulation Sources (1). The status bar at the bottom indicates 'Generate a programming file after implementation'.

Note: The original project window can be closed

Compile Example Design

- Open and view the Implemented Design
- Click **Open Hardware Manager**

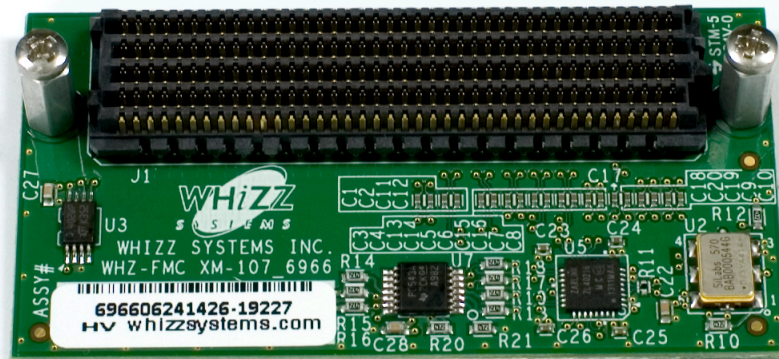
The screenshot shows the Vivado 2017.3 IDE interface. The title bar indicates the project is 'ibert_bank_all_ex' located at '[c:/kcu105_ibert/ibert_bank_all/ibert_bank_all_ex/ibert_bank_all_ex.xpr]'. The main window is titled 'IMPLEMENTED DESIGN - xcku040-ffva1156-2-e (active)'. The interface includes a menu bar (File, Edit, Flow, Tools, Window, Layout, View, Help), a toolbar, and a 'Quick Access' search bar. On the right, a status bar shows 'write_bitstream Complete' with a green checkmark and a 'Default Layout' dropdown menu. The left sidebar is the 'Flow Navigator', which lists various tasks such as 'Constraints Wizard', 'Edit Timing Constraints', 'Report Timing Summary', 'Report Clock Networks', 'Report Clock Interaction', 'Report Methodology', 'Report DRC', 'Report Noise', 'Report Utilization', 'Report Power', and 'Schematic'. Under the 'PROGRAM AND DEBUG' section, the 'Open Hardware Manager' option is highlighted. The main workspace displays a 'Device' window with a 4x4 grid of device images, each labeled with coordinates (X0Y0 to X0Y4, X1Y0 to X1Y4). The bottom of the IDE features a 'Tcl Console' and several tabs for 'Messages', 'Log', 'Reports', 'Design Runs', 'Power', 'DRC', and 'Methodology'.

Note: Presentation applies to the KCU105

Testing All Banks with Optional User Provided Hardware

Hardware Setup with User Provided Hardware

- ▶ Attach a second XM107 to the LPC connector
 - Additional XM107 boards available through [Whizz Systems](#)



Hardware Setup with User Provided Hardware

➤ Two SMA Cables

- www.rosenbergerna.com
- Part number:
72D-32S1-32S1-00610A



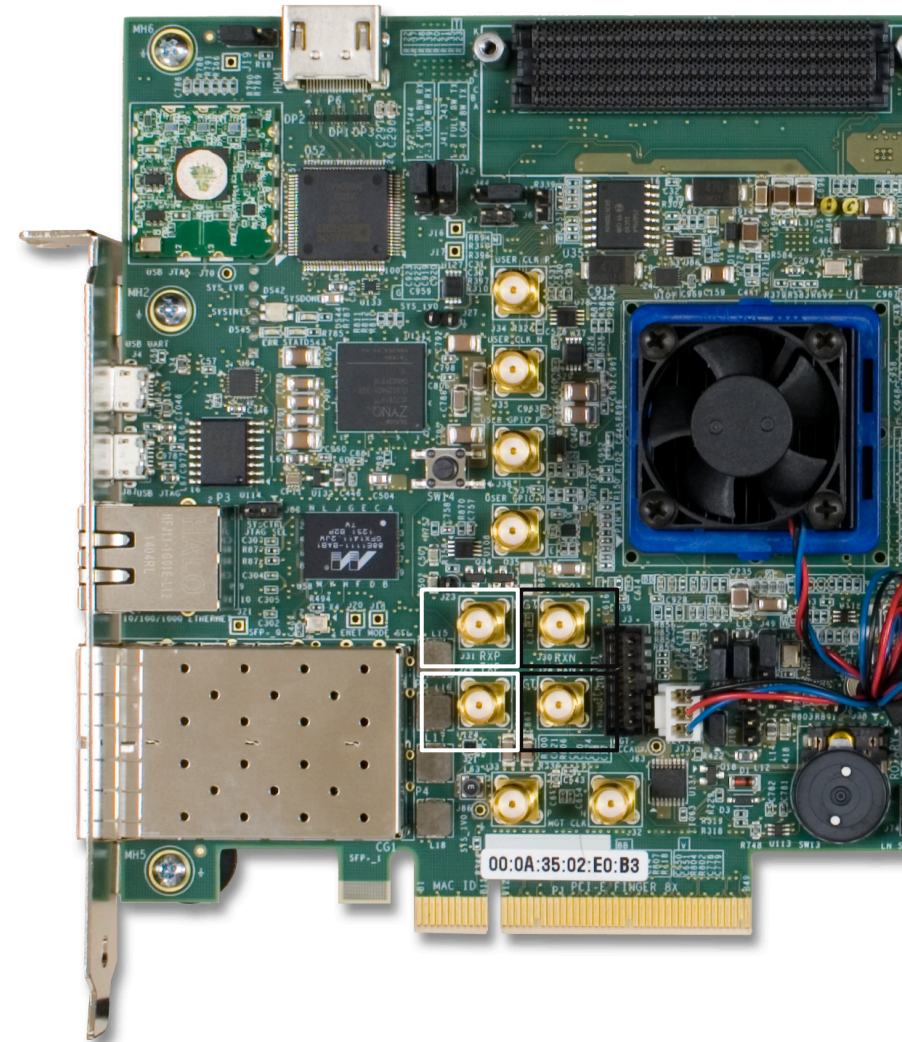
➤ Optional: SMA Quick connects

- RADIALL
- Part number: R125791501
- Available [here](#) or [here](#)



Hardware Setup

- Hook up the SMA cables as shown
- IBERT Test:
 - J29 to J31 (White)
 - J28 to J30 (Black)



Run IBERT Example Design

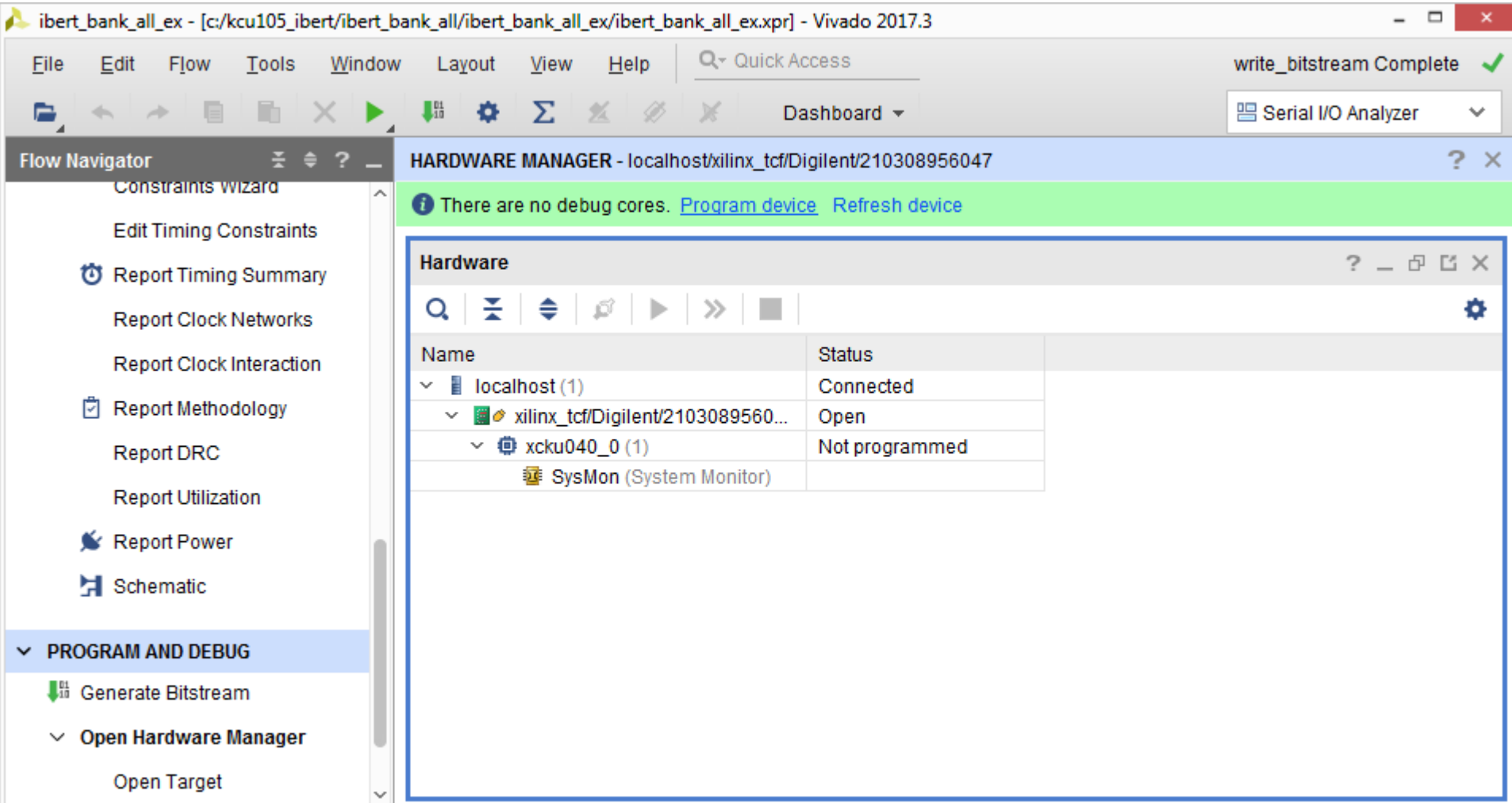
➤ Click **Open target** and select **Auto Connect**

The screenshot displays the Vivado 2017.3 IDE interface. The title bar shows the project name 'ibert_bank_all_ex' and the file path. The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. A toolbar with various icons is visible below the menu bar. The 'Flow Navigator' on the left lists various reports and the 'PROGRAM AND DEBUG' section, which is expanded to show 'Generate Bitstream', 'Open Hardware Manager', and 'Open Target'. The 'Open Hardware Manager' window is active, showing a message: 'No hardware target is open. Open target'. A context menu is open over the 'Hardware' section, with 'Auto Connect' selected. Other options in the menu include 'Recent Targets', 'Available Targets on Server', and 'Open New Target...'. The 'Properties' window below shows 'Select an object to see properties'. The bottom status bar indicates 'Automatically connect to local hardware target'.

Note: Presentation applies to the KCU105

Run IBERT Example Design

➤ Select Program device



The screenshot shows the Vivado 2017.3 interface. The title bar reads "ibert_bank_all_ex - [c:/kcu105_ibert/ibert_bank_all/ibert_bank_all_ex/ibert_bank_all_ex.xpr] - Vivado 2017.3". The top menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. A "Quick Access" search bar is present. The "write_bitstream Complete" status is shown in the top right corner. The "Flow Navigator" on the left lists various tasks, with "PROGRAM AND DEBUG" expanded to show "Generate Bitstream" and "Open Hardware Manager". The "Open Hardware Manager" sub-menu is also expanded, showing "Open Target". The main "HARDWARE MANAGER" window is titled "localhost/xilinx_tcf/Digilent/210308956047" and displays a message: "There are no debug cores. Program device Refresh device". Below this is a "Hardware" table with the following data:

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/2103089560...	Open
xcku040_0 (1)	Not programmed
SysMon (System Monitor)	

Run IBERT Example Design

- The newly created bitstream and LTX files are set to the default
- Click **Program**

The screenshot shows the Vivado 2017.3 interface with the 'Program Device' dialog box open. The dialog box contains the following text: 'Select a bitstream programming file and download it to your hardware device. You can optionally select a debug probes file that corresponds to the debug cores contained in the bitstream programming file.' Below this text are two input fields: 'Bitstream file:' with the value 'bank_all_ex/ibert_bank_all_ex.runs/impl_1/example_ibert_bank_all.bit' and 'Debug probes file:' with the value 'bank_all_ex/ibert_bank_all_ex.runs/impl_1/example_ibert_bank_all.ltx'. There is a checked checkbox for 'Enable end of startup check'. At the bottom of the dialog are 'Program' and 'Cancel' buttons. The background shows the Vivado interface with the 'Flow Navigator' on the left and the 'Hardware Manager' at the top. The status bar at the bottom indicates 'Hardware Device: xcu040_0'.

Run IBERT Example Design

➤ Click Create links

The screenshot shows the Vivado 2017.3 interface. The title bar indicates the project is 'ibert_bank_all_ex' located at '[c:/kcu105_ibert/ibert_bank_all/ibert_bank_all_ex/ibert_bank_all_ex.xpr]'. The 'Flow Navigator' on the left lists various tasks, with 'PROGRAM AND DEBUG' expanded to show 'Open Hardware Manager'. The 'Hardware Manager' window is active, displaying a message: 'There are no serial I/O links. Auto-detect links **Create links**'. Below this, a table lists the hardware components and their status.

Name	Status
localhost (1)	Connected
xilinx_tcf/Digilent/2103089560...	Open
xcku040_0 (2)	Programmed
SysMon (System Monitor)	
IBERT (IBERT)	
Quad_224 (5)	
COMMON_X0Y0	Qpll0 Locked
MGT_X0Y0	8.000 Gbps
MGT_X0Y1	8.010 Gbps
MGT_X0Y2	7.984 Gbps
MGT_X0Y3	8.004 Gbps
Quad_225 (5)	
COMMON_X0Y1	Qpll0 Locked
MGT_X0Y4	8.000 Gbps

Note: Si570 and Si5328 clocks must be set as per XTP352

Run IBERT Example Design

➤ Click on the Add Link button

Create Links

To create a new link select a TX GT and/or an RX GT, then click the Add button on the New Links toolbar.

TX GTs

Search:

- ▶ MGT_X0Y0/TX (xcku040_0/Quad_224)
- ▶ MGT_X0Y1/TX (xcku040_0/Quad_224)
- ▶ MGT_X0Y2/TX (xcku040_0/Quad_224)
- ▶ MGT_X0Y3/TX (xcku040_0/Quad_224)
- ▶ MGT_X0Y4/TX (xcku040_0/Quad_225)
- ▶ MGT_X0Y5/TX (xcku040_0/Quad_225)
- ▶ MGT_X0Y6/TX (xcku040_0/Quad_225)
- ▶ MGT_X0Y7/TX (xcku040_0/Quad_225)

RX GTs

Search:

- ◀ MGT_X0Y0/RX (xcku040_0/Quad_224)
- ◀ MGT_X0Y1/RX (xcku040_0/Quad_224)
- ◀ MGT_X0Y2/RX (xcku040_0/Quad_224)
- ◀ MGT_X0Y3/RX (xcku040_0/Quad_224)
- ◀ MGT_X0Y4/RX (xcku040_0/Quad_225)
- ◀ MGT_X0Y5/RX (xcku040_0/Quad_225)
- ◀ MGT_X0Y6/RX (xcku040_0/Quad_225)
- ◀ MGT_X0Y7/RX (xcku040_0/Quad_225)

New Links

+ **-**

No content

Create link group

Link group description:

Open Serial I/O Analyzer layout

Run IBERT Example Design

➤ Add all the links and click **OK**

Create Links

To create a new link select a TX GT and/or an RX GT, then click the Add button on the New Links toolbar.

TX GTs **RX GTs**

Search:

Search:

New Links

+ | -

Desc... ^1	TX	RX	Internal Loopback
Link 0	MGT_X0Y0/TX (xcku040_0/Quad_224)	MGT_X0Y0/RX (xcku040_0/Quad_224)	<input type="checkbox"/>
Link 1	MGT_X0Y1/TX (xcku040_0/Quad_224)	MGT_X0Y1/RX (xcku040_0/Quad_224)	<input type="checkbox"/>

Create link group

Link group description:

Open Serial I/O Analyzer layout

?

OK Cancel

Run IBERT Example Design

➤ The links appear under the **Serial I/O Links** tab

Hardware Manager - localhost/xilinx_tcf/Digilent/210308956047

Serial I/O Links

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	R
Ungrouped Links (0)									
Link Group 0 (20)									
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	7.998 Gbps	3.175E11	8.3E1	2.614E-10	Reset	PRBS 7-bit	PF
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	7.987 Gbps	3.175E11	9.6E1	3.024E-10	Reset	PRBS 7-bit	PF
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	7.995 Gbps	3.175E11	1.06E2	3.339E-10	Reset	PRBS 7-bit	PF
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	3.176E11	8.8E1	2.771E-10	Reset	PRBS 7-bit	PF
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	7.983 Gbps	3.176E11	1.11E2	3.495E-10	Reset	PRBS 7-bit	PF
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	8.000 Gbps	3.176E11	9.4E1	2.96E-10	Reset	PRBS 7-bit	PF
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	8.000 Gbps	3.176E11	9.1E1	2.865E-10	Reset	PRBS 7-bit	PF
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	8.000 Gbps	3.176E11	9.4E1	2.96E-10	Reset	PRBS 7-bit	PF
Link 8	MGT_X0Y8/TX	MGT_X0Y8/RX	10.313 Gbps	4.094E11	8.6E1	2.1E-10	Reset	PRBS 7-bit	PF
Link 9	MGT_X0Y9/TX	MGT_X0Y9/RX	10.313 Gbps	4.095E11	9.5E1	2.32E-10	Reset	PRBS 7-bit	PF
Link 10	MGT_X0Y10/TX	MGT_X0Y10/RX	10.311 Gbps	4.095E11	1.07E2	2.613E-10	Reset	PRBS 7-bit	PF
Link 11	MGT_X0Y11/TX	MGT_X0Y11/RX	10.313 Gbps	4.095E11	9.2E1	2.247E-10	Reset	PRBS 7-bit	PF
Link 12	MGT_X0Y12/TX	MGT_X0Y12/RX	16.300 Gbps	6.472E11	5.684E3	8.782E-9	Reset	PRBS 7-bit	PF

Run IBERT Example Design

➤ Set all TX and RX Patterns to **PRBS 31-bit**

The screenshot shows the Vivado 2017.3 Hardware Manager interface. The 'Serial I/O Links' tab is active, displaying a table of link configurations. The 'TX Pattern' dropdown menu is open, showing options: PRBS 7-bit, PRBS 9-bit, PRBS 15-bit, PRBS 23-bit, PRBS 31-bit (highlighted), Fast Clk, and Slow Clk. The table below shows the configuration for various links, with PRBS 31-bit selected for the TX Pattern.

TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-
						Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y0/TX	MGT_X0Y0/RX	7.998 Gbps	4.687E11	8.3E1	1.771E-10	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y1/TX	MGT_X0Y1/RX	8.002 Gbps	4.687E11	9.6E1	2.048E-10	Reset	PRBS 9-bit	PRBS 7-bit	0.00 dE
MGT_X0Y2/TX	MGT_X0Y2/RX	8.000 Gbps	4.687E11	1.06E2	2.262E-10	Reset	PRBS 15-bit	PRBS 7-bit	0.00 dE
MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	4.687E11	8.8E1	1.877E-10	Reset	PRBS 23-bit	PRBS 7-bit	0.00 dE
MGT_X0Y4/TX	MGT_X0Y4/RX	8.000 Gbps	4.687E11	1.11E2	2.368E-10	Reset	PRBS 31-bit	PRBS 7-bit	0.00 dE
MGT_X0Y5/TX	MGT_X0Y5/RX	8.000 Gbps	4.688E11	9.4E1	2.005E-10	Reset	Fast Clk	PRBS 7-bit	0.00 dE
MGT_X0Y6/TX	MGT_X0Y6/RX	8.000 Gbps	4.688E11	9.1E1	1.941E-10	Reset	Slow Clk	PRBS 7-bit	0.00 dE
MGT_X0Y7/TX	MGT_X0Y7/RX	8.000 Gbps	4.688E11	9.4E1	2.005E-10	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y8/TX	MGT_X0Y8/RX	10.313 Gbps	6.043E11	8.6E1	1.423E-10	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y9/TX	MGT_X0Y9/RX	10.313 Gbps	6.044E11	9.5E1	1.572E-10	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y10/TX	MGT_X0Y10/RX	10.308 Gbps	6.044E11	1.07E2	1.77E-10	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y11/TX	MGT_X0Y11/RX	10.313 Gbps	6.044E11	9.2E1	1.522E-10	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE
MGT_X0Y12/TX	MGT_X0Y12/RX	16.300 Gbps	9.553E11	5.684E3	5.95E-9	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dE

Link Group: Link Group 0

Note: Presentation applies to the KCU105

Run IBERT Example Design

➤ Click the BERT Reset button to reset the link error counts

The screenshot shows the Vivado 2017.3 Hardware Manager interface. The 'Serial I/O Links' tab is active, displaying a table of link configurations. The 'BERT Reset' column contains buttons for each link, with the top button highlighted by a red box. The table includes columns for TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, and TX Pre-.

TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-
						<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y0/TX	MGT_X0Y0/RX	8.000 Gbps	6.619E11	8.863E9	1.339E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y1/TX	MGT_X0Y1/RX	7.997 Gbps	6.619E11	8.863E9	1.339E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y2/TX	MGT_X0Y2/RX	8.000 Gbps	6.619E11	8.863E9	1.339E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	6.619E11	8.862E9	1.339E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y4/TX	MGT_X0Y4/RX	7.997 Gbps	6.619E11	8.86E9	1.339E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y5/TX	MGT_X0Y5/RX	8.000 Gbps	6.619E11	8.861E9	1.339E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y6/TX	MGT_X0Y6/RX	8.010 Gbps	6.62E11	8.863E9	1.339E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y7/TX	MGT_X0Y7/RX	8.003 Gbps	6.62E11	8.862E9	1.339E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y8/TX	MGT_X0Y8/RX	10.313 Gbps	8.535E11	1.142E10	1.338E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y9/TX	MGT_X0Y9/RX	10.313 Gbps	8.536E11	1.142E10	1.338E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y10/TX	MGT_X0Y10/RX	10.313 Gbps	8.536E11	1.143E10	1.339E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y11/TX	MGT_X0Y11/RX	10.313 Gbps	8.536E11	1.143E10	1.339E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE
MGT_X0Y12/TX	MGT_X0Y12/RX	16.300 Gbps	1.349E12	1.807E10	1.339E-2	<input type="button" value="Reset"/>	PRBS 31-bit	PRBS 31-bit	0.00 dE

Note: Presentation applies to the KCU105

Run IBERT Example Design

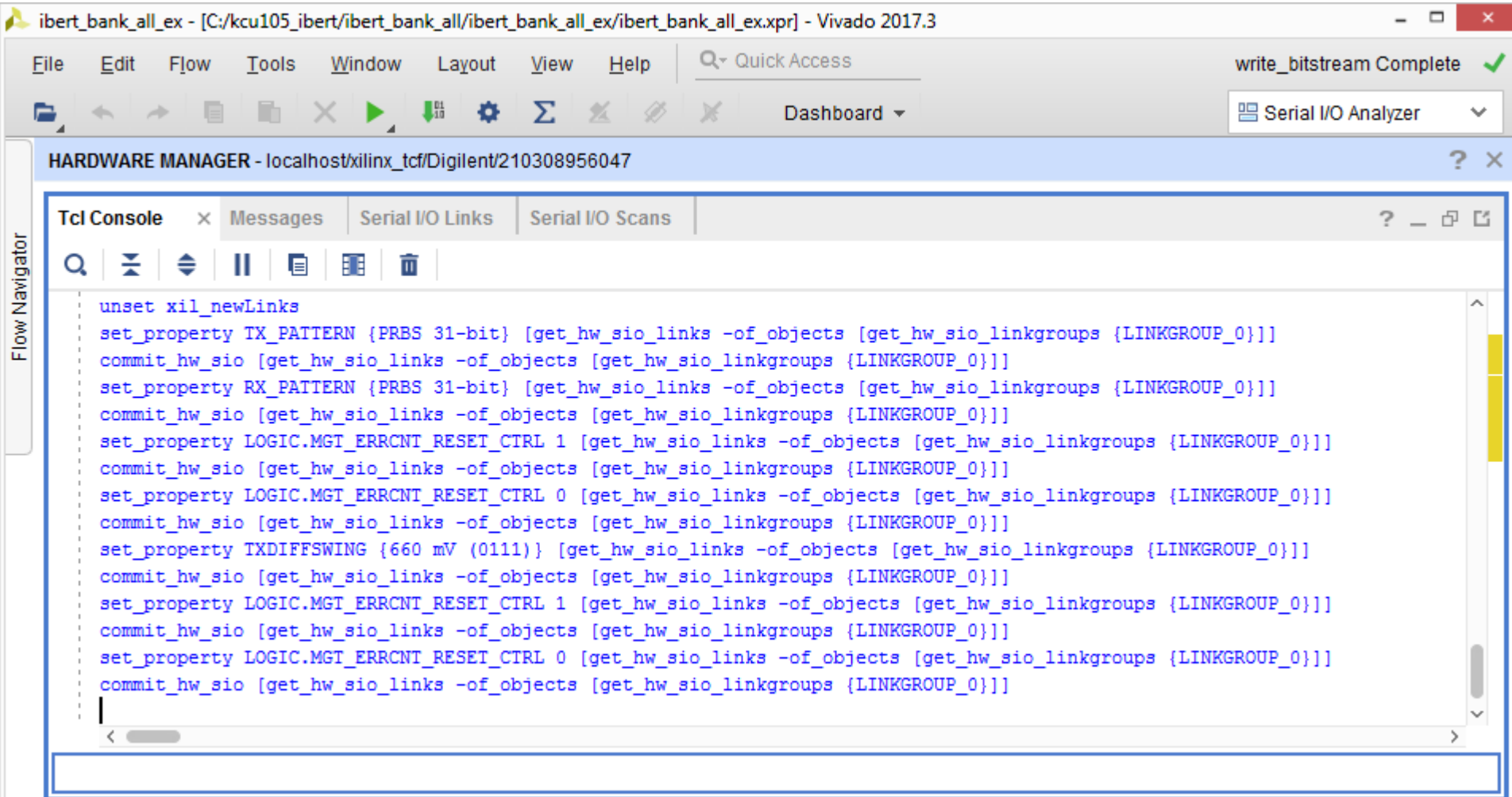
➤ All links are showing no errors

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
Link Group 0 (20)									
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	7.989 Gbps	1.455E12	0E0	6.871E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	8.009 Gbps	1.455E12	0E0	6.872E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	8.000 Gbps	1.455E12	0E0	6.872E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	8.000 Gbps	1.455E12	0E0	6.872E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	8.000 Gbps	1.455E12	0E0	6.872E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	8.006 Gbps	1.455E12	0E0	6.872E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	8.000 Gbps	1.455E12	0E0	6.875E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	8.000 Gbps	1.455E12	0E0	6.874E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 8	MGT_X0Y8/TX	MGT_X0Y8/RX	10.313 Gbps	1.875E12	0E0	5.332E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 9	MGT_X0Y9/TX	MGT_X0Y9/RX	10.308 Gbps	1.875E12	0E0	5.333E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 10	MGT_X0Y10/TX	MGT_X0Y10/RX	10.313 Gbps	1.875E12	0E0	5.332E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 11	MGT_X0Y11/TX	MGT_X0Y11/RX	10.313 Gbps	1.875E12	0E0	5.332E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 12	MGT_X0Y12/TX	MGT_X0Y12/RX	16.300 Gbps	2.964E12	0E0	3.374E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 13	MGT_X0Y13/TX	MGT_X0Y13/RX	16.300 Gbps	2.964E12	0E0	3.374E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 14	MGT_X0Y14/TX	MGT_X0Y14/RX	16.303 Gbps	2.964E12	0E0	3.373E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 15	MGT_X0Y15/TX	MGT_X0Y15/RX	16.300 Gbps	2.964E12	0E0	3.373E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 16	MGT_X0Y16/TX	MGT_X0Y16/RX	16.314 Gbps	2.964E12	0E0	3.373E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 17	MGT_X0Y17/TX	MGT_X0Y17/RX	16.300 Gbps	2.964E12	0E0	3.373E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 18	MGT_X0Y18/TX	MGT_X0Y18/RX	16.281 Gbps	2.964E12	0E0	3.373E-13	Reset	PRBS 31-bit	PRBS 31-bit
Link 19	MGT_X0Y19/TX	MGT_X0Y19/RX	16.300 Gbps	2.964E12	0E0	3.373E-13	Reset	PRBS 31-bit	PRBS 31-bit

Note: If FMC HPC shows errors, set TXDIFFSWING to 660 mV XILINX ➤ ALL PROGRAMMABLE.

Run IBERT Example Design

➤ Tcl console commands can be saved as TCL file for later playback



The screenshot shows the Vivado 2017.3 interface. The title bar indicates the project is 'ibert_bank_all_ex' located at 'C:/kcu105_ibert/ibert_bank_all/ibert_bank_all_ex/ibert_bank_all_ex.xpr'. The 'Hardware Manager' window is open, showing the 'Tcl Console' tab. The console contains the following commands:

```
unset xil_newLinks
set_property TX_PATTERN {PRBS 31-bit} [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
set_property RX_PATTERN {PRBS 31-bit} [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
set_property LOGIC.MGT_ERRCNT_RESET_CTRL 1 [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
set_property LOGIC.MGT_ERRCNT_RESET_CTRL 0 [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
set_property TXDIFFSWING {660 mV (0111)} [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
set_property LOGIC.MGT_ERRCNT_RESET_CTRL 1 [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
set_property LOGIC.MGT_ERRCNT_RESET_CTRL 0 [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
```

References

References

➤ IBERT IP

- LogiCORE IP Integrated Bit Error Ratio Tester for UltraScale GTH – PG173
 - https://www.xilinx.com/support/documentation/ip_documentation/ibert_ultrascale_gth/v1_3/pg173-ibert-ultrascale-gth.pdf

➤ Vivado Release Notes

- Vivado Design Suite User Guide - Release Notes – UG973
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_3/ug973-vivado-release-notes-install-license.pdf
- Vivado Design Suite 2017 - Vivado Known Issues
 - <https://www.xilinx.com/support/answers/68923.html>

➤ Vivado Programming and Debugging

- Vivado Design Suite Programming and Debugging User Guide – UG908
 - https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_3/ug908-vivado-programming-debugging.pdf

Documentation

Documentation

➤ Kintex UltraScale

- Kintex UltraScale FPGA Family

- <https://www.xilinx.com/products/silicon-devices/fpga/kintex-ultrascale.html>

➤ KCU105 Documentation

- Kintex UltraScale FPGA KCU105 Evaluation Kit

- <https://www.xilinx.com/products/boards-and-kits/kcu105.html>

- KCU105 Board User Guide – UG917

- https://www.xilinx.com/support/documentation/boards_and_kits/kcu105/ug917-kcu105-eval-bd.pdf

- KCU105 Evaluation Kit Quick Start Guide User Guide – XTP391

- https://www.xilinx.com/support/documentation/boards_and_kits/kcu105/xtp391-kcu105-quickstart.pdf

- KCU105 - Known Issues Master Answer Record

- <https://www.xilinx.com/support/answers/63175.html>