Concept for a shingled 1Mpix ePixM camera

June 24, 2020

on behalf of SLAC TID
Detector Team
Electronic system
Integrated Circuits

U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

Motivation

- ePixM project aims a developing a high rate camera for soft x-rays experiment at LCLS
  - Soft x-ray scattering/imaging detectors form a significant part of the LCLS detector development strategy
    - Key detector for soft x-ray (SXR) resonant elastic x-ray scattering (REXS) experiments in LCLS NEH 2.2.
    - XPCS
    - Other Coherent Scattering (CS) experiments

Goal for this project

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- *On going ePixM project aims at developing a tileable 192x384 pixels camera prototype with performance within requirements*

- *Goal of the proposed project:*
  - ***Develop a low risk concept for tileing ePixM prototype modules into a large area 1Mpix camera.***
  - *Setup the infrastructure for soft x-ray entrance window fabrication*

- Critical for:
  - being in the conditions to present required results for the FY20 down-selection process comparing ePixM to VFCCD

Motivation

TID-AIR SLAC

- Project requirements

Parameter	Threshold	Objective	REXS	XPCS	CS	1MPixM
Pixel Pitch (um)	50	50	✓	✓	✓	50
Read Noise (e- rms)	15	10		✓	✓	12
Quantum efficiency (%, 275eV-1500eV)	70	90	✓	✓	✓	~84
Frame Rate (kHz)	5	10	✓	✓	✓	7.5
Array size (pixels)	512x512	1024x1024	✓	✓	✓	1152x1152
Well Depth (Number of 530eV photons)	1000	3000	✓		✓	>1000
Vacuum outgassing rate (torr*L/s)	2E-8	1E-8	✓			2E-8
Cabling and cooling length (m)	2	4	✓		✓	2
Physical package envelope (WxLxD, mm)	100x175x75mm	75x150x50mm	✓			100x175x75mm
Maximum Power dissipation (W)	100[1]	50	✓	✓	✓	250

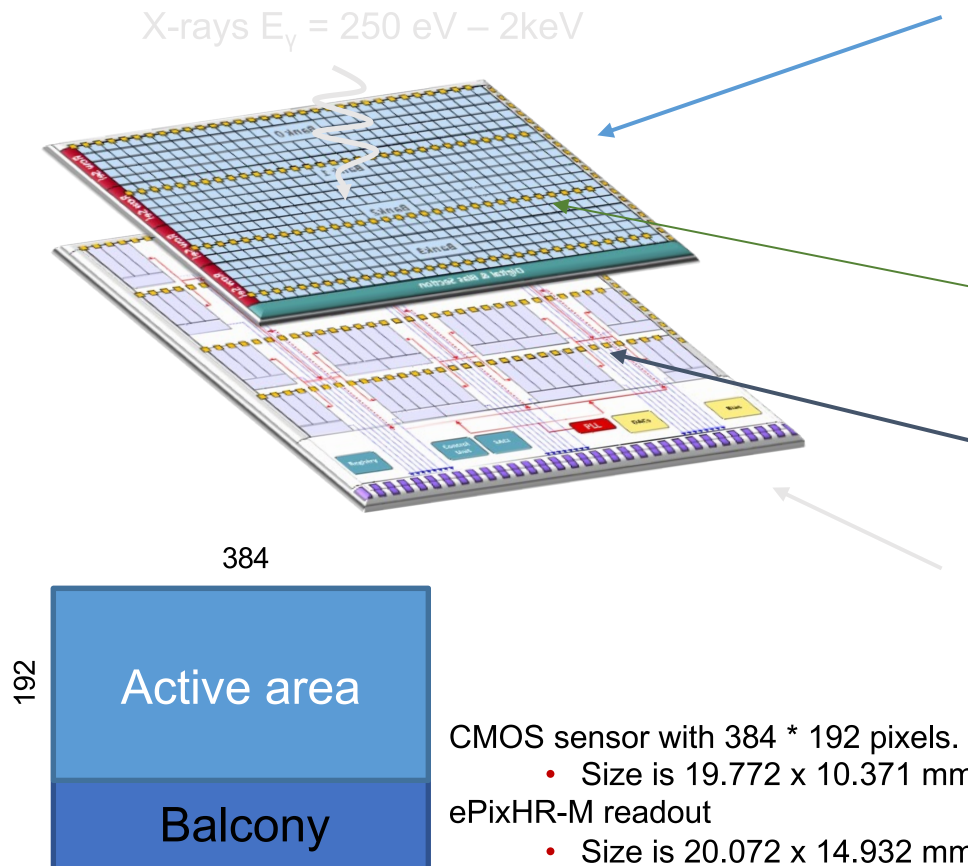
1 – Assuming a 2x3 tiles or 768x576 consumes 125W

Array Size:

- Impractical to complete a full-size device in FY20,
- In FY20 compliance with this requirement can be met on the basis of a demonstrated tileable submodule, as long as a low-risk path to realizing the threshold array size requirement with a fill factor >80% is demonstrated.

Standard modular hybrid approach

Core module architecture:



CMOS sensor with 384 * 192 pixels.
- Size is 19.772 x 10.371 mm

ePixHR-M readout
- Size is 20.072 x 14.932 mm

ePixM monolithic front-end

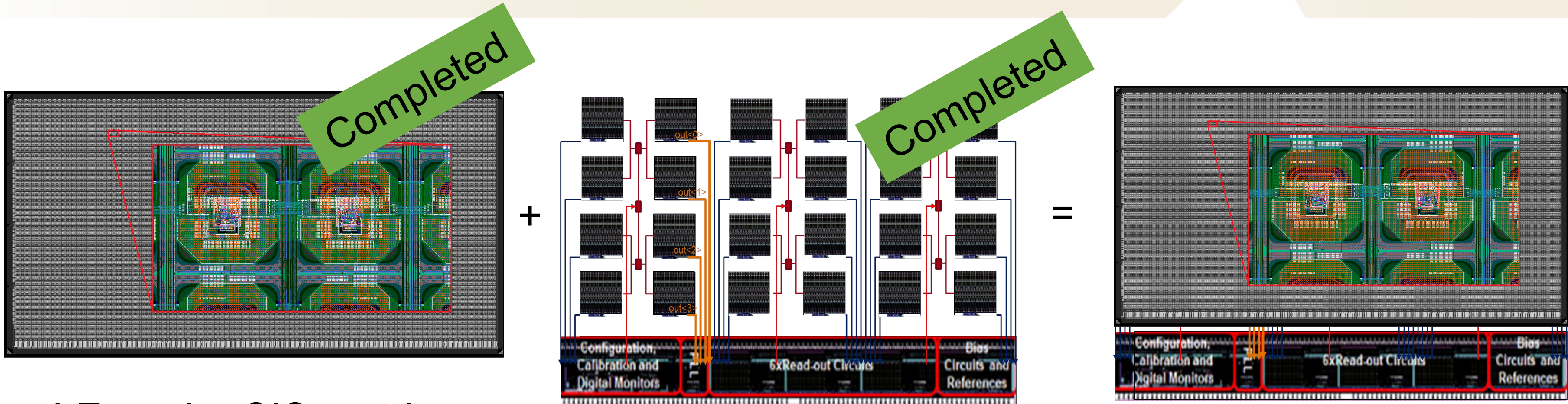
Fully depleted CMOS Image Sensor with front-end circuitry
- on-sensors amplifier reduces input detector capacitance and thus noise
- Back-thinned and back illuminated
- Entrance window optimized for soft X-rays (demonstrated)

Standard micro-bumps

Readout ASIC (ROIC)

Variant of the ePixHR back-end
- 4 arrays of 192 ADCs
- Each array is a copy of the ePixHR back-end (demonstrated)

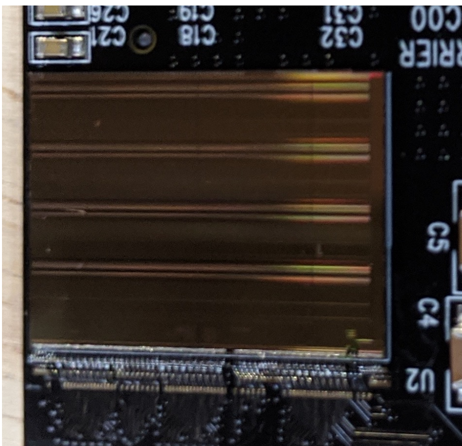
ePixM module (cartoon)



LFoundry CIS matrix
192 x 384 pixels
19772 x 10371 µm

ePixM HR backend
768 (4 x 192) ADCs
20072 x 14932 µm

Bump bonded
192x384 pixel module

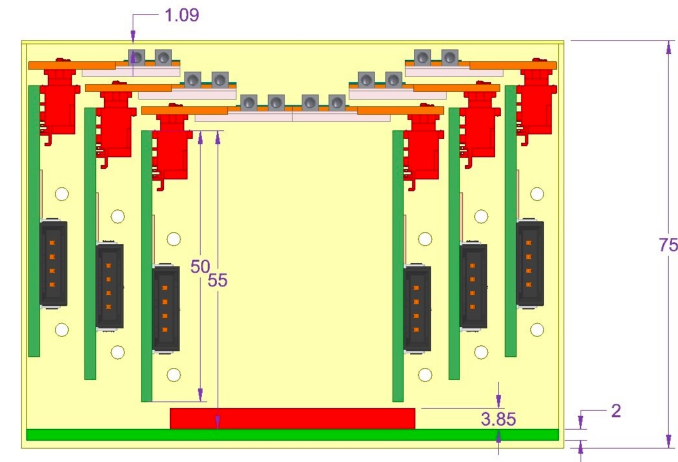


- *Backend is currently being tested without the sensor.*

- *To avoid gaps in the detectors shingling is required to hide balconies when tiling modules*

ePix M camera system

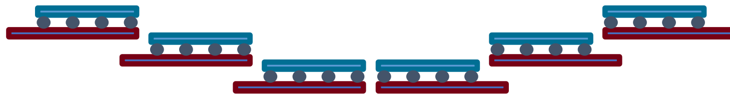
- Components
  - ***Front end electronics***
    - *Tightly connected to ASIC geometry/shingle geometry*
    - *Power to ASICs/sensor*
    - *Control signal to ASICs*
    - *Data access to ASIC*
    - *Cooling system*
  - ***Camera DAQ***
    - *IO to FPGA*
    - *Control logic*
    - *Data storage (full frames)*
    - *Data compression*
    - *Data transmission*
  - Back end DAQ
    - User interface
    - Data reception
    - Data storage



- *Aspects to be studied*
  - *Mechanics*
  - *Thermal dissipation*
  - *Power distribution*
  - *Signal distribution*
  - *Data reduction*

Tiling for a 1Mpix camera

Side view



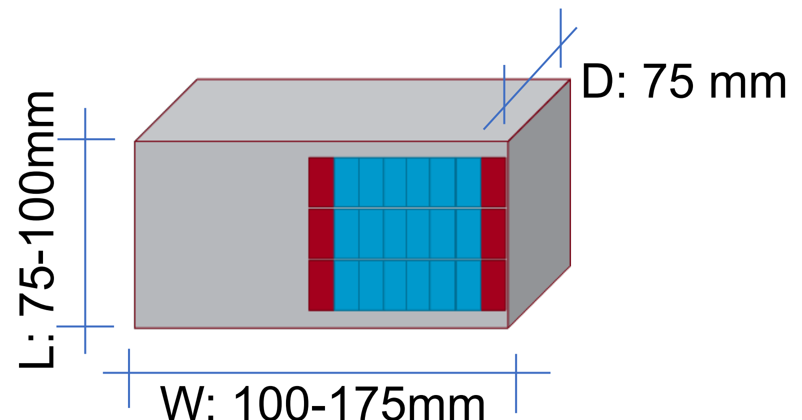
1152 (active area of ~ 57.2mmx 57.2mm)

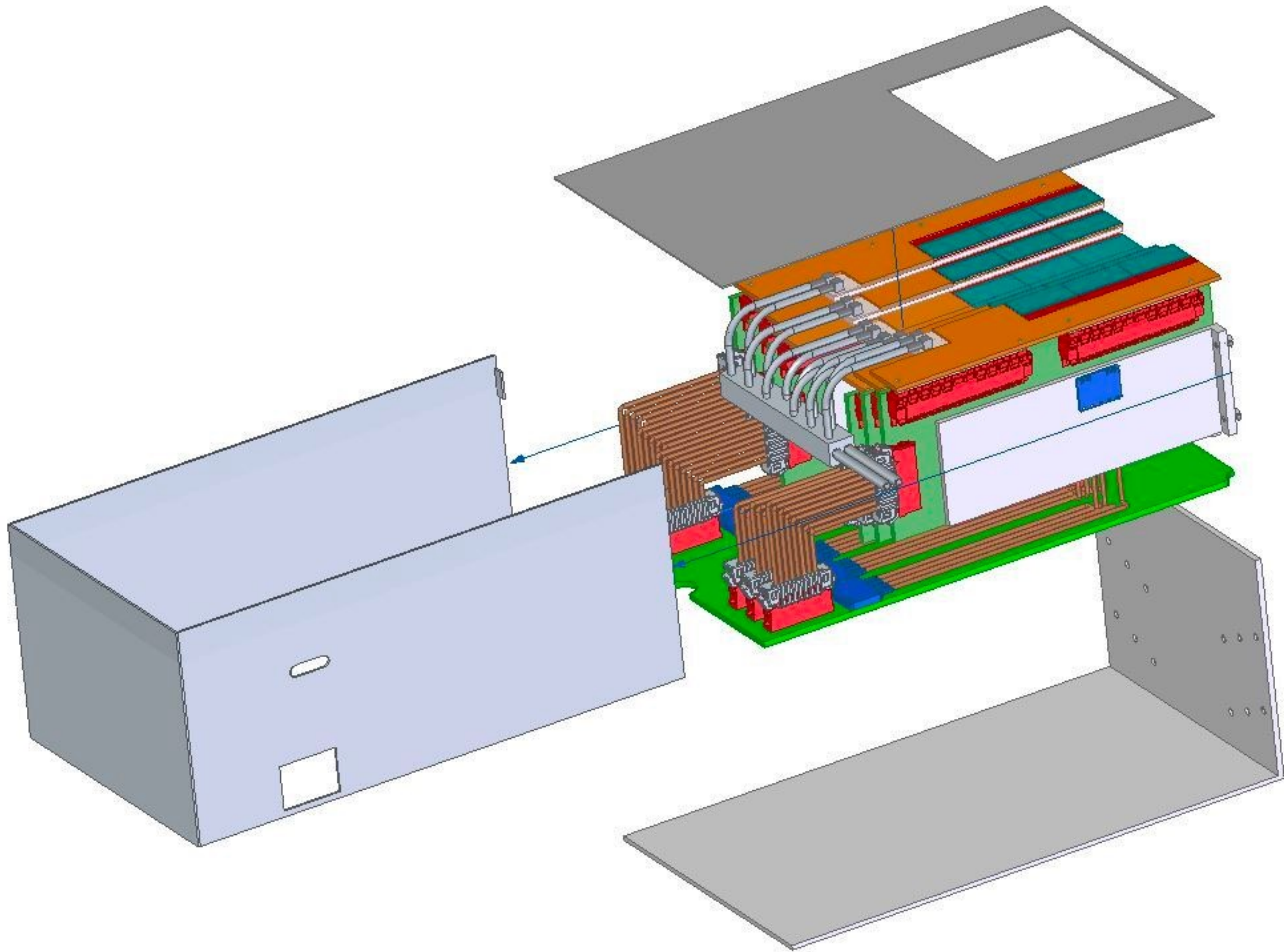
1152

Balcony	Active Area	Active Area	Active Area	Active Area	Active Area	Active Area	Balcony
Balcony	Active Area	Active Area	Active Area	Active Area	Active Area	Active Area	Balcony
Balcony	Active Area	Active Area	Active Area	Active Area	Active Area	Active Area	Balcony

Front view

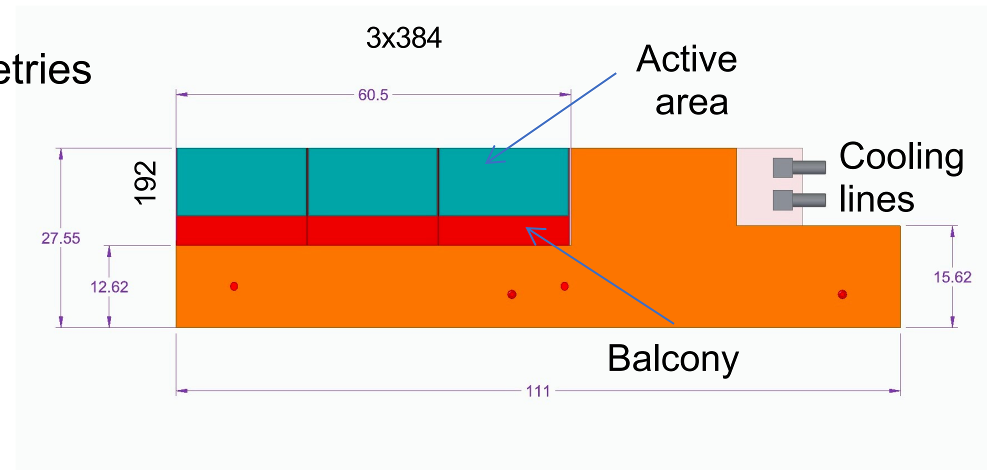
- Shingled assembly to maximize fill factor
- Overall dimensions compatible with requirements

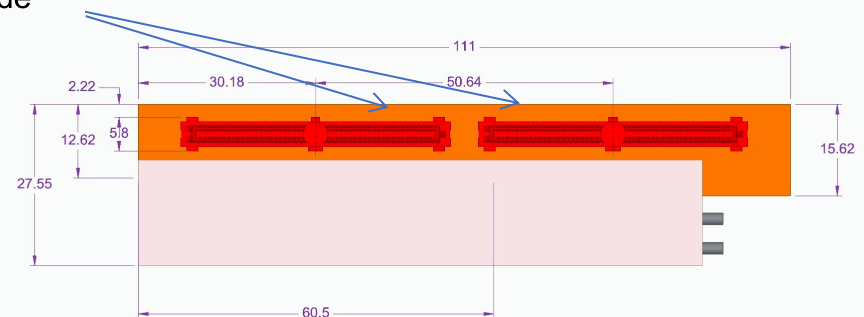




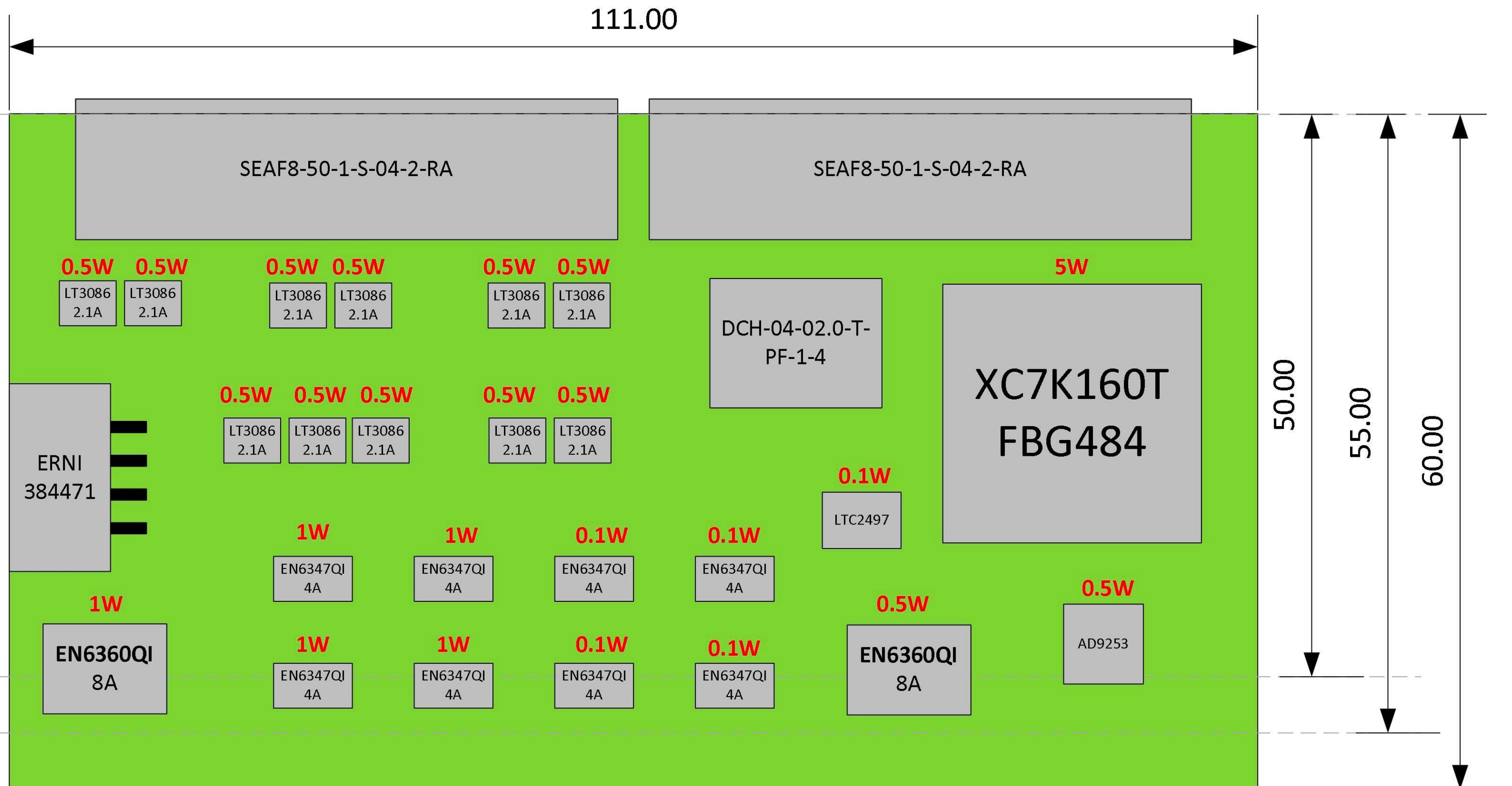
Rigid to flex boards + power cable

- Shingle unit based on current ASIC geometries
- 3 ROIC + ePixM matrix per tile
- Flex circuit
  - transmit control and data signals
  - SAM8 connector family
- Independent power path
  - 24W
  - Connector
    - 3 pins for analog
    - 2 pins for digital
    - >6A/pin
    - Solution
      - ERNI 214356

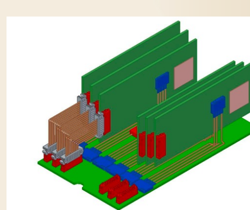




Concentrator card



Motherboard
Data & Power backplane card



30G bps

30G bps

30G bps

30G bps

30G bps

30G bps

FPGA HBM
(XCVU31P-1FSVH1924E)

12x 25Gpbs

Power In

DCDC converters

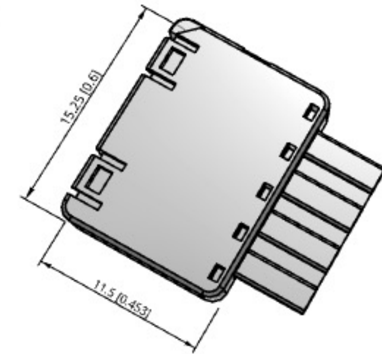
98

170

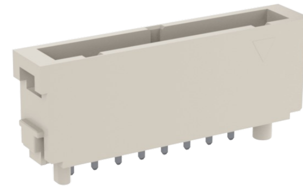
Mother board

- Data connector

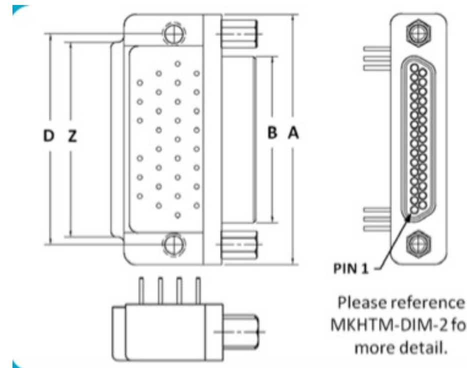
•DCH-04-04.0-T-PF-1-1



- Power connector (to concentrator cards)
- Part-No. 109939



- Input power connector



- DCDC regulator
  - RAA210610
  - 48V to 6.5V
  - 15A

Power up sequence

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- The recommended power-on sequence to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on is
- VCCINT,
- VCCINT_IO/VCCBRAM,
- VCCAUX/VCCAUX_IO, and
- VCCO
- If VCCINT and VCCINT_IO/VCCBRAM have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously.
- VCCINT_IO must be connected to VCCBRAM.
- If VCCAUX/VCCAUX_IO and VCCO have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously.
- VCCAUX and VCCAUX_IO must be connected together.
- VCCADC and VREF can be powered at any time and have no power-up sequencing requirements.

Power up sequence

SLAC

- For devices with HBM, the HBM power supplies can be powered on/off after or in-parallel with the core power supplies.
- The required power-on sequence is
  - VCCAUX_HBM and VCCINT_IO followed by
  - VCC_HBM/VCC_IO_HBM. VCC_IO_HBM must be connected to VCC_HBM. VCCAUX_HBM must be equal to or higher than VCC_HBM at all times. The recommended power-off sequence is the reverse of the power-on sequence.

Power up sequence

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The recommended power-on sequence to achieve minimum current draw for the GTY or GTM transceivers is

VCCINT,

VCCINT_GT,

VMGTAVCC,

VMGTAVTT

OR

VMGTAVCC,

VCCINT,

VCCINT_GT,

VMGTAVTT.

There is no recommended sequencing for VMGTVCCAUX.

Both VMGTAVCC and VCCINT can be ramped simultaneously.

When VCCINT and VCCINT_GT have the same recommended operating conditions, VCCINT and VCCINT_GT can be connected to the same power regulation circuit.

When VCCINT and VCCINT_GT are connected to separate regulation circuits, VCCINT_GT must be within the recommended operating condition before device configuration.

https://www.xilinx.com/support/documentation/data_sheets/ds923-virtex-ultrascale-plus.pdf

- Question
  - What do I do with Vbatt

Settings

Device	
Family	Virtex UltraScale+
Device	XCVU31P
Package	FSVH1924
Speed Grade	-1
Temp Grade	Extended
Process	Typical
Voltage ID Used	
Characterization	Production (± 15% accuracy)

Total On-Chip Power	13.9 W	
Junction Temperature	33.7 °C	
Thermal Margin	66.3°C	101.0W
Effective ΘJA	0.6 °C/W	

Power Supply

Source	Voltage	Total (A)
V_{CCINT}	0.850	3.494
V_{CCINT_IO}	0.850	0.537
V_{CCBRAM}	0.850	0.015
V_{CCAUX}	1.800	0.368
V_{CCAUX_IO}	1.800	0.012
V_{CCO} 3.3V	3.300	
V_{CCO} 2.5V	2.500	
V_{CCO} 1.8V	1.800	
V_{CCO} 1.5V	1.500	
V_{CCO} 1.35V	1.350	
V_{CCO} 1.2V	1.200	
V_{CCO} 1.0V	1.000	
$V_{CC_IO_HBM}$	1.200	0.307
V_{CC_HBM}	1.200	0.320
V_{CCAUX_HBM}	2.500	0.016
-		
$MGTYV_{CCAUX}$	1.800	0.285
$MGTYAV_{CC}$	0.900	2.629
$MGTYAV_{TT}$	1.200	5.042
-		
V_{CCADC}	1.800	0.008
-		

1		2			
VCCINT	0.85	VCCAUX_HBM / VCCINT_IO	2.5 / 0.85	VCCINT,	0.85
VCCINT_IO/VCCBRAM	0.85	VCC_HBM/VCC_IO_HBM	1.2	VCCINT_GT	0.85
VCCAUX/VCCAUX_IO	1.8			VMGTAVCC	0.9
VCCO				VMGTAVTT	1.2
VCCADC and VREF	1.8/1.25				
MGTYVccaux	1.8				

Notes

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- VCCINT_IO must be connected to VCCBRAM.
- For VCCO_0, the minimum recommended operating voltage for power on and during configuration is 1.425V. After configuration, data is retained even if VCCO drops to 0V.
- Includes VCCO of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HD I/O only) at ±5%, and 3.3V (HD I/O only) at +3/–5%.
- VCCAUX_IO must be connected to VCCAUX.
- If battery is not used, connect VBATT to either GND or VCCAUX.
- Each voltage listed requires filtering as described in the *UltraScale Architecture GTY Transceivers User Guide* (UG578) or the *UltraScale FPGAs*
- *GTM Transceivers User Guide* (UG581).

Implemented

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- VCCINT 0.85V @ 8A
  - When VCCINT and VCCINT_GT have the same recommended operating conditions, VCCINT and VCCINT_GT can be connected to the same power regulation circuit.
  - R_A = 48,400*6.5 = 314,600 => 316k
  - R_B = (0.6*316,000) / (0.85-0.6) = 758.4k=>750k

- $MGTYAV_{TT}$ 1.2V @ 8A
  - R_A = 48,400*6.5 = 314,600 => 316k
  - R_B = (0.6*316,000) / (1.2-0.6) = 316k

$R_A\,[\Omega] = 48{,}400 \times V_{IN}\,[V]$

$R_B[\Omega] = (V_{FB} \times R_A) / (V_{OUT} - V_{FB})\,[V]$

V_{FB} = 0.6V nominal

*Round R_A & R_B to closest standard value

$C_A\,[F] = 3.83 \times 10^{-6} / R_A\,[\Omega]$

*Round C_A down to closest standard value

R1 = 15kΩ

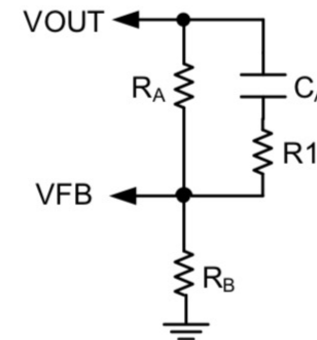
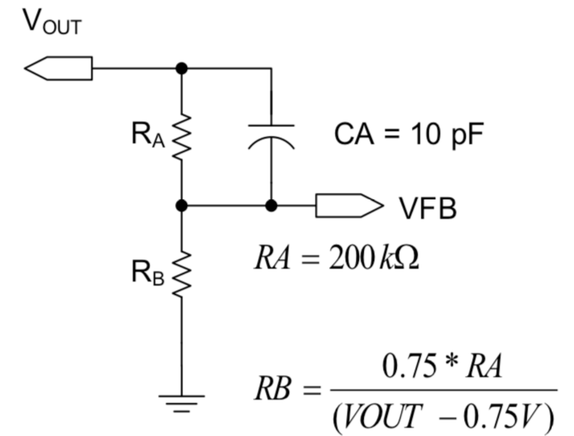


Figure 6: External Feedback/Compensation Network

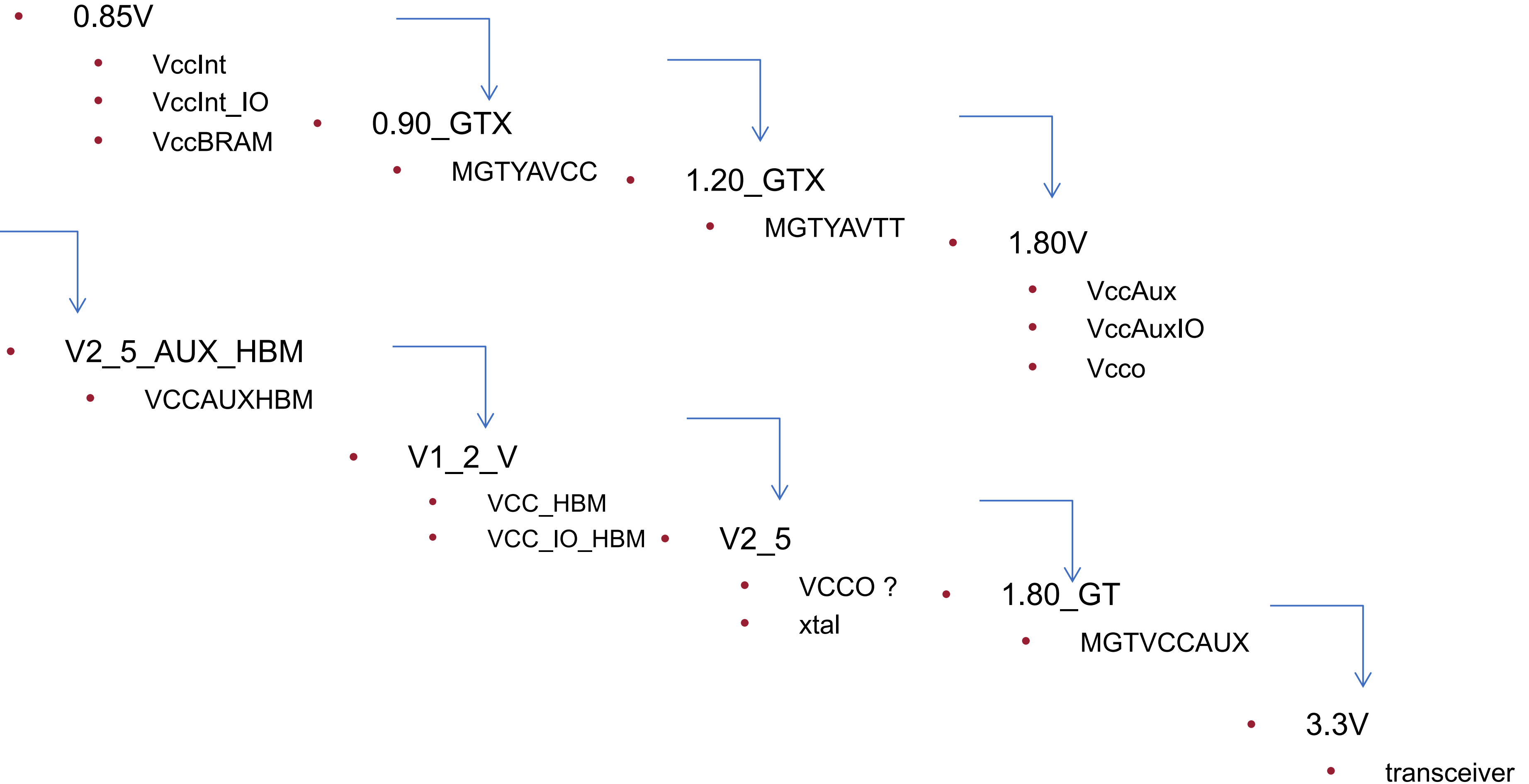
Implemented

- MGTYAV$_{cc}$ 0.9V @ 4A
  - R_A = 200k
  - R_B = (0.75*200,000) / (0.9-0.75) = 1M



Power up sequence implemented ds923-virtex-ultrascale-plus.pdf

SLAC



Power up decoupling

ug583-ultrascale-pcb-design.pdf and ug578

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- 0.85V
  - VccInt
  - VccInt_IO
  - VccBRAM
- 0.90_GTX
  - MGTYAVCC
- 1.20_GTX
  - MGTYAVTT
- 1.80V
  - VccAux
  - VccAuxIO
  - Vcco
- V2_5_AUX_H
  - MGTVCCAUX
- V2_5_AUX_HBM
  - VCCAUXHBM
- V1_2_V
  - VCC_HBM
  - VCC_IO_HBM
- V2_5
  - VCCO ?
  - xtal
- 1.80_GT
  - MGTVCCAUX
- 3.3V
  - transceiver

Power input

Name	LDO Voltage (V)	Power (W)	Input (V)	Current (A)	Supply current (A)	Return current (A)
AVDD2V5	2.5	14.4	6.5	2.461538462	2.5	2.5
AVDD1V8	1.8	10.35	6.5	1.769230769	1.8	1.8
DVDD2V5	2.5	4.5	6.5	0.769230769	1.8	1.8
DVDD_FPGA	NA	5	6.5	1		
HV	120	mW	120	uA	uA	NA

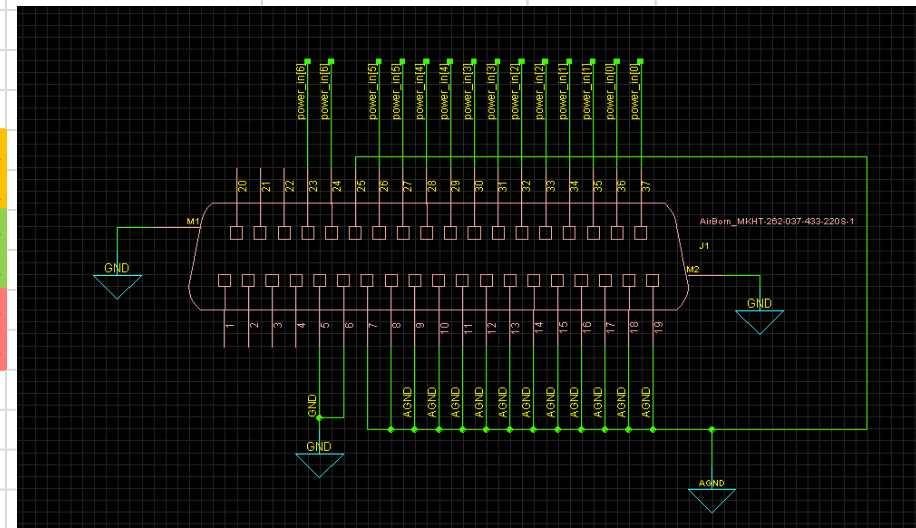
Assuming 0.5V LDO dropout voltage

Assuming 5W FPGA power

Assuming 50% more current need for the AVDD1V8 with high signal

Mother board 48V DCDCs

Name	Output (V)	Output (A)	Input (V)	Input (A)
AVDD_2V5_1	6.5	7.5	48	1.128472222
AVDD_2V5_2	6.5	7.5	48	1.128472222
AVDD_1V8_1	6.5	5.4	48	0.8125
AVDD_1V8_2	6.5	5.4	48	0.8125
DVDD_2V5_1	6.5	5.4	48	0.8125
DVDD_2V5_2	6.5	5.4	48	0.8125

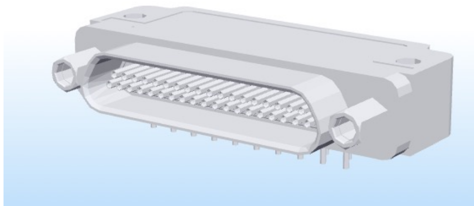


PCB mount and cable mount cables

MKHT-262-037-433-220S

High Temperature, Right Angle Plated Thru Hole PCB Connector with a Narrow Footprint (RECEPTACLE)

MKHT26, 36, 46, High Temperature Right Angle Plated Thru Hole (PTH) with a Narrow Footprint, Receptacle, 2, 3, 4-Row, Sizes: 9-100 | M Series

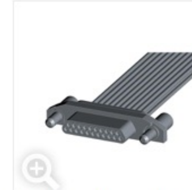


Max 600V
I/contact 3A max

Distributor	Available Inventory	Last Updated
Powell Electronics, Inc. 200 Commodore Dr. Swedesboro, New Jersey 08085 United States (800) 235-7880 airborninfo@powell.com	25	6/19/2020

MTHT-212-037-161-415R
Normally not stocked since we need to tell them what the cable length required.

MTHT-212-037-161-415R



High Temperature Cable Connector, Low Profile with Radius (PLUG)

MTHT-21, 31, High Temperature Cable Connector with a Low Profile and Radius, Plug, 2, 3-Row, Sizes: 9-51 | M Series

A family of high temperature low profile male cable connectors that have 2 and 3 rows of contacts spaced at 0.050". These connectors can be located along concave surfaces such as the inside wall of a tube/pipe. They are available in sizes ranging from 9 to 51 contacts.

Vin 48V
I/supply (2 wires) <1A
Wire thickness is 26AWG

Max length of 120" (3m)
Max drop per wire of 0.4V

Voltage Drop Calculator

Result

Voltage drop: 0.40
Voltage drop percentage: 0.84%
Voltage at the end: 47.6

Please note that the result is an estimation based on normal conditions. The actual voltage drop can vary depending on the condition of the wire, the conduit being used, the temperature, the connector, the frequency etc. But, in most cases, it will be very close.

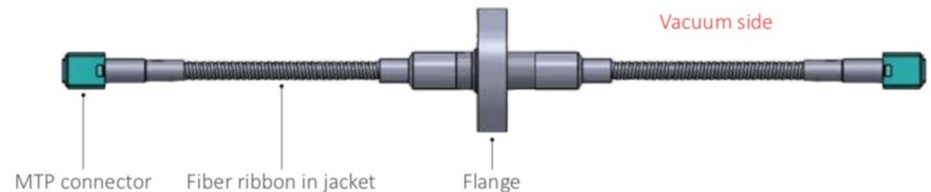
Wire Material	Copper
Wire Size	26 AWG (0.254 kcmil)
Voltage	48
Phase	DC
Number of conductors	2 conductors per phase in parallel
Distance*	3 meters
Load current	1 Amps

https://www.calculator.net/voltage-drop-calculator.html?material=copper&wiresize=133.9&voltage=48&phase=dc&noofconductor=2&distance=3&distanceunit=meters&eres=1&x=71&y=20

Fiber optics cable and vacuum feedthough

https://www.fs.com/products/69995.html

RETA-RIB-CF40-12-050a-2-S48-11b



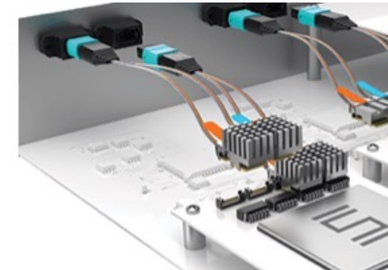
https://www.lasercomponents.com/fileadmin/user_upload/home/Datasheets/sedi/fibre-optic-ribbon-hermetic-feedthroughs.pdf

Mother board FPGA and transceivers

SLAC

- FPGA
  - Xilinx Kintex Ultrascale plus
    - 2 FPGS / data module ($)
      - Enable the use of DDR4
      - Capable of implementing simple data reduction
      - Uses full camera size, consumes more power
    - 1 FPGA per data module ($)
      - No DDR4 memory
      - Control camera and routes data through
    - FPGA + HBM (3D) ($$$)
      - 8GB HBM (BW 460GB/s)
      - Capable of image processing
- Transceiver
  - Amphenol
    - 300 Gbps (12 x 25Gbps), 25 x 25 mm
    - https://www.amphenol-icc.com/product-series/leap-on-board-transceiver.html
    - **Meeting with them 7/14**
  - Samtec
    - Up to 28 Gbps (x4 modules)
    - **NDA pending**

leap-on-board

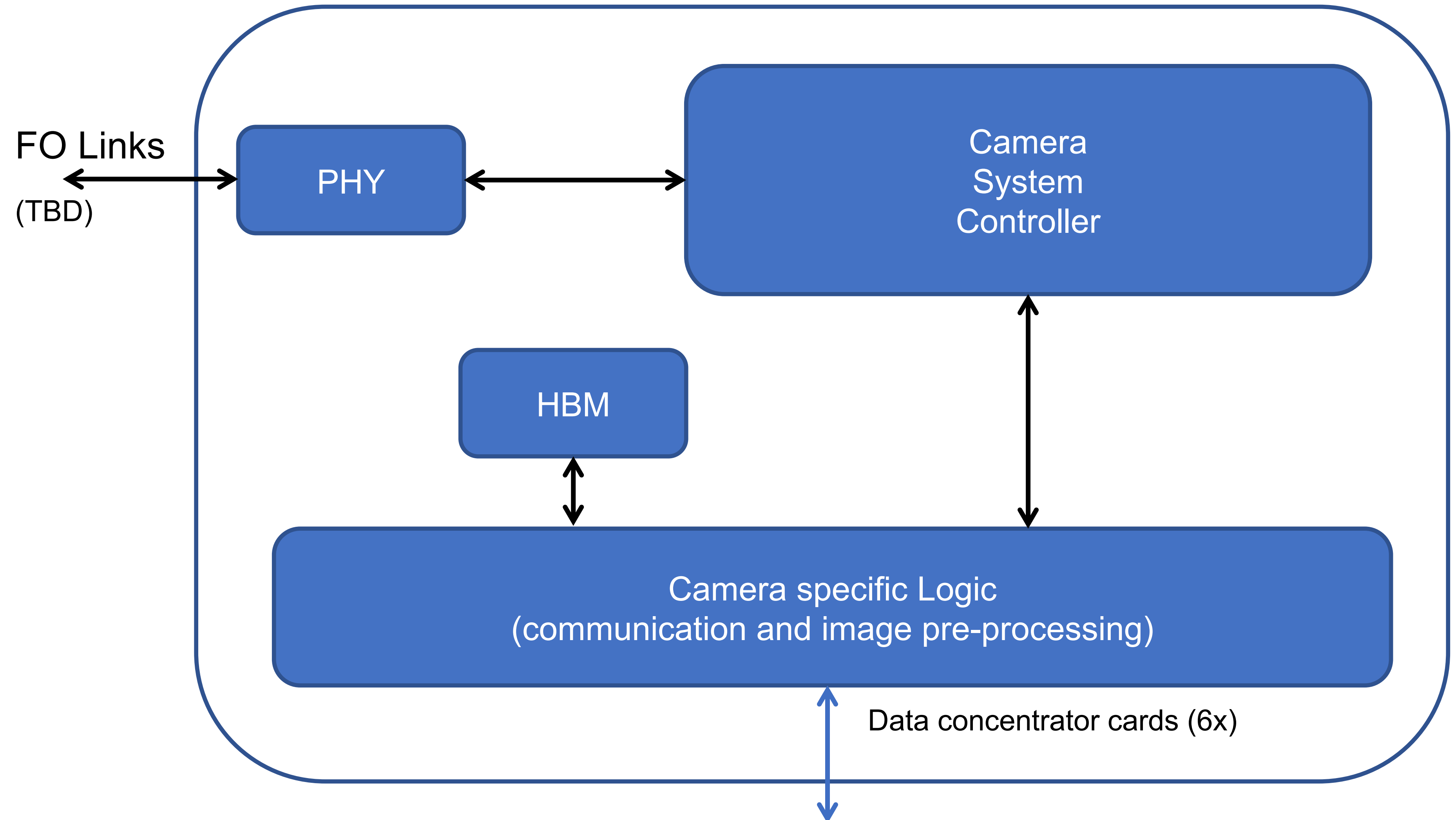


Pending NDAs

Next steps

- Take a decision on which transceiver we will use
  - Amphenol vs. Samtec
- Build schematic parts for new components
- Start working on MB schematic and parts placement (next week) with Tung

Firmware structure – MB Top Level Design



Single concentrator current per contact

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Name	LDO Voltage (V)	Power (W)	Input (V)	Current (A)	Supply current (A)	Return current (A)
AVDD2V5	2.5	27	6.5	4.615384615	4.7	4.7
AVDD1V8	1.8	6.9	6.5	1.179487179	1.2	1.2
DVDD2V5	2.5	9	6.5	1.538461538	2.6	2.6
DVDD_FPGA	NA	5	6.5	1		
HV	120	mW	120	uA	uA	NA

Assuming 0.5V LDO dropout voltage

Assuming 5W FPGA power

Mother board 48V DCDCs					
Name	Output (V)	Output (A)	Input (V)	Input (A)	
AVDD_2V5_1	6.5	4.7	48	0.707175926	
AVDD_2V5_2	6.5	4.7	48	0.707175926	
AVDD_2V5_3	6.5	4.7	48	0.707175926	
AVDD_2V5_4	6.5	4.7	48	0.707175926	
AVDD_2V5_5	6.5	4.7	48	0.707175926	
AVDD_2V5_6	6.5	4.7	48	0.707175926	
AVDD_1V8_1	6.5	7.2	48	1.083333333	→ Split into two
DVDD_2V5_1	6.5	7.8	48	1.173611111	→ Split into three
DVDD_2V5_2	6.5	7.8	48	1.173611111	

Motherboard
Data & Power backplane card

Power
Power
Power
30G bps
30G bps
30G bps
30G bps
FPGA HBM (XCVU31P-1FSVH1924E)
12x 25Gpbs
300Gbps Leap On Trans.
Power
Power
Power
30G bps
30G bps
Power In
Power In
70mm
165mm
DCDC converters

Power connector

https://www.erni.com/fileadmin/user_upload/Downloads/Products/MicroBridge/MicroBridge-EN.pdf

CAPABILITIES

Male connector
right angle or
vertical -
Female connector
90° cable outlet

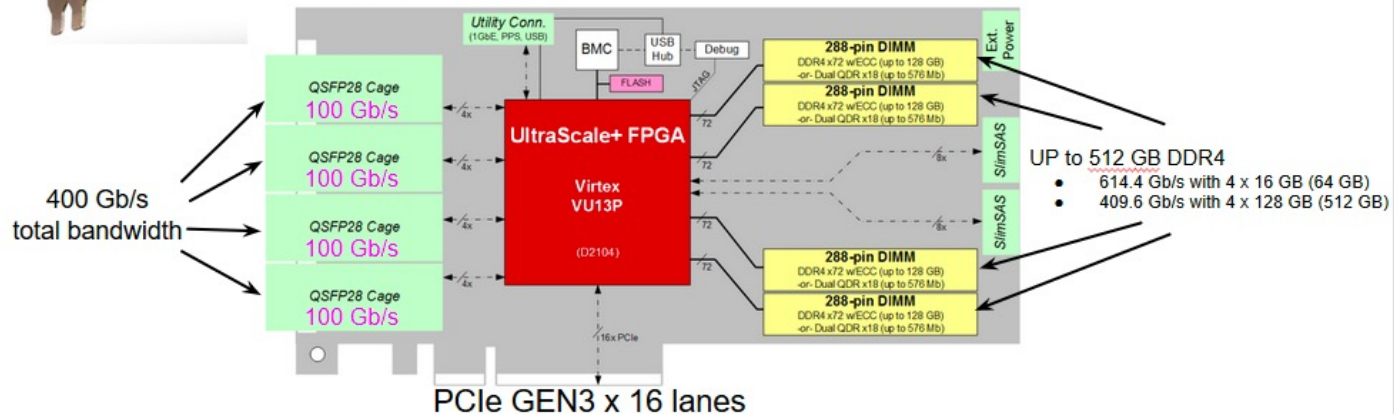
DAQ COTS FPGA

COTS FPGA PCIe DAQ Card: BittWare XUP-VV4

Active or Passive Cooling Options

Device Name	VU13P
System Logic Cells (K)	3,780
CLB Flip-Flops (K)	3,456
CLB LUTs (K)	1,728
Max. Dist. RAM (Mb)	48.3
Total Block RAM (Mb)	94.5
UltraRAM (Mb)	360.0
DSP Slices	12,288

Type	Size	Speed (MTPS)
DDR4 RDIMM VLP	16GB	2400
DDR4 RDIMM	32GB	1866
DDR4 LRDIMM	32GB	2400
DDR4 LRDIMM	64GB	2133
DDR4 RDIMM	128GB	1600
QDR-II+ Q2XDM2	2x 288Mbit	550 MHz



PCIe GEN3 x 16 lanes

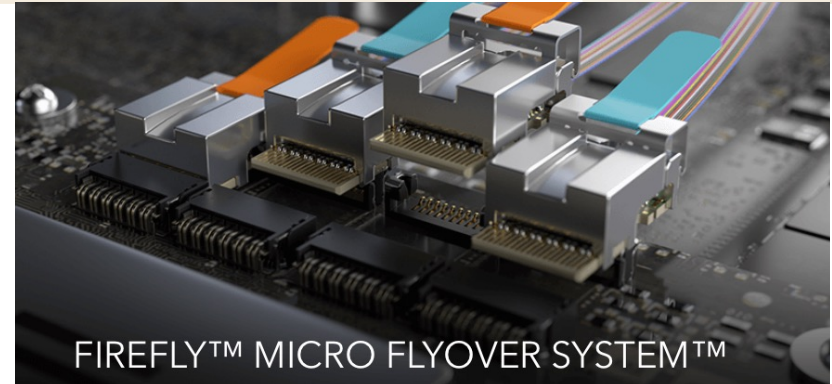
https://www.bittware.com/fpga/xup-vv4/

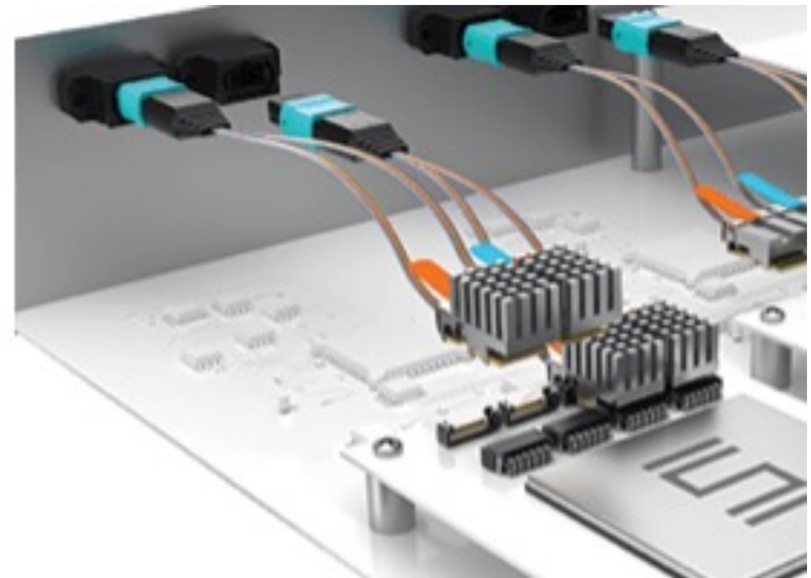
11

xup-vv8 has 8 input and could be used for mm to sm conversion on the 300Gbps option

FireFly fo SAMTEC

- Transceiver of upto 28Gbps





SLAC

Power considerations

ASIC characteristics

SLAC

1 ASIC

- Power supply voltage level
  - 2.5V @ 4A
  - 1.8V @1A
- Power supply coupling requirements
- LVDS
  - 24 data transmission per ASIC
  - 1 clock receiver
- single ended
  - 17 control lines inputs and output
  - 1 x Analog monitor

3 ASICs

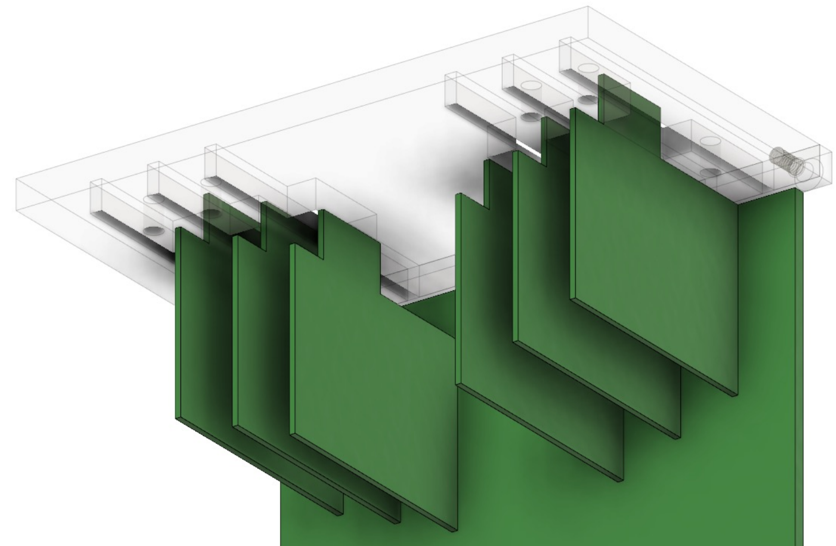
- Power supply voltage level
  - 2.5V @ 12A
  - 1.8V @ 3A
- Power supply coupling requirements
- LVDS
  - 72 data transmission per module
  - 3 clock receiver
- single ended
  - 20 control lines inputs and output
  - 3 x Analog monitor

18 ASICs

- Power supply voltage level
  - 2.5V @ 72A
  - 1.8V @ 18A
- Power supply coupling requirements
- LVDS
  - 432 data transmission per camera
  - 6 clock receiver
- single ended
  - 68 control lines inputs and output
  - 18 Analog monitor

Power consideration

- The estimate is 200W of power (ASICs)
  - @6V : 33.3A
  - @12V: 16.6A
  - @24V: 8.3A
- Separate power from signal (flex)
  - Use power connectors with independent cable
- Implementation
  - Power backplane
    - Power to ASIC + data modules
  - Power "fins"
    - 3 ASICs per fin



Questions about power limits

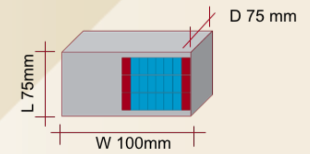
- The proposed camera consumes
  - at the ASIC level 200W
  - At the FPGA level 50W (estimated)

- What is driving the parameter for the requested power limits?
  - What are the compromises that can be made here?
    - Array size?
    - Others

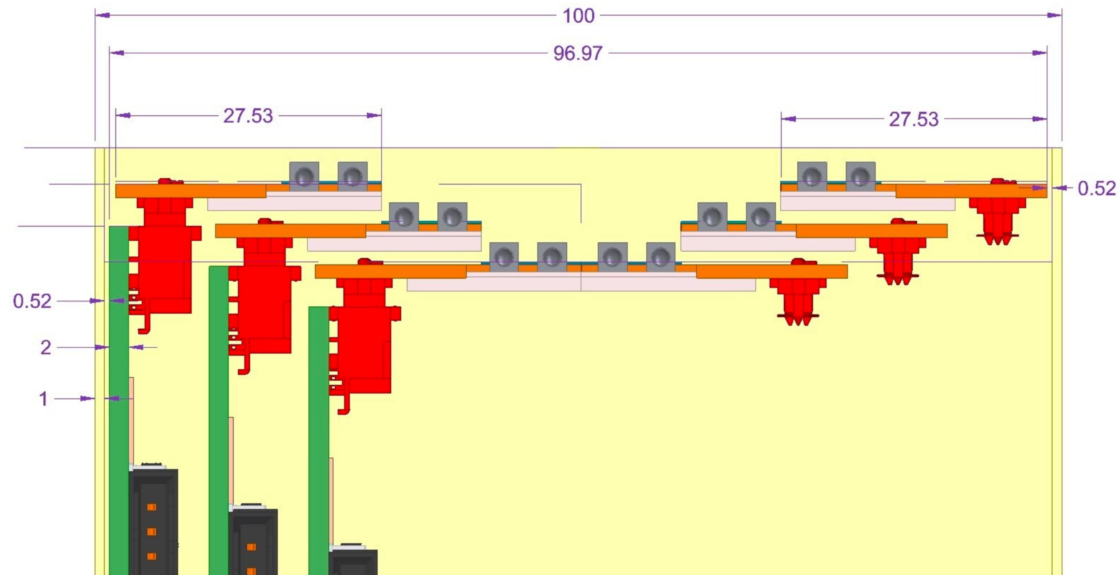
SLAC

Data considerations

Camera head mechanical simplified sketch

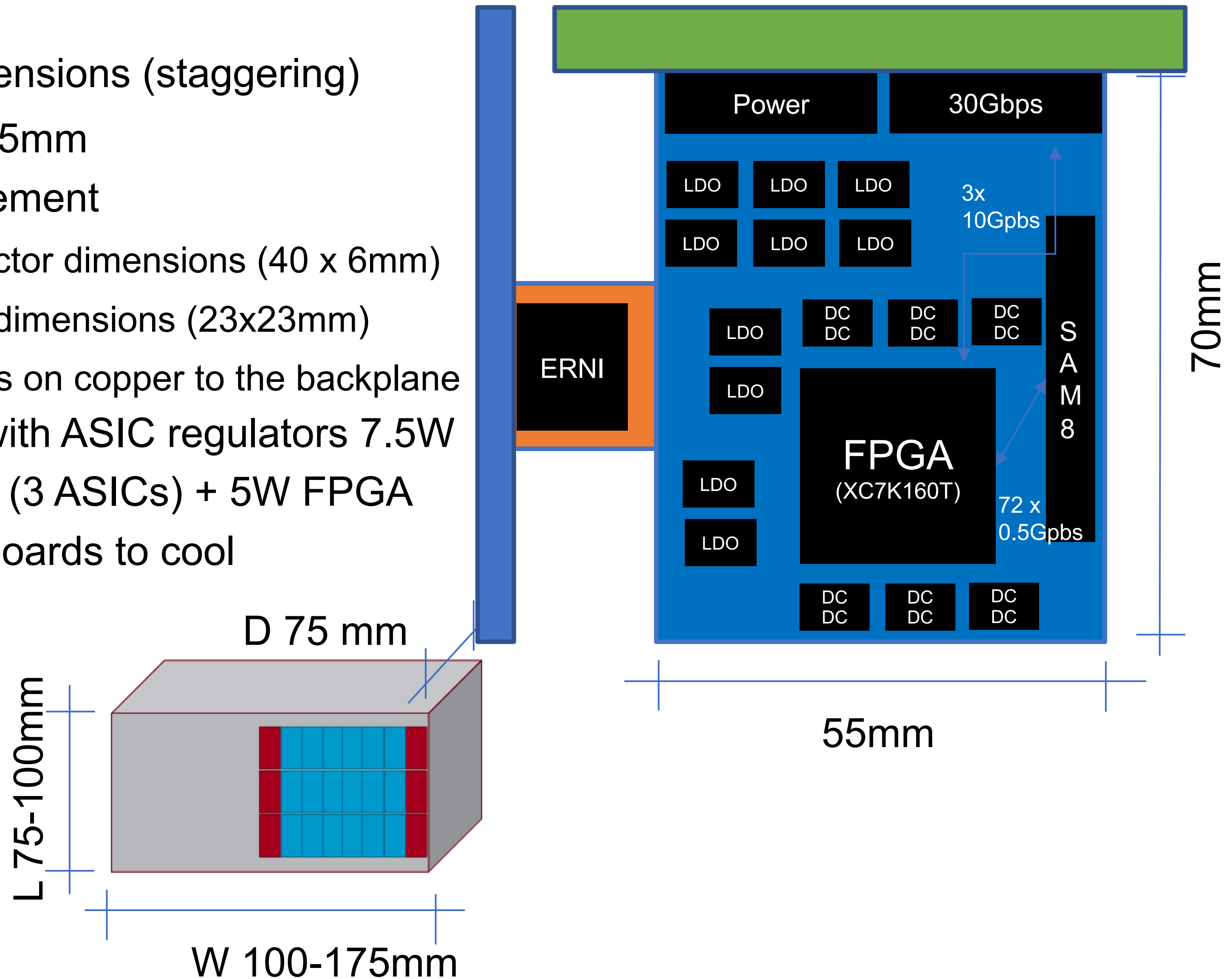


* ½ of the shingles are shown


100
96.97
27.53
27.53
0.52
0.52
2
1

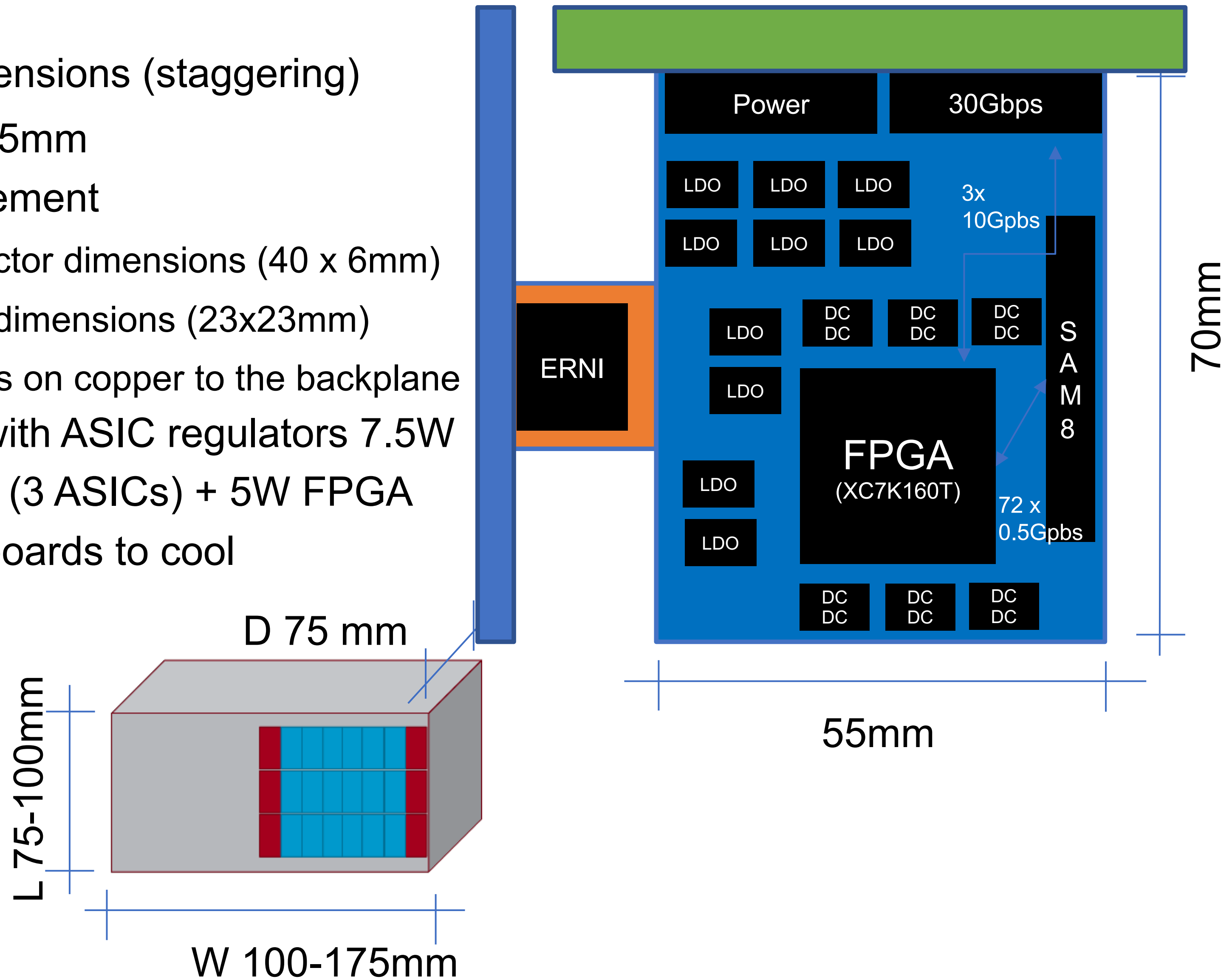
Data concentrator & ASIC power card

- Board dimensions (staggering)
  - 70 x 55mm
- Parts placement
  - Connector dimensions (40 x 6mm)
  - FPGA dimensions (23x23mm)
  - 30Gbps on copper to the backplane
- Combine with ASIC regulators 7.5W dissipation (3 ASICs) + 5W FPGA
- 6 vertical boards to cool



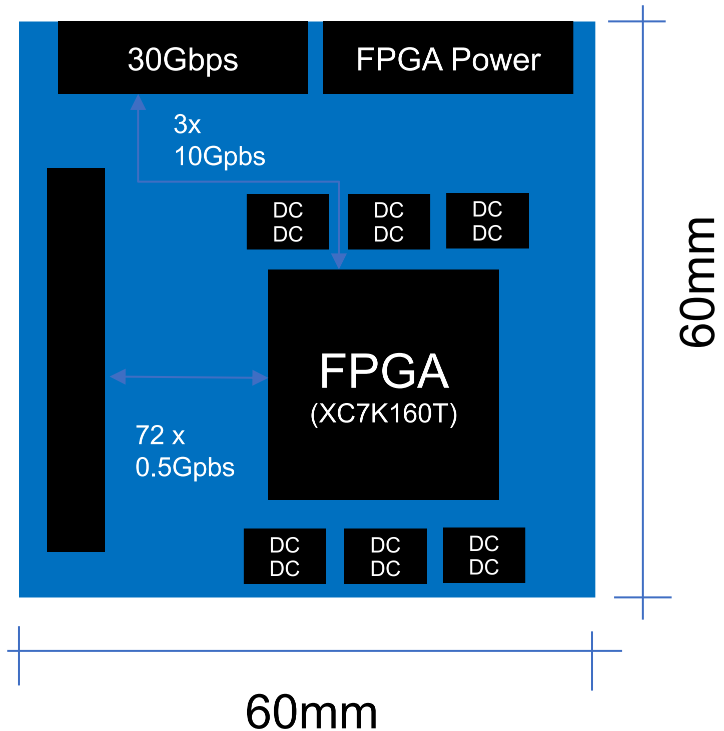
Data concentrator & ASIC power card

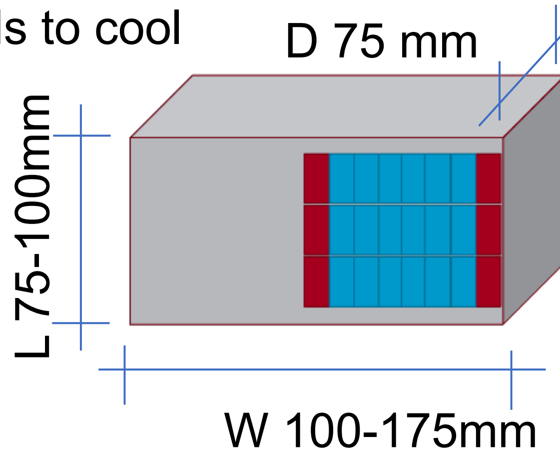
- Board dimensions (staggering)
  - 70 x 55mm
- Parts placement
  - Connector dimensions (40 x 6mm)
  - FPGA dimensions (23x23mm)
  - 30Gbps on copper to the backplane
- Combine with ASIC regulators 7.5W dissipation (3 ASICs) + 5W FPGA
- 6 vertical boards to cool



Data concentrator card

- Board dimensions
  - 60 x 60mm
- Parts placement
  - Connector dimensions (40 x 6mm)
  - FPGA dimensions (23x23mm)
  - 30Gbps on copper to the backplane
- FPGA power dissipation ~5W
- Separate power fin boards with ASIC regulators 7.5W dissipation (3 ASICs, 15A, 0.5V dropout LDO)
- 12 vertical boards to cool

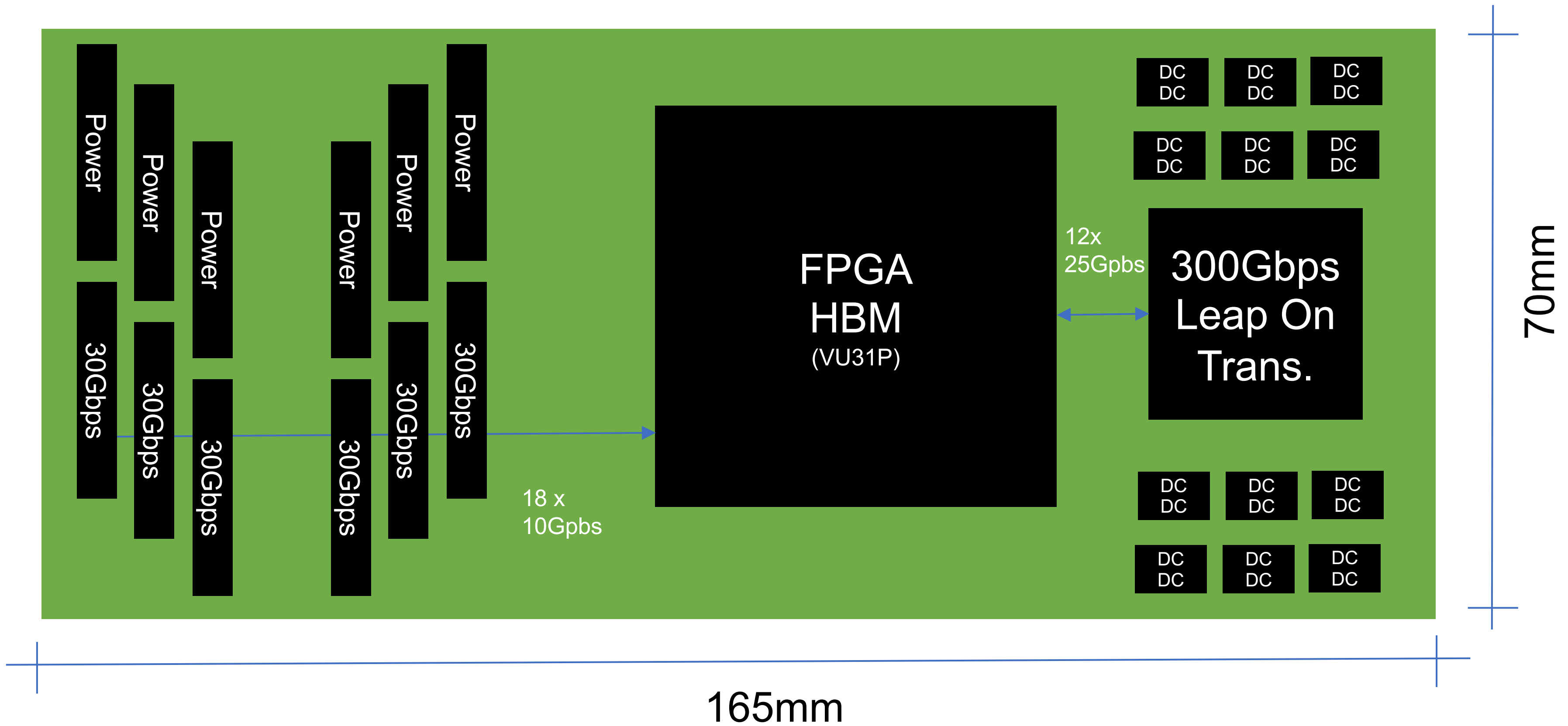




Data concentrator cards

- 6 data concentrator cards per camera
  - IO requirements (data into the camera)
    - 144 IO/module (24 x 2 IOs per line x 3 ASICs x 1 modules)
    - 23 IO/module for ASIC control
    - Analog monitoring ADC IOs
    - Digital monitoring IOs
  - Data volume at 7.5kFPS
    - **28Gbps/per data card** (384*192 pixels * 3 ASICs * 16 bits * 7.5kFPS, 66b/64b)
    - **84Gbps/per side** (384*192 pixels * 9 ASICs * 16 bits * 7.5kFPS, 66b/64b)
    - **168Gbps/per camera** (384*192 pixels * 18 ASICs * 16 bits * 7.5kFPS, 66b/64b)
  - Data transmission **200Gbps** out of the camera (8x25Gbps lanes)

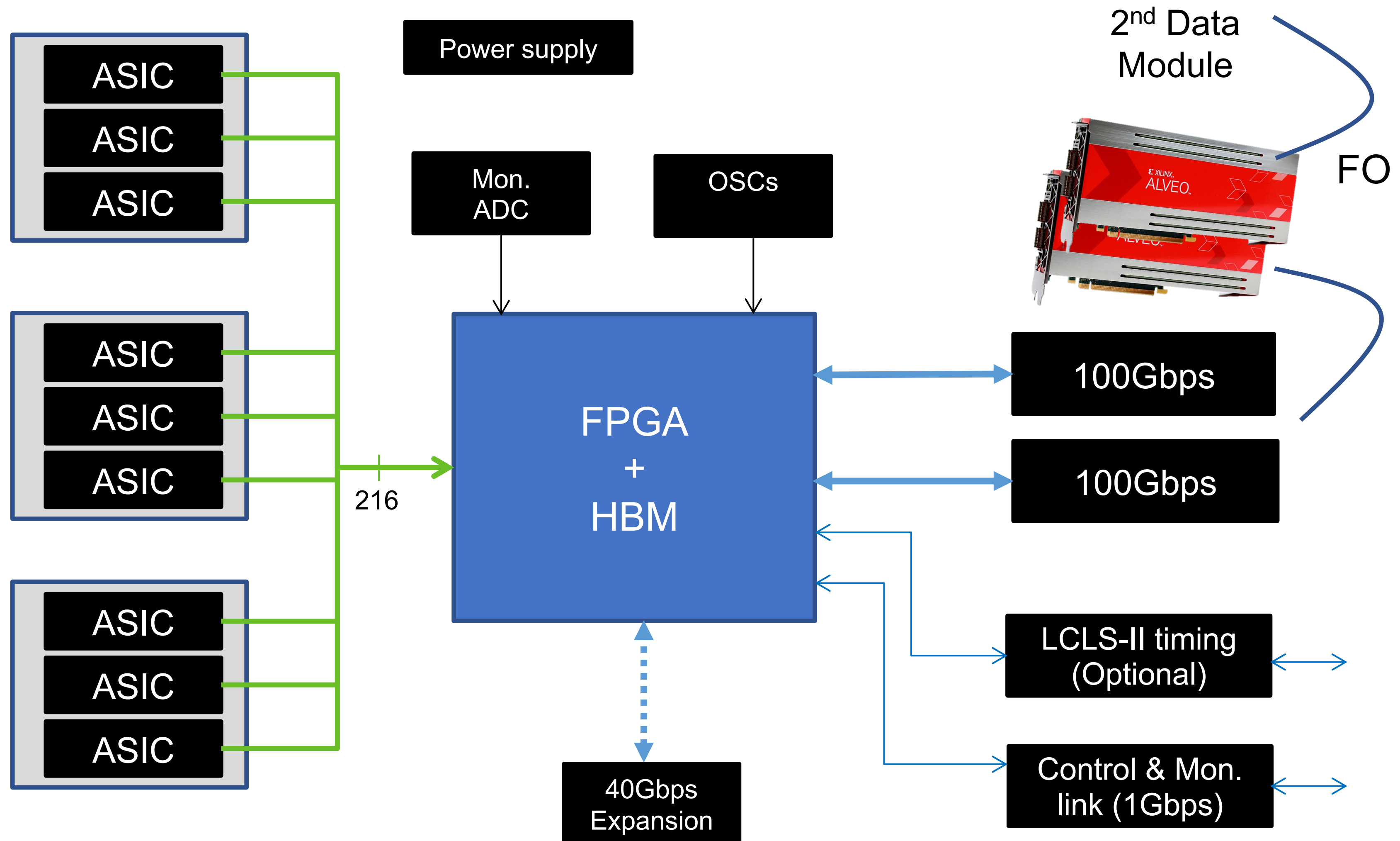
Data & Power backplane card



Data & Power backplane card

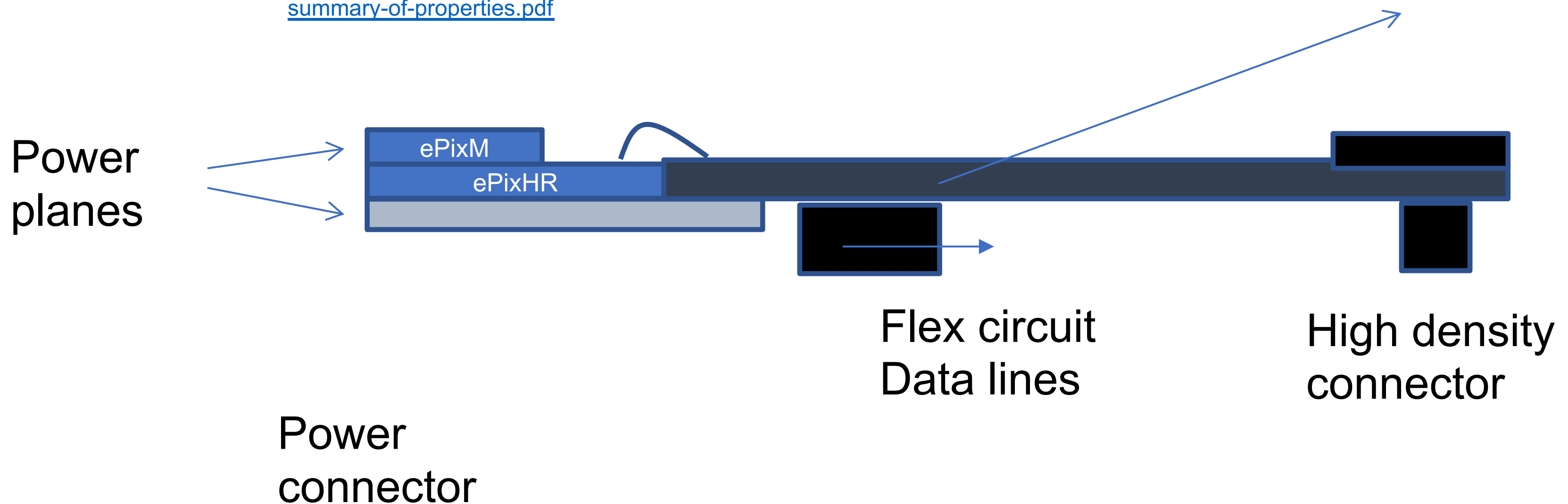
- Ultrascale+ Virtex with High Bandwidth Memory (4GB)
  - 45x45mm package
  - 32 x 32.75 Gbps transceivers
    - 18 used to capture data from concentrator boards (RX)
    - The TX lanes of the above 18 transceivers can be used to serialize ASIC controls (SACI, Acq, SRO, triggers etc) for simplified routing in between FPGAs
    - 12 used for 300 Gbps off camera link (full duplex)
- Two optical transceiver options
  - 12 lane Leap-On Amphenol
    - Compact 25.4x25.4mm
    - Fiber connector can exit in any direction (MTP pigtail)
    - 300Gbps full duplex
    - Multi-mode fiber only
  - 8 lane QSFP-DD (double density)
    - Larger footprint 88x19.25mm (26mm height, staged 2x QSFPs)
    - Fiber connector can exit only in directions parallel to the backplane board
    - 200Gbps full duplex (more than enough for 7.5kFPS)
    - Multi-mode and single-mode options (accepts standard QSFP modules)
- Multiple DCDCs for FPGA, Transceiver and ASIC 1st stage regulation

Camera data board



Chamber + outgassing considerations

- Board materials
  - FR4
    - Porous material
  - Polyimide
    - Has been used in camera that were installed in soft x-ray chambers
    - https://www.dupont.com/content/dam/dupont/products-and-services/membranes-and-films/polyimde-films/documents/DEC-Kapton-summary-of-properties.pdf



Feedthrough + outgassing considerations

- Manufacturer suggest Electron Beam welding, aluminum to aluminum
- For our tests
  - Evaluate mechanical stress on the 100Gbps
  - Use epoxy
  - Limit it to High Vacuum

Heat dissipation

- Thermal simulation should use fluid dynamics
  - That includes not only the inside of the material but all air/vacuum influences

DRP – Data reduction pipeline

- Can start at the camera level
- General algorithms may be used
  - Lossless compression
  - https://www.sciencedirect.com/topics/computer-science/lossless-compression
- Application specific algorithms may be at use
  - ROI (row, col data formatting + ROI corners)
  - Thresholding (dark subtraction, gain correction common mode correction?, plus threshold to select pixel)
  - Digital integration
  - Hit counting
  - clustering

SLAC

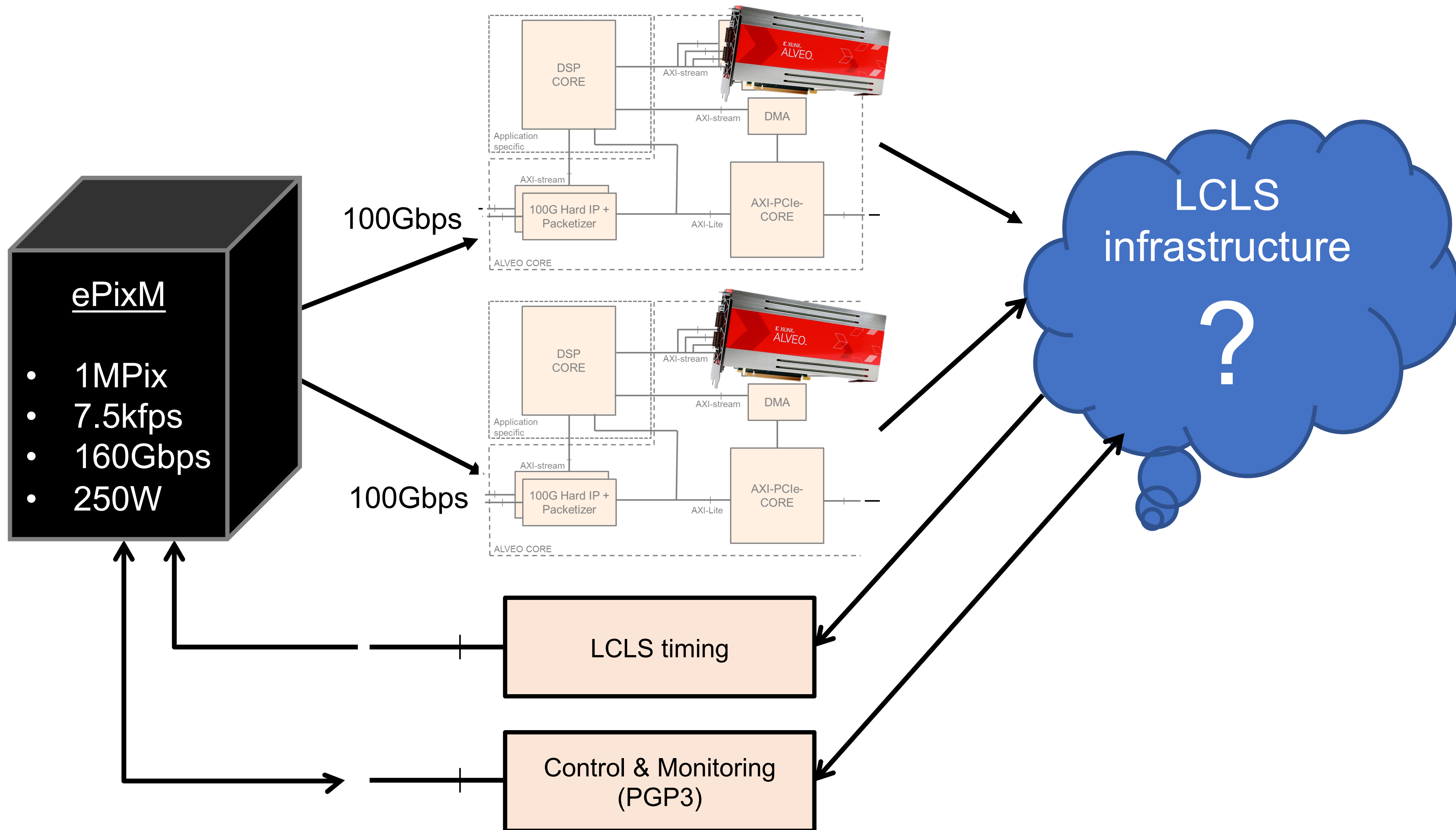
DAQ & Data considerations

Data interface card
DAQ A-U200-A64G-PQ-G

Off-chip Memory Capacity	64 GB
Off-chip Total Bandwidth	77 GB/s
Internal SRAM Capacity	35 MB
Internal SRAM Total Bandwidth	31 TB/s
PCI Express	Gen3x16
Network Interfaces	2x QSFP28 (100GbE)
Maximum Total Power	225W
Thermal Cooling	Passive/Active

Working with
Matt Weaver
Larry Ruckman
Ryan Herbst

Going beyond the camera



Project Scope & Deliverables

SLAC

- 1Mpix camera concept development including:
  - Mechanics (started)
  - Thermal dissipation (not started)
  - DAQ concept (started)
    - Power distribution (started)
    - Data streaming - vacuum to air (started)
    - Camera specific firmware (not started)

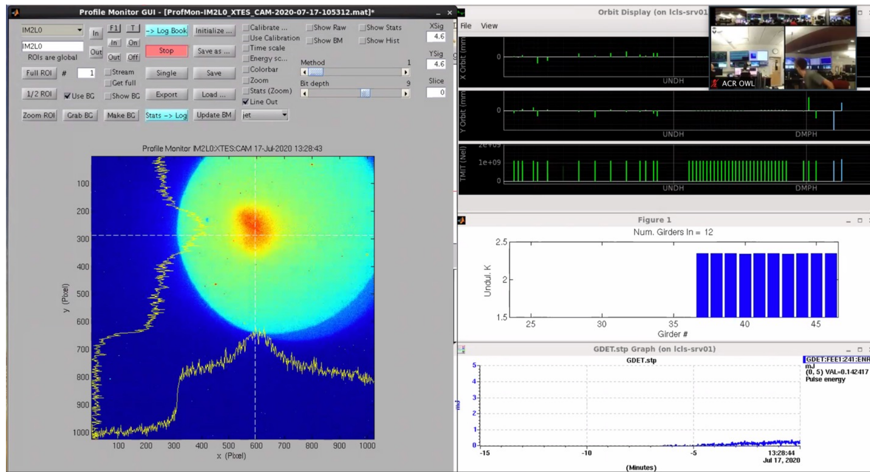
Deliverables:

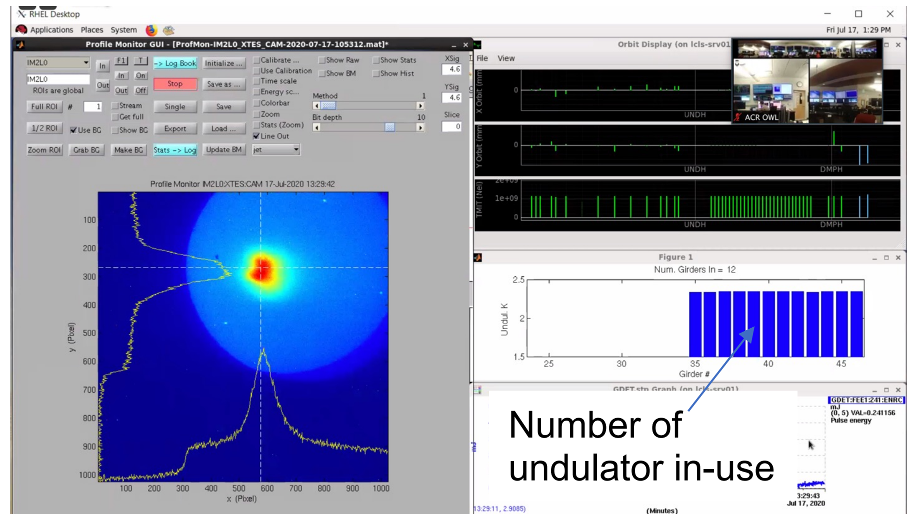
- ***Report documenting concept and risk analysis.***

First light at LCLS-II live

SLAC

- 07/17/2020

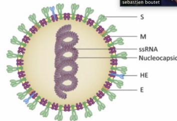




Science is coming up next

SARS CoV-2 Virus

- The CoV-2 virus is ~120 nm in diameter (1/1000 of a human hair)
- Composed of 28 unique proteins
- Potentially all the proteins are antiviral or vaccine targets
- Important protein targets include:
  - Spike: infection
  - NSP3: replication and immune response
  - NSP5: replication



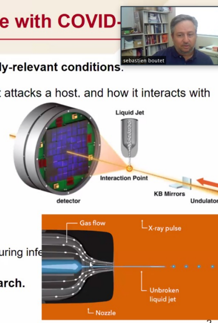
LCLS can study tiny crystals, shortening the time to assess drug targets, and ensuring they are in as "human-relevant" a condition as possible

LCLS can significantly help in the battle with COVID-

LCLS allows us to study the coronavirus under physiologically-relevant conditions.

This can more accurately reveal how the virus is structured, how it attacks a host, and how it interacts with potential drugs under relevant conditions.

Prior work at LCLS has studied proteins linked to coronavirus, Zika, dengue fever, tularemia, and African sleeping sickness.



Attributes of LCLS ultrafast diffraction:

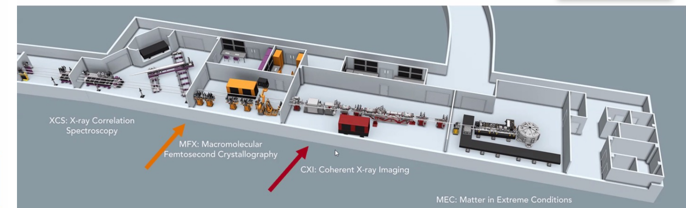
- Extremely small crystals (e.g. from the envelope protein)
- Room temperature and native-like membrane environments
- Potential to capture dynamic changes that viral proteins undergo during inf

Rapid access to LCLS will be prioritized for coronavirus research.

https://biology-lcls.slac.stanford.edu/

2

LCLS Instruments for Biology



- Instruments mainly unchanged from LCLS-I, major improvements in detectors
- Re-commissioning is a key step following first light

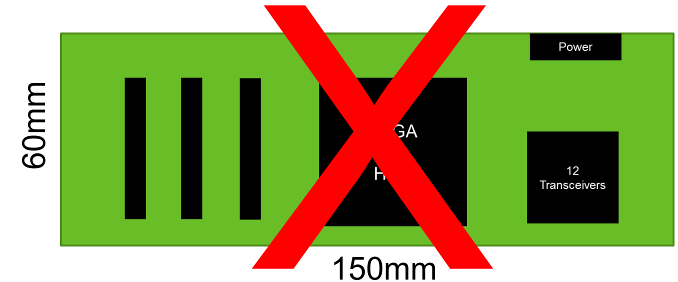
3

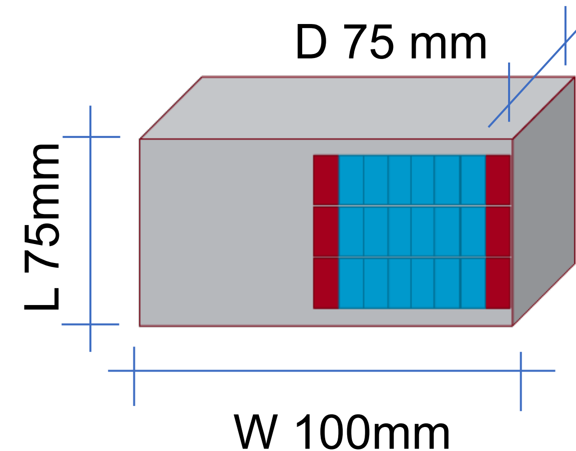
BACKUP slides

Metrology consideration

Data cards platform

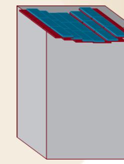
- FPGA
  - Xilinx Kintex Ultrascale plus
    - 2 FPGS / data module ($)
      - Enable the use of DDR4
      - Capable of implementing simple data reduction
      - Uses full camera size, consumes more power
    - 1 FPGA per data module ($)
      - No DDR4 memory
      - Control camera and routes data through
    - FPGA + HBM (3D) ($$$)
      - 8GB HBM (BW 460GB/s)
      - Capable of image processing





- Transceiver
  - 300 Gbps (12 x 25Gbps), 25 x 25 mm
  - https://www.amphenol-icc.com/product-series/leap-on-board-transceiver.html

Camera head sketch



TID-AIR SLAC

100mm

60mm

...

Cold plate

Power fins

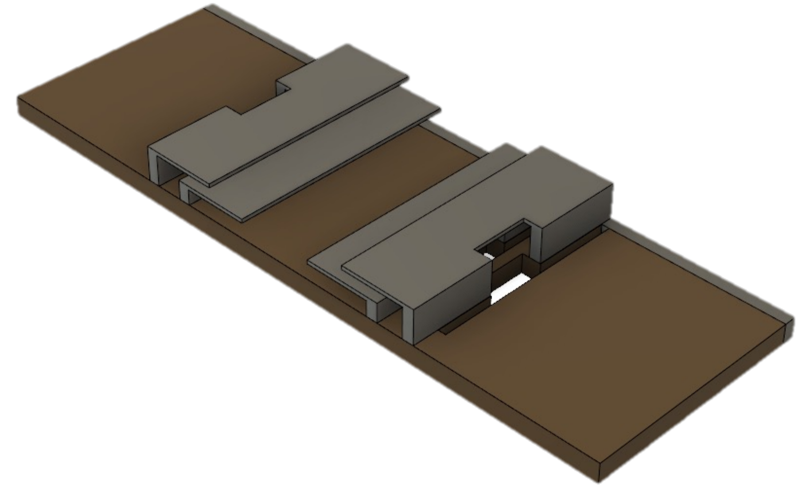
Data cards

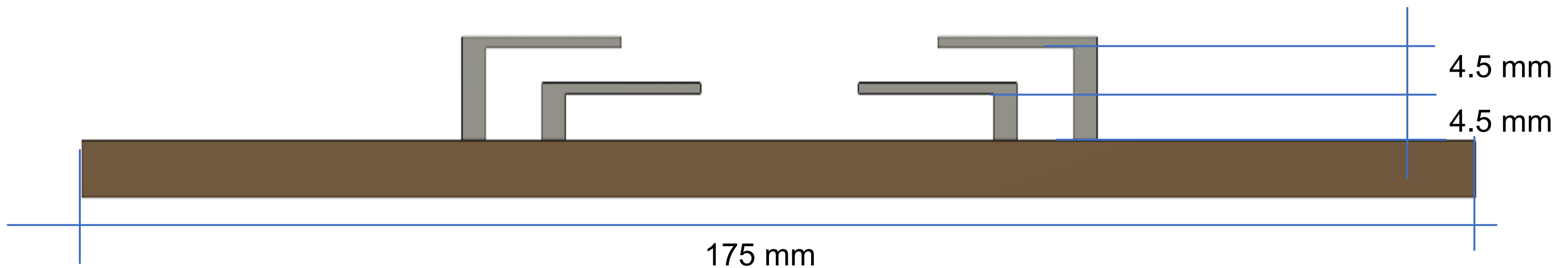
Power back plane

* ½ of the shingles are shown

Cold plate for the shingle

- Gap among fins are 4.5 mm
  - 1mm for fins base
  - 1mm for board
  - 1.5 mm for ASIC stack
  - 1 mm for wirebond
- Fins + cold plate
  - 18.5mm
- 3 boards have
  - 56.5mm





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      - 8GB HBM (BW 460GB/s)
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- Transceiver
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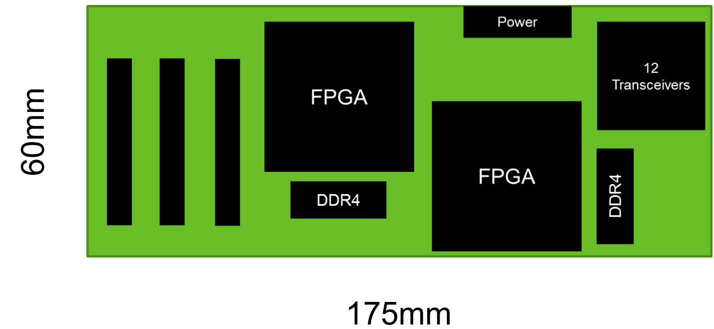

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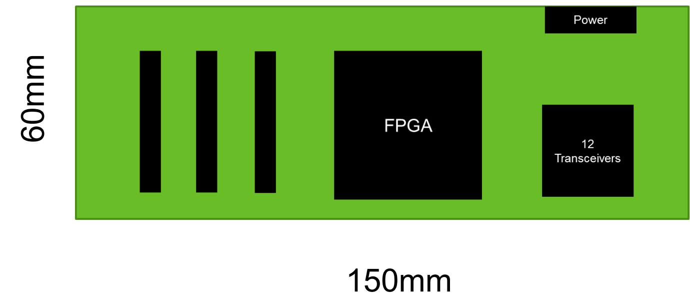

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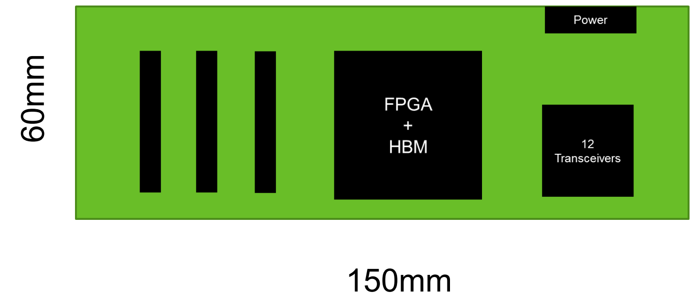

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DAQ A-U200-A64G-PQ-G

DSP CORE

16GB EEC DDR4

AXI-stream

AXI-stream

DMA

Application specific

AXI-stream

QSFP 100Gbps

100G Hard IP + Packetizer

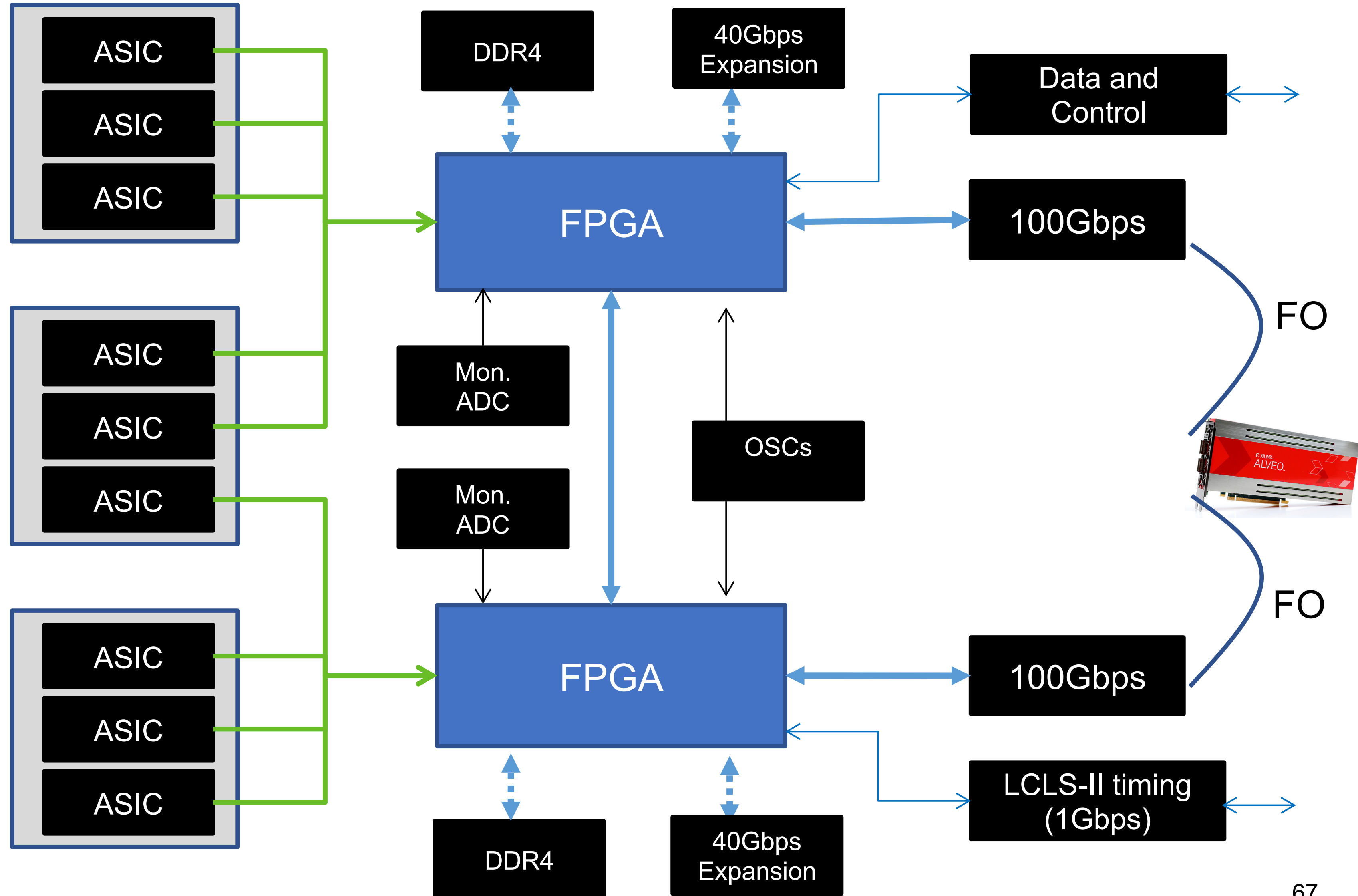
AXI-Lite

AXI-PCIe-CORE

CPU

ALVEO CORE

Camera data board (x2)

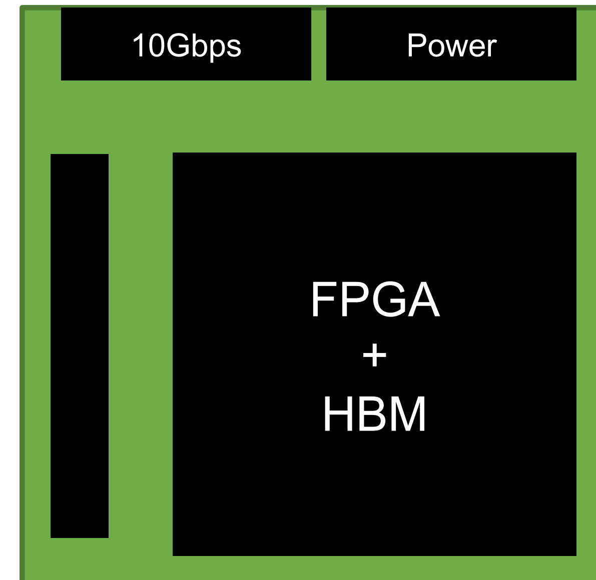


Data card

- Board dimensions
  - 60 x 175mm
- Parts placement
  - Connector dimensions (40 x 6mm)
  - FPGA dimensions (42x42mm)
  - Transceiver dimensions (25x25mm)

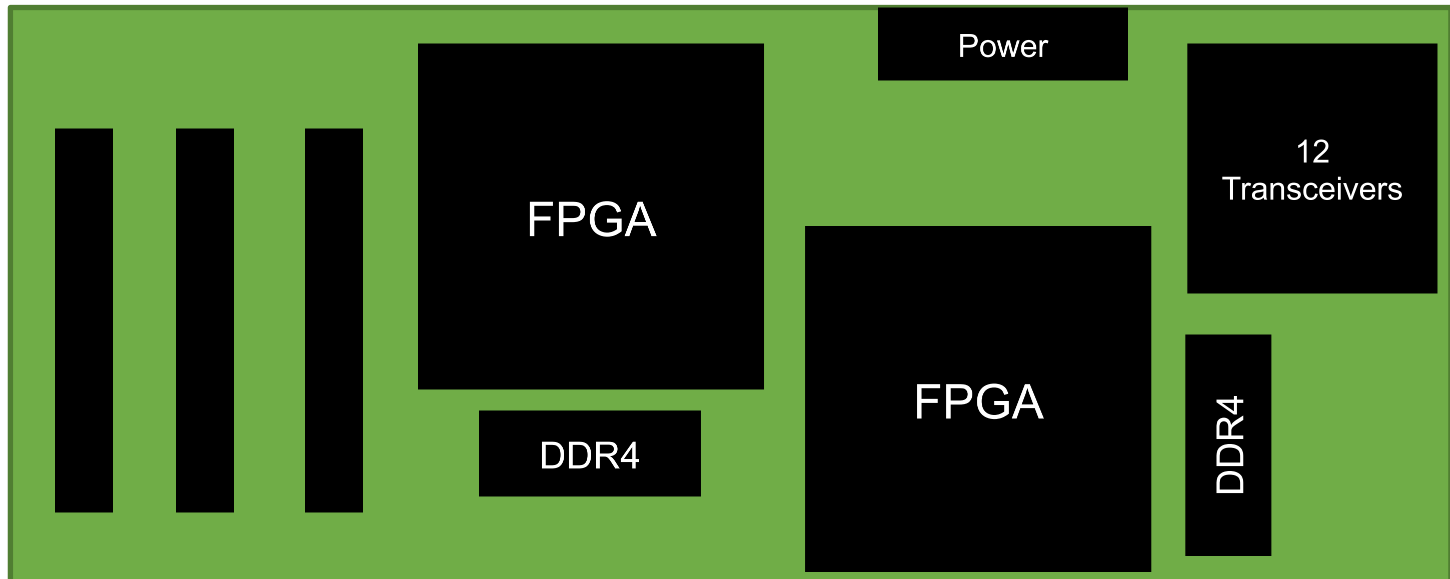
Data card

- Board dimensions
  - 60 x 175mm
- Parts placement
  - Connector dimensions (40 x 6mm)
  - FPGA dimensions (42x42mm)
  - 10Gbps on copper to the backplane



Data card

- Board dimensions
  - 60 x 150mm
- Parts placement
  - Connector dimensions (40 x 6mm)
  - FPGA dimensions (35x35mm)
  - Transceiver dimensions (25x25mm)



Risks and mitigation plan

SLAC

- Extraction heat from the camera in vacuum
  - Mitigation
    - Thermal simulation analyses
- Transferring the data from vacuum to DAQ system
  - Mitigate
    - Test eval. board & data center card using IBERT, DMA, peak and average bandwidth analyses tools
    - https://www.pavetechnologyco.com/sealed-fiber-optic/
- Power distribution
  - High current, at ASIC voltage level
    - Mitigation
      - DCDC + LDO at the “fin” level.
  - DCDC + LDO at the carrier “fins”
    - Prototype a carrier and investigate board layout + filter for low noise
- Protocol
  - Current PGP3 does not meet requirements
    - Eval. 100GbE hard IP with lightweight wrapper. Plan B is PGP v4

Risks and mitigation plan

SLAC

- Direct beam exposure (DBE)
  - Direct beam exposures is avoided or stopped when users notice the incident and move the camera and or shut the beam. At 10k events per second the dose imposed into the sensor will be 3 order of magnitude higher than current practices, but the radiation tolerance for the silicon sensor is still the same.
  - Mitigation
    - Development image processing firmware to process on the fly images to detect DBE. This information will warn users of the DBE situation by adding a flag to the image header. This flag can be the origin of a push notification at the DAQ system, instead of a pooling, increasing the chances of fast reaction time and less radiation dose due to beam exposure.

On going tests
100Gb optical vacuum to air testing

TID-AIR SLAC

- Data center card
  - https://www.xilinx.com/products/boards-and-kits/alveo/u200.html#buy
- Data module simulation card
  - https://www.xilinx.com/products/boards-and-kits/ek-u1-kcu116-g.html#hardware
- 25GB/s SFP transceivers
  - https://www.fs.com/products/67991.html
- Feedthrough
  - PAVE-Seal® 4626. 48 fibers per assembly

https://belilove.com/article_205_Fiber-Optic-Feedthrough.cfm

Partial results DMA to Alveo DDR4 memory

Raw Speed: 512 x 300 MHz = 64b x 2400 speed = 153.6Gb/s

Write Speed: ((300 MHz) x 8b/B (0x3fffffff + 1)B) / 0x13000034 = **129.3 Gbps** (84.2% eff) per bank

Read Speed: ((300 MHz) x 8b/B (0x3fffffff + 1)B) / 0x184f67e1= **101.1 Gbps** (65.8% eff) per bank

QSFP loopback

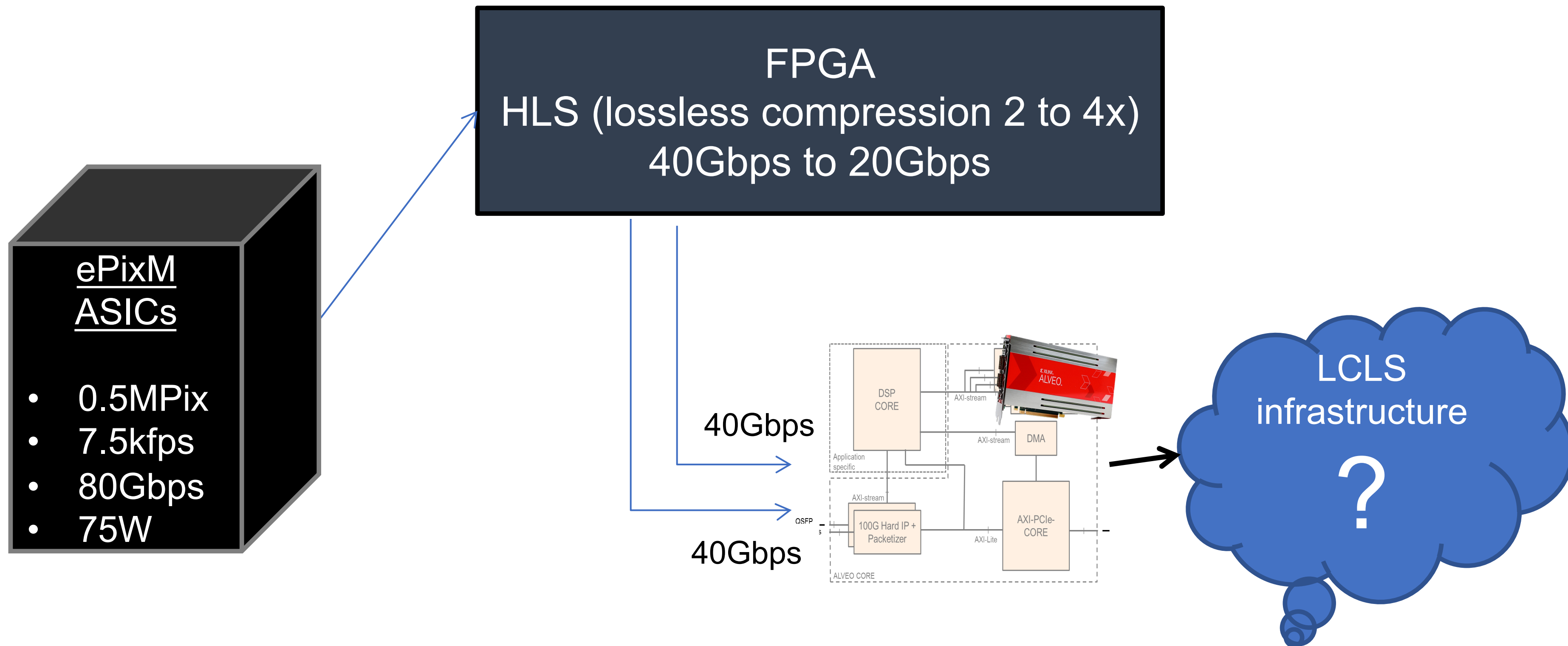
TID-AIR SLAC

- Firmware enables to test the 25gbps shows links in lock
- Can be the baseline for the air-vacuum-air fiber loopback

TX	RX	Status	Bits	Errors	BER	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	BERT Reset	TX Pattern	RX Pattern	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
						0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	✓	Inject	Reset	Reset			None
MGT_X1Y44/TX	MGT_X1Y44/RX	25.781 Gbps	4.041E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	✓	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y45/TX	MGT_X1Y45/RX	25.781 Gbps	4.041E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	✓	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y46/TX	MGT_X1Y46/RX	25.781 Gbps	4.042E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	✓	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y47/TX	MGT_X1Y47/RX	25.781 Gbps	4.042E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	✓	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y48/TX	MGT_X1Y48/RX	25.748 Gbps	4.042E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	✓	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y49/TX	MGT_X1Y49/RX	25.781 Gbps	4.042E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	✓	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y50/TX	MGT_X1Y50/RX	25.781 Gbps	4.042E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	✓	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y51/TX	MGT_X1Y51/RX	25.802 Gbps	4.042E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	✓	Inject	Reset	Reset	Locked	Locked	None

Ways to implement this camera using 40Gbps links

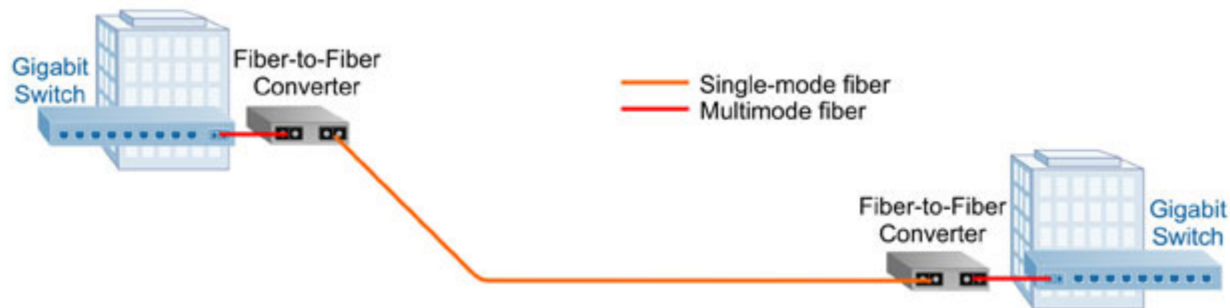
TID-AIR SLAC



How much resources does the algorithm will require?
How much power will the algorithm consume?

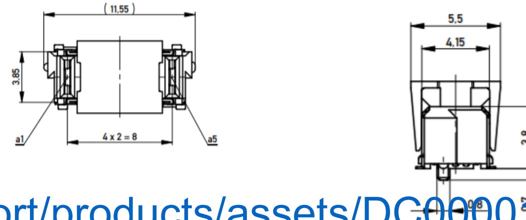
Multi mode to single mode fiber concept

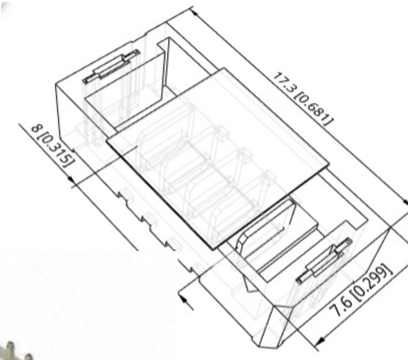
- https://www.omnitron-systems.com/products/flexpoint-unmanaged-fiber-to-fiber-media-converters.php

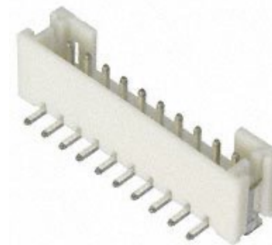


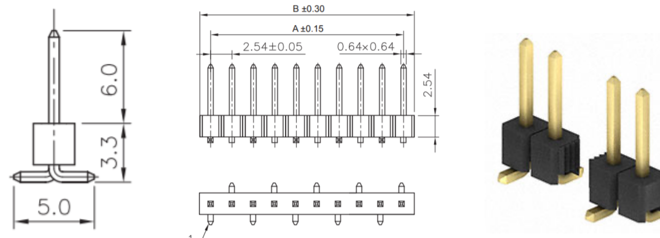
Power connector

- Erni
  - 5 pin 18A/pin
  - https://www.erni.com/fileadmin/import/products/assets/DC0000110.PDF
- Samtec
  - UMPT-05-01.5-T-VT-SM-WT-K
  - 21A per pin
- JST
  - 455-1742-2-ND
  - 2A per pin
- WE
  - 732-5367-5-ND/732-2859-ND
  - 3A per pin



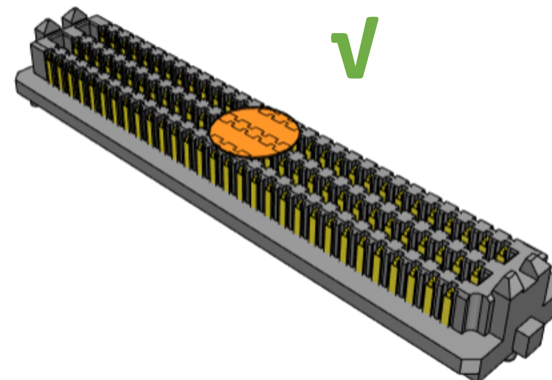






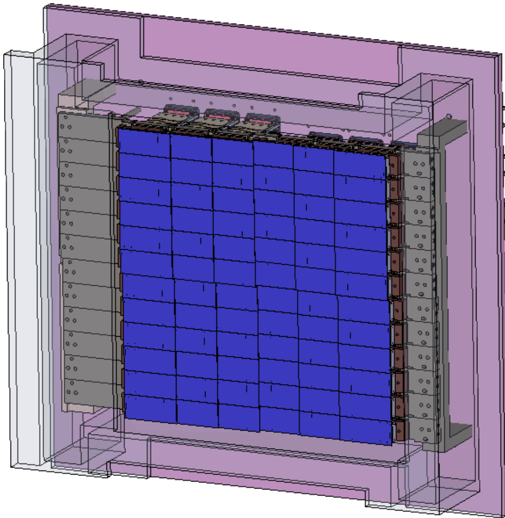
connectors

- Airborne
  - Mil standard
  - Low profile
  - Very reliable
  - Up to 100 pins
  - Cost is larger
- SEAM8 √
  - SEAM8-40-S02.0-L-06-2-K
    - Height is 2mm
  - 56Gpbs
  - 0.050” / 0.0315” pitch
  - Low insertion force
  - Up to 500 pins
  - Lower cost (~$15)

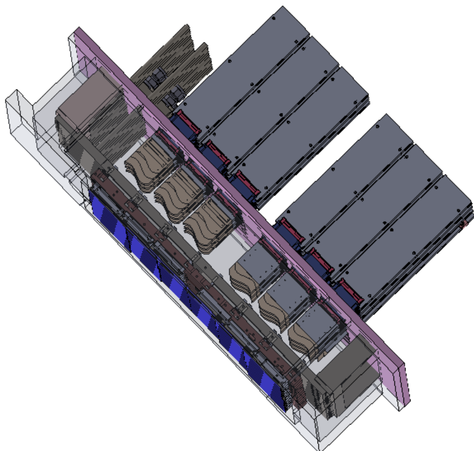


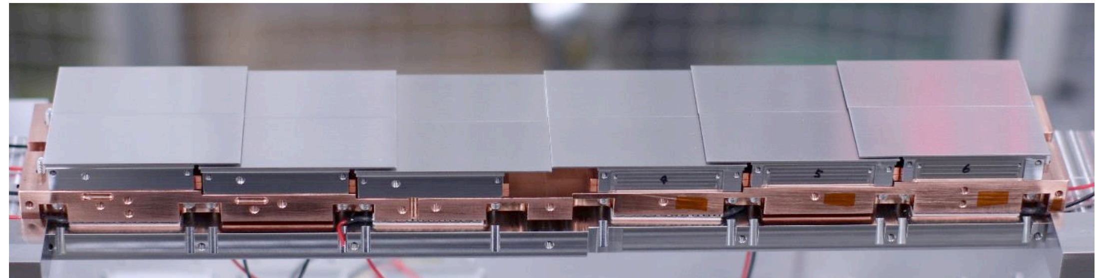
Example of a shingled camera (CITIUS - T. Hatsui)

Front view



Top view





Shingled ladder