Concept for a shingled 1Mpix ePixM camera

August 22, 2019

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on behalf of SLAC TID
Detector Team
Electronic system
Integrated Circuits

U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

Motivation

- ePixM project aims a developing a high rate camera for soft x-rays experiment at LCLS
  - Soft x-ray scattering/imaging detectors form a significant part of the LCLS detector development strategy
    - Key detector for soft x-ray (SXR) resonant elastic x-ray scattering (REXS) experiments in LCLS NEH 2.2.
    - XPCS
    - Other Coherent Scattering (CS) experiments

Goal for this project

- *On going ePixM project aims at developing a tileable 192x384 pixels camera prototype with performance within requirements*

- *Goal of the proposed project:*
  - ***Develop a low risk concept for tileing ePixM prototype modules into a large area 1Mpix camera.***
  - *Setup the infrastructure for soft x-ray entrance window fabrication*

- Critical for:
  - being in the conditions to present required results for the FY20 down-selection process comparing ePixM to VFCCD

Motivation

- Project requirements

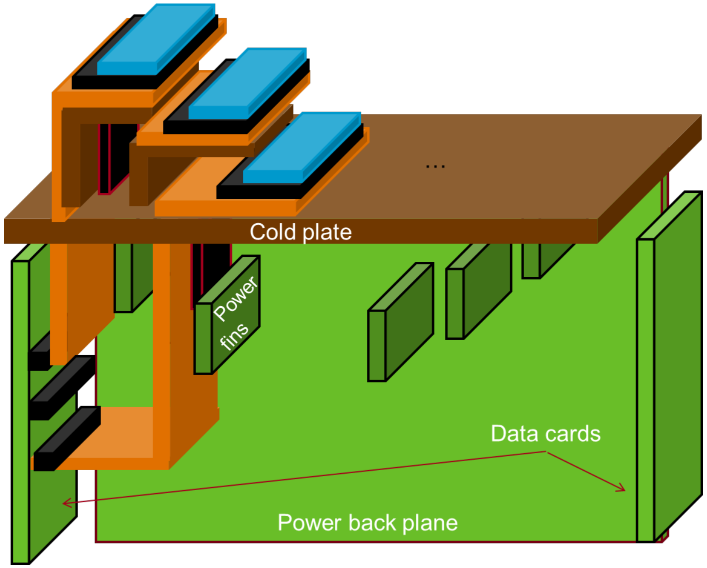
Parameter	Threshold	Objective	REXS	XPCS	CS	1MPixM
Pixel Pitch (um)	50	50	√	√	√	50
Read Noise (e- rms)	15	10		√	√	12
Quantum efficiency (%, 275eV-1500eV)	70	90	√	√	√	TBD
Frame Rate (kHz)	5	10	√	√	√	7.5
Array size (pixels)	512x512	1024x1024	√	√	√	1152x1152
Well Depth (Number of 530eV photons)	1000	3000	√		√	TBD
Vacuum outgassing rate (torr*L/s)	2E-8	1E-8	√			TBD
Cabling and cooling length (m)	2	4	√		√	TBD
Physical package envelope (WxLxD, mm)	100x175x75mm	75x150x50mm	√			100x175x75mm
Maximum Power dissipation (W)	100*	50	√	√	√	200

* Assuming a 2x3 tiles or 768x576

Array Size:
- Impractical to complete a full-size device in FY20,
- In FY20 compliance with this requirement can be met on the basis of a demonstrated tileable submodule, as long as a low-risk path to realizing the threshold array size requirement with a fill factor >80% is demonstrated.

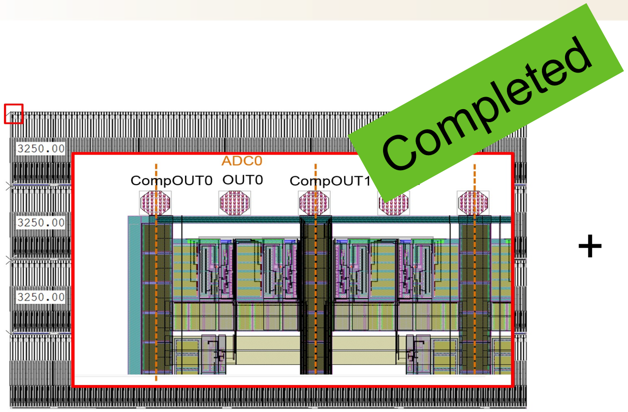
ePix M camera system

- Components
  - ***Front end electronics***
    - *Tightly connected to ASIC geometry/shingle geometry*
    - *Power to ASICs/sensor*
    - *Control signal to ASICs*
    - *Data access to ASIC*
    - *Cooling system*
  - ***Camera DAQ***
    - *IO to FPGA*
    - *Control logic*
    - *Data storage (full frames)*
    - *Data compression*
    - *Data transmission*
  - Back end DAQ
    - User interface
    - Data reception
    - Data storage



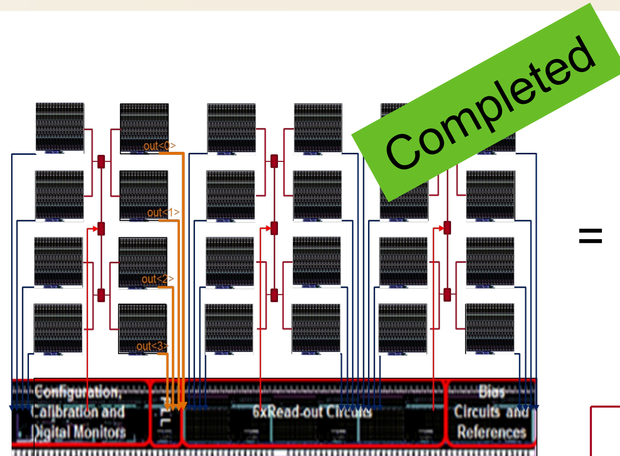
- *Aspects to be studied*
  - *Mechanics*
  - *Thermal dissipation*
  - *Power distribution*
  - *Signal distribution*
  - *Data reduction*

ePixM module (cartoon)



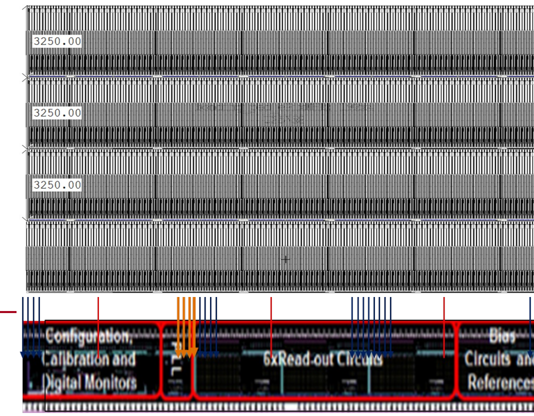
LFoundry CIS matrix
192 x 384 pixels
19772 x 10371 µm

+

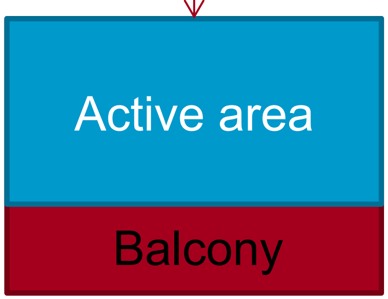


ePixM HR backend
768 (4 x 192) ADCs
20072 x 14932 µm

=



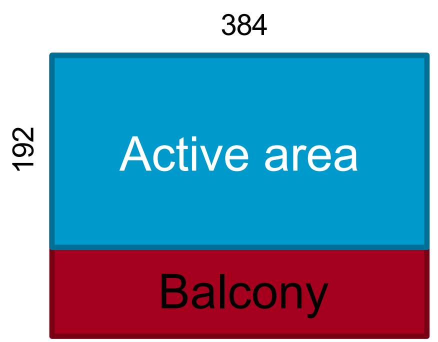
Bump bonded
192x384 pixel module

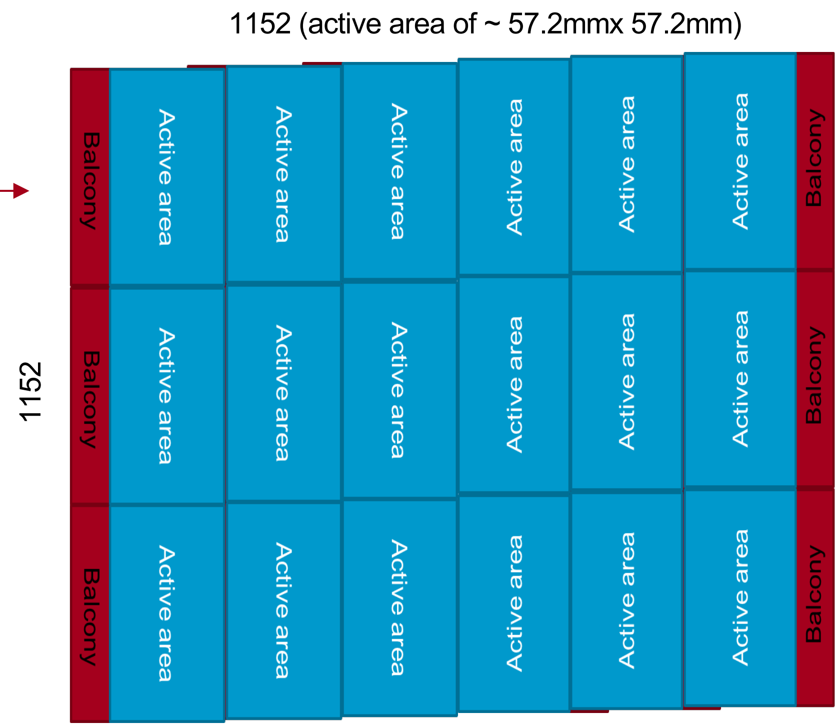


- *To avoid gaps in the detectors shingling is required to hide balconies when tiling modules*

Baseline concept to be developed in this project

Side view





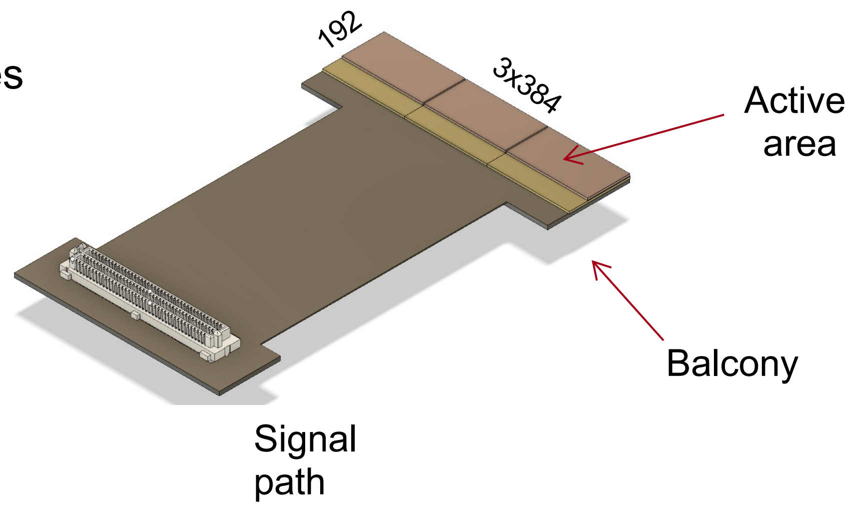
- The ePixM front-end ASIC is 384 * 192 pixels.
  - Size is 19.772 x 10.371 mm
- The ePixHR-M readout
  - Size is 20.072 x 14.932 mm

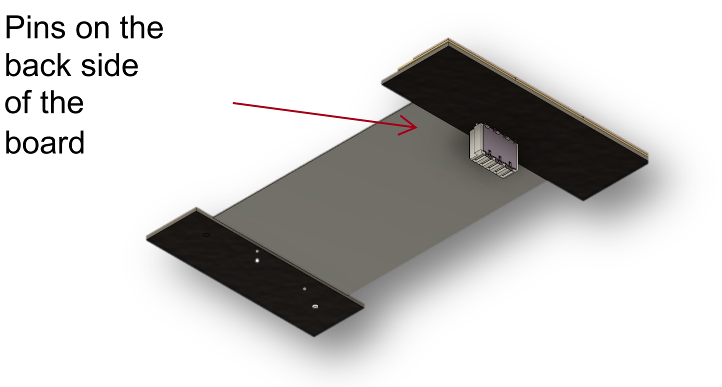
1 tile ~ 8W
Total ~150W

Front view

Rigid to flex boards + power cable

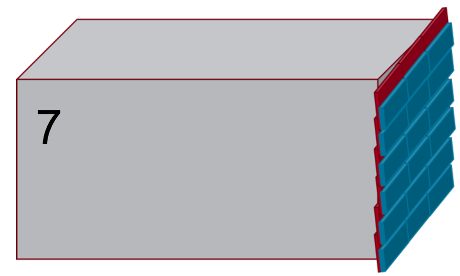
- Shingle unit based on current ASIC geometries
- 3 ROIC + ePixM matrix per tile
- Flex circuit
  - transmit control and data signals
  - SAM8 connector family
- Independent power path
  - 24W
  - Connector
    - 3 pins for analog
    - 2 pins for digital
    - >6A/pin
    - Solution
      - ERNI 214356

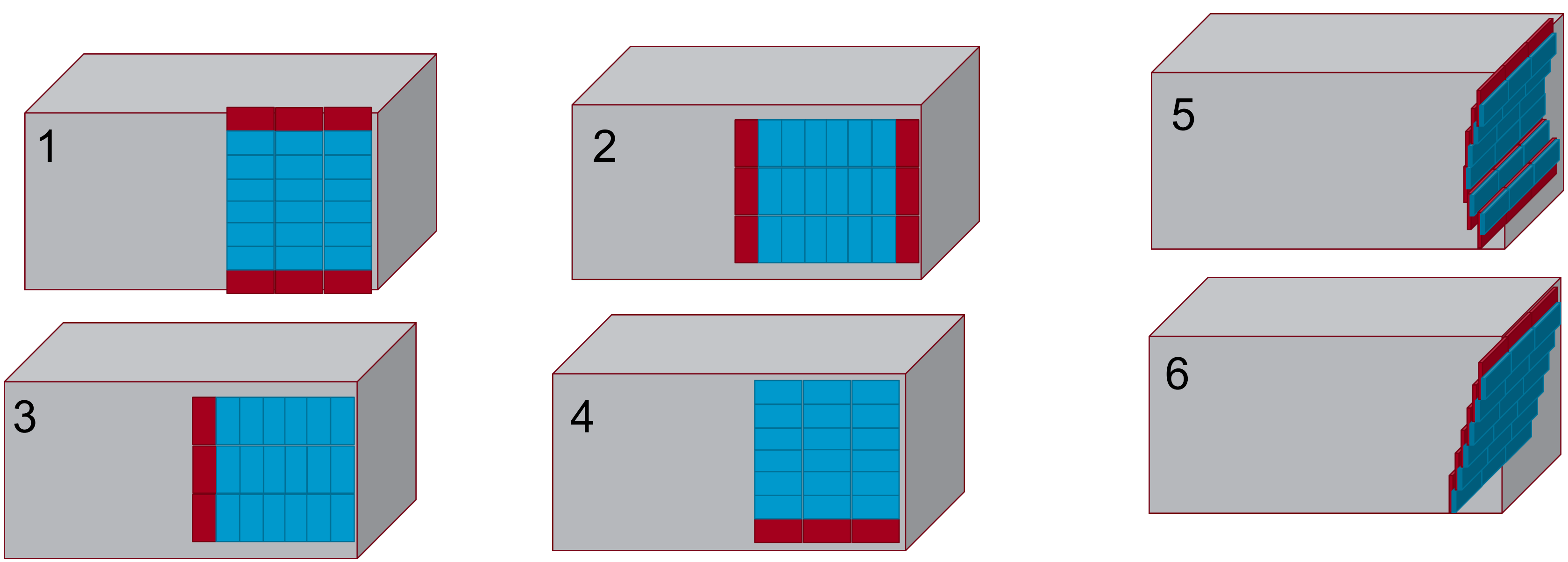




Is there a preferred tiling direction?

- Possible shingle arrangements
  - ASICs parallel to the camera face (1 to 6)
  - ASICs at an angle with the camera face (7)
- Meet threshold 100x175x75mm
  - 1, 2, 3 and 4
- Any variation that would make sense?





What are the camera dimensions flexibilities?

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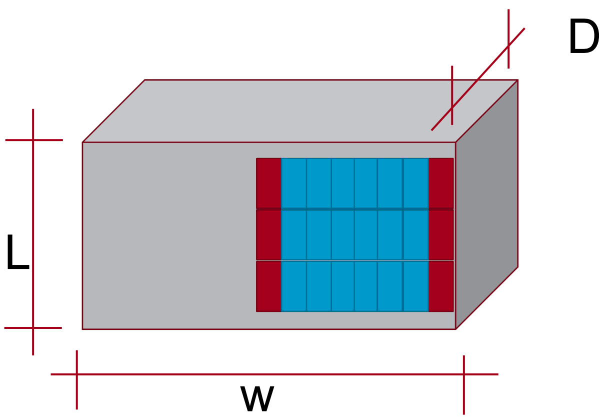
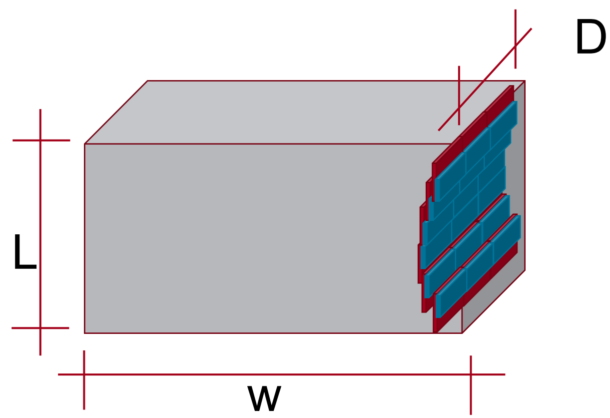
“

Physical package envelope (WxLxD, mm)	100x175x75mm	75x150x50mm	√			100x175x75mm

”

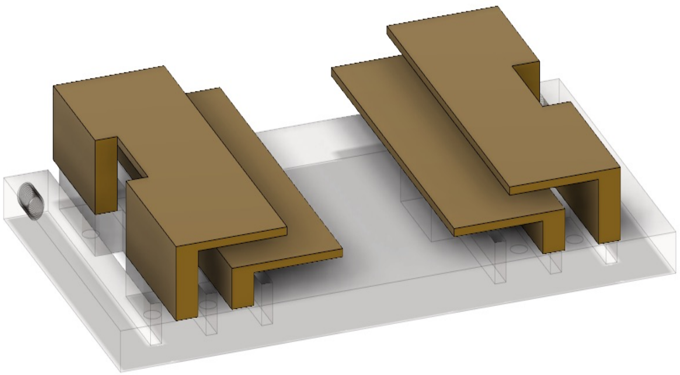


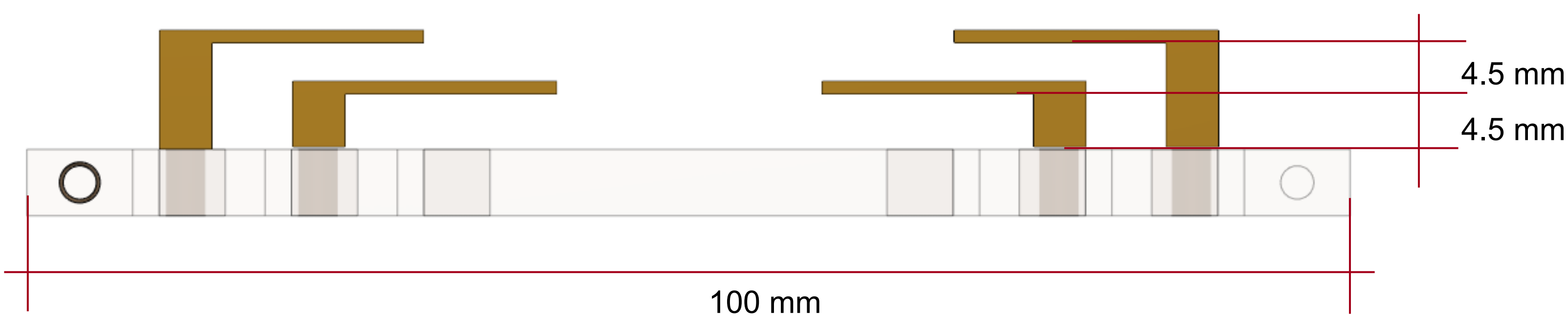


Are these valid interpretations?

What is the limit for the tile step (away from the face of the camera)?

- Gap among fins are 4.5 mm
  - 1mm for fins base
  - 1mm for board
  - 1.5 mm for ASIC stack
  - 1 mm for wirebonds





Questions about camera mechanics

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- Is there a preferred tiling direction?
- What is the limit for the tile step (away from the face of the camera)?
- What are the camera dimensions flexibilities?

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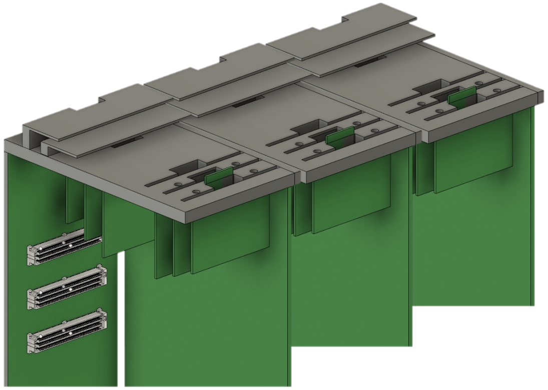

Our choice of tiling and camera face impact multiple camera arrangements.

Power considerations

ASIC characteristics

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1 ASIC

- Power supply voltage level
  - 2.5V @ 2A
  - 1.8V @1A
- Power supply coupling requirements
- LVDS
  - 24 data transmission per ASIC
  - 1 clock receiver
- single ended
  - 17 control lines inputs and output
  - 1 x Analog monitor

3 ASICs

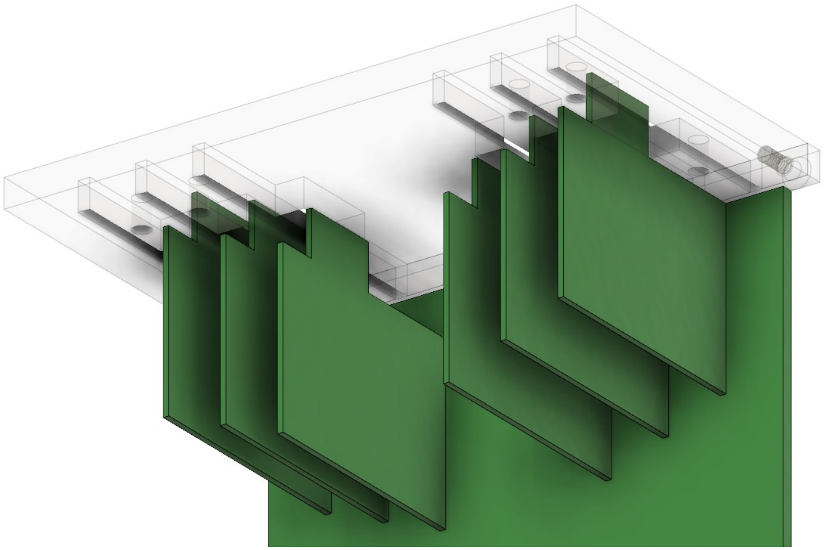
- Power supply voltage level
  - 2.5V @ 6A
  - 1.8V @ 3A
- Power supply coupling requirements
- LVDS
  - 72 data transmission per module
  - 3 clock receiver
- single ended
  - 20 control lines inputs and output
  - 3 x Analog monitor

18 ASICs

- Power supply voltage level
  - 2.5V @ 36A
  - 1.8V @ 18A
- Power supply coupling requirements
- LVDS
  - 432 data transmission per camera
  - 6 clock receiver
- single ended
  - 68 control lines inputs and output
  - 18 Analog monitor

Power consideration

- The estimate is 150W of power
  - @6V : 25A
  - @12V: 12.5A
  - @24V: 6.25A
- Separate power from signal (flex)
  - Use power connectors with independent cable
- Implementation
  - Power backplane
    - Power to ASIC + data modules
  - Power "fins"
    - 3 ASICs per fin



Questions about power limits

- The proposed camera consumes
  - at the ASIC level 150W
  - At the FPGA level 50W (estimated)

- What is driving the parameter for the requested power limits?
  - What are the compromises that can be made here?
    - Array size?
    - Others

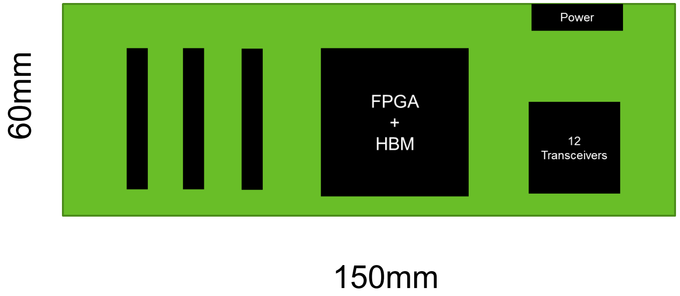
Data considerations

Data cards

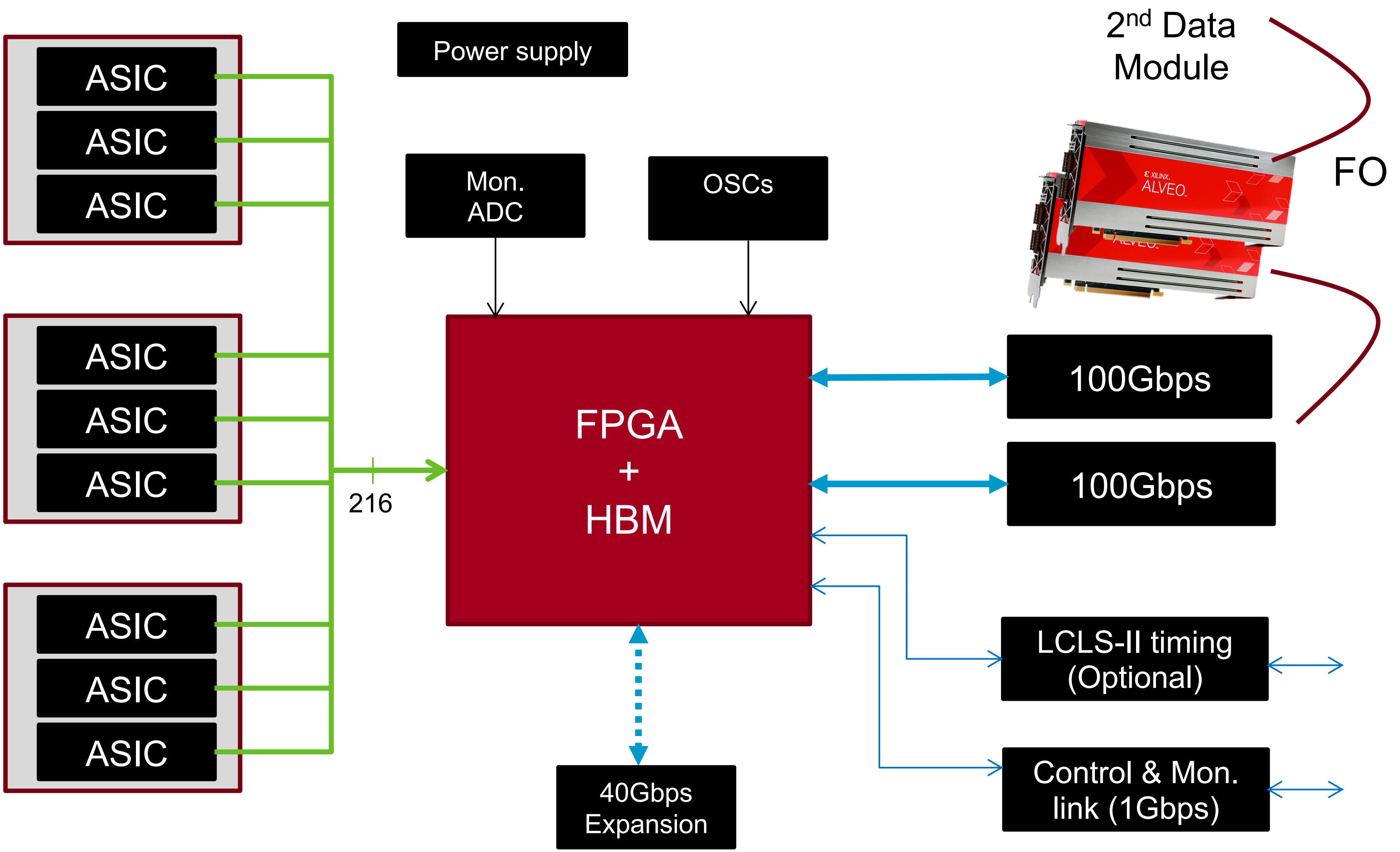
- 2 data cards per camera
  - IO requirements (data into the camera)
    - **432** IO/module (24 x 2 IOs per line x 3 ASICs x 3 modules)
    - 23 IO/module for ASIC control
    - Analog monitoring ADC IOs
    - Digital monitoring IOs
  - Data volume
    - **108Gbps/per side** (216 diff. data lines @ 500Mbps)
    - **80Gbps/per side** (512*1152 pixels *2 bytes * 7.5kfps * 8bits)
  - Data transmission (data out from the camera)
    - 25Gbps per transceiver
    - **100Gbps** links per data module

Data cards platform

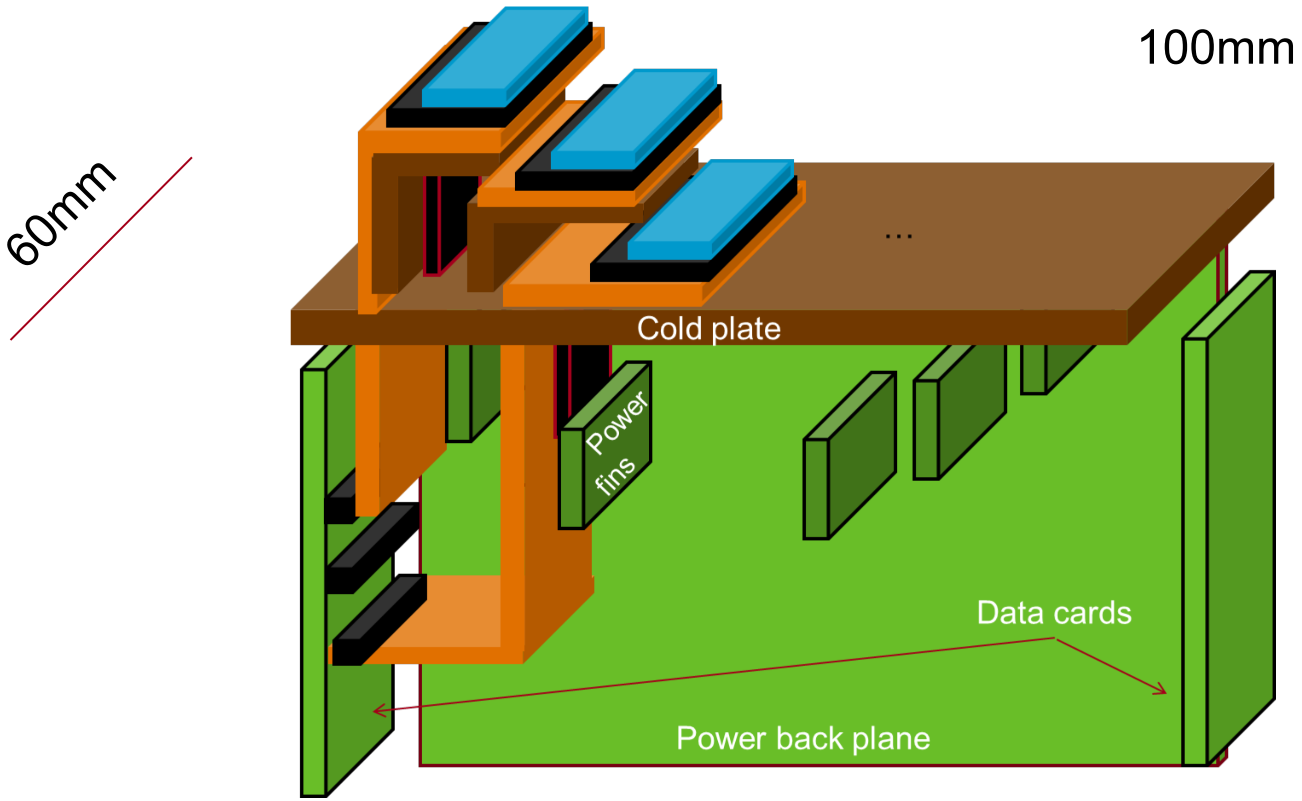
- FPGA
  - Xilinx Kintex Ultrascale plus
    - 2 FPGS / data module ($)
      - Enable the use of DDR4
      - Capable of implementing simple data reduction
      - Uses full camera size, consumes more power
    - 1 FPGA per data module ($)
      - No DDR4 memory
      - Control camera and routes data through
    - FPGA + HBM (3D) ($$$)
      - 8GB HBM (BW 460GB/s)
      - Capable of image processing
- Transceiver
  - 300 Gbps (12 x 25Gbps), 25 x 25 mm
  - https://www.amphenol-icc.com/product-series/leap-on-board-transceiver.html



Camera data board



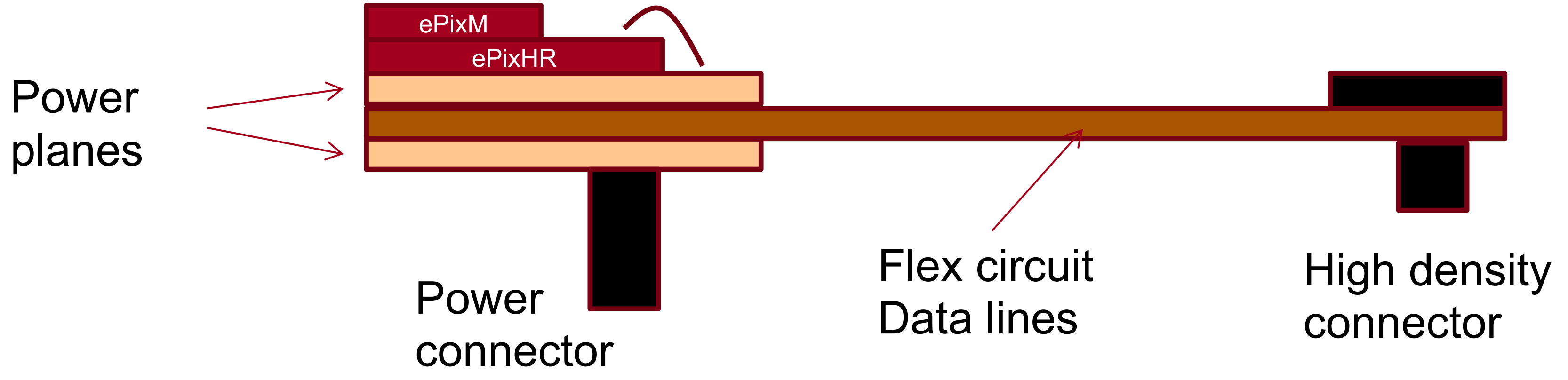
Camera head sketch



* ½ of the shingles are shown

Chamber + outgassing considerations

- Board materials
  - FR4
    - Porous material
  - Polyimide
    - Has been used in camera that were installed in soft x-ray chambers (cFCCD, 1kFSCCD)
    - https://www.dupont.com/content/dam/dupont/products-and-services/membranes-and-films/polyimde-films/documents/DEC-Kapton-summary-of-properties.pdf



Feedthrough + outgassing considerations

- Manufacturer suggest Electron Beam welding, aluminum to aluminum
- For our tests
  - Evaluate mechanical stress on the 100Gbps
  - Use epoxy
  - Limit it to High Vacuum

Metrology consideration

Heat dissipation

- Thermal simulation should use fluid dynamics
  - That includes not only the inside of the material but all air/vacuum influences

DRP – Data reduction pipeline

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- Can start at the camera level
- General algorithms may be used
  - Lossless compression
  - https://www.sciencedirect.com/topics/computer-science/lossless-compression
- Application specific algorithms may be at use
  - ROI (row, col data formatting + ROI corners)
  - Thresholding (dark subtraction, gain correction common mode correction?, plus threshold to select pixel)
  - Digital integration
  - Hit counting
  - clustering

DAQ & Data considerations

Data interface card
DAQ A-U200-A64G-PQ-G

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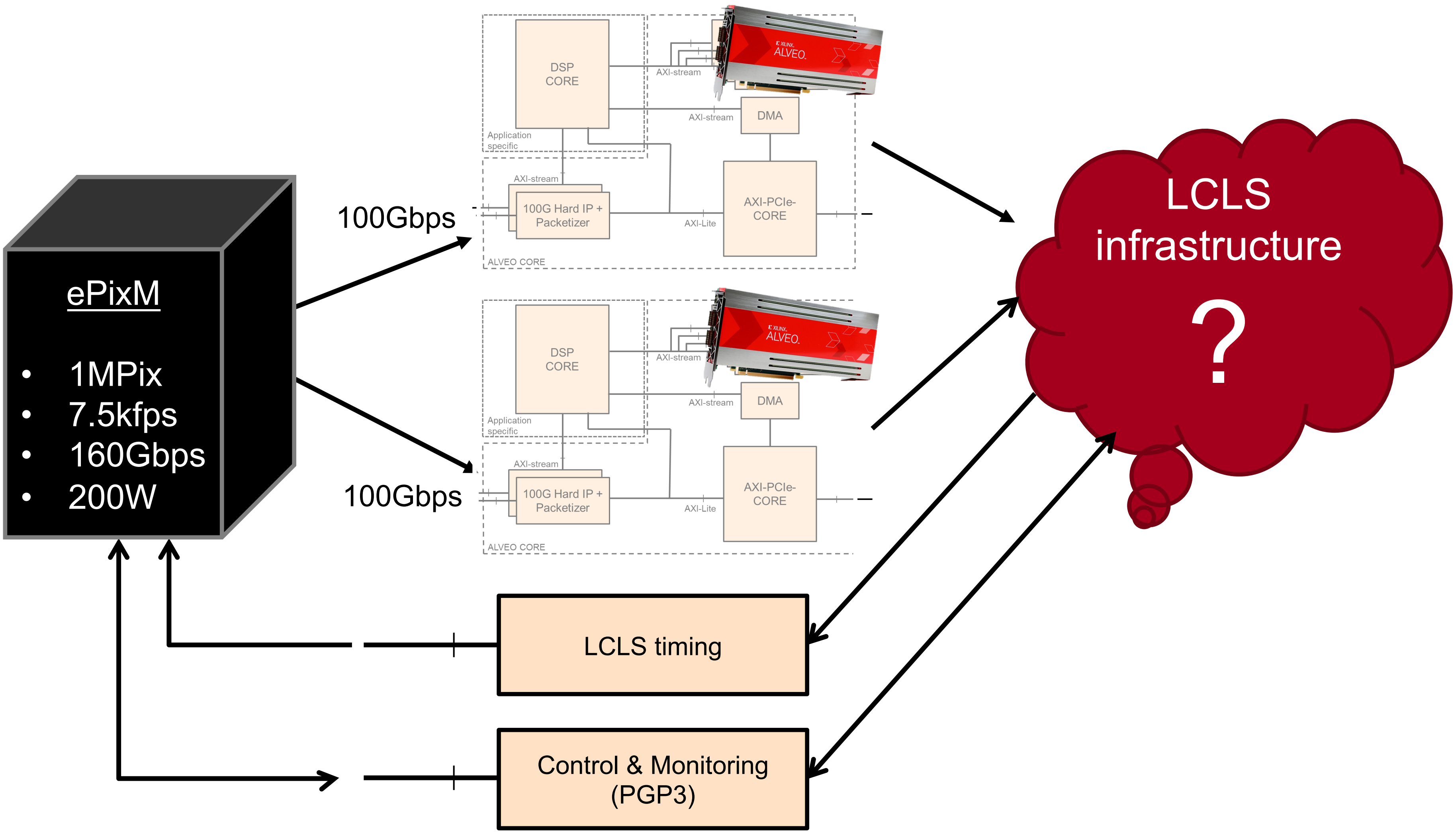
Off-chip Memory Capacity	64 GB
Off-chip Total Bandwidth	77 GB/s
Internal SRAM Capacity	35 MB
Internal SRAM Total Bandwidth	31 TB/s
PCI Express	Gen3x16
Network Interfaces	2x QSFP28 (100GbE)
Maximum Total Power	225W
Thermal Cooling	Passive/Active

Working with
Matt Weaver
Larry Ruckman
Ryan Herbst

Going beyond the camera



Project Scope & Deliverables

- 1Mpix camera concept development including:
  - Mechanics (started)
  - Thermal dissipation (not started)
  - DAQ concept (started)
    - Power distribution (started)
    - Data streaming - vacuum to air (started)
    - Camera specific firmware (not started)

Deliverables:

- ***Report documenting concept and risk analysis.***

Main questions that we would like to answer today

- What are the limiting factor for the camera envelope (WxHxD)?
- What is the preferred tiling option?
- What is the limiting factor for the power consumption?

BACKUP slides

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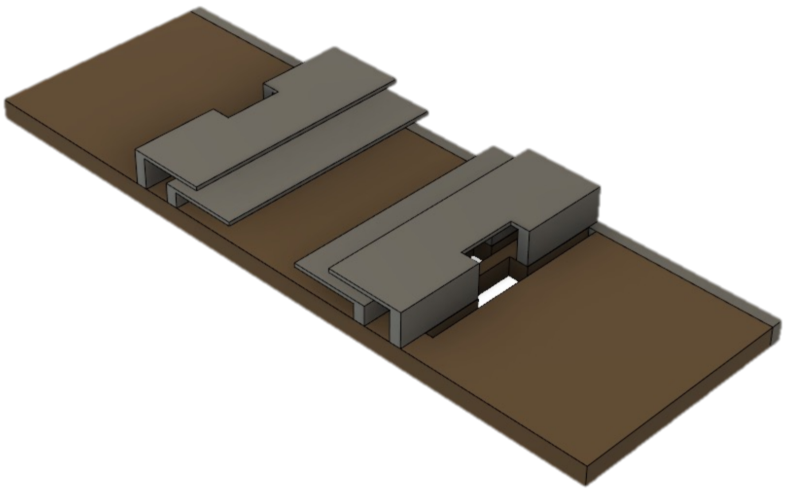
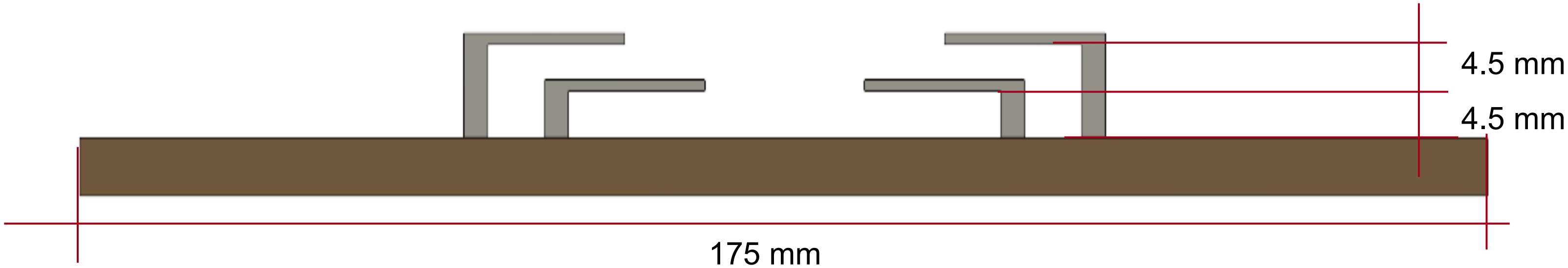
Cold plate for the shingle

- Gap among fins are 4.5 mm
  - 1mm for fins base
  - 1mm for board
  - 1.5 mm for ASIC stack
  - 1 mm for wirebond
- Fins + cold plate
  - 18.5mm
- 3 boards have
  - 56.5mm





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    - **2 FPGS / data module ($)**
      - **Enable the use of DDR4**
      - **Capable of implementing simple data reduction**
      - **Uses full camera size, consumes more power**
    - 1 FPGA per data module ($)
      - No DDR4 memory
      - Control camera and routes data through
    - FPGA + HBM (3D) ($$$)
      - 8GB HBM (BW 460GB/s)
      - Capable of image processing
- Transceiver
  - 300 Gbps (12 x 25Gbps), 25 x 25 mm
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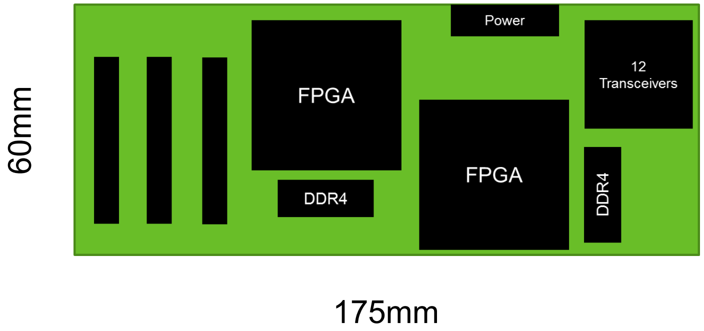

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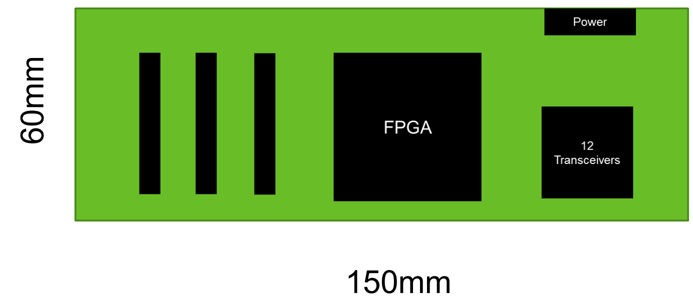

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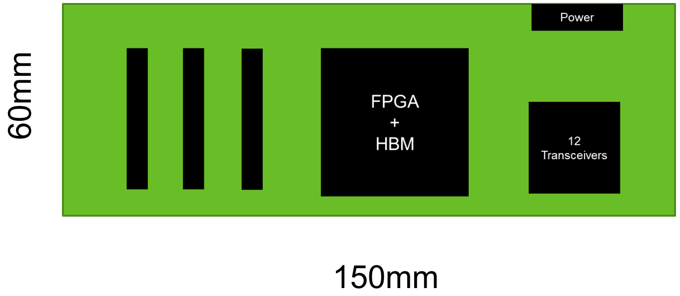

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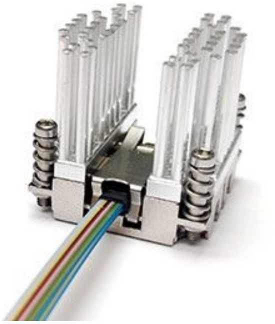

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DAQ A-U200-A64G-PQ-G

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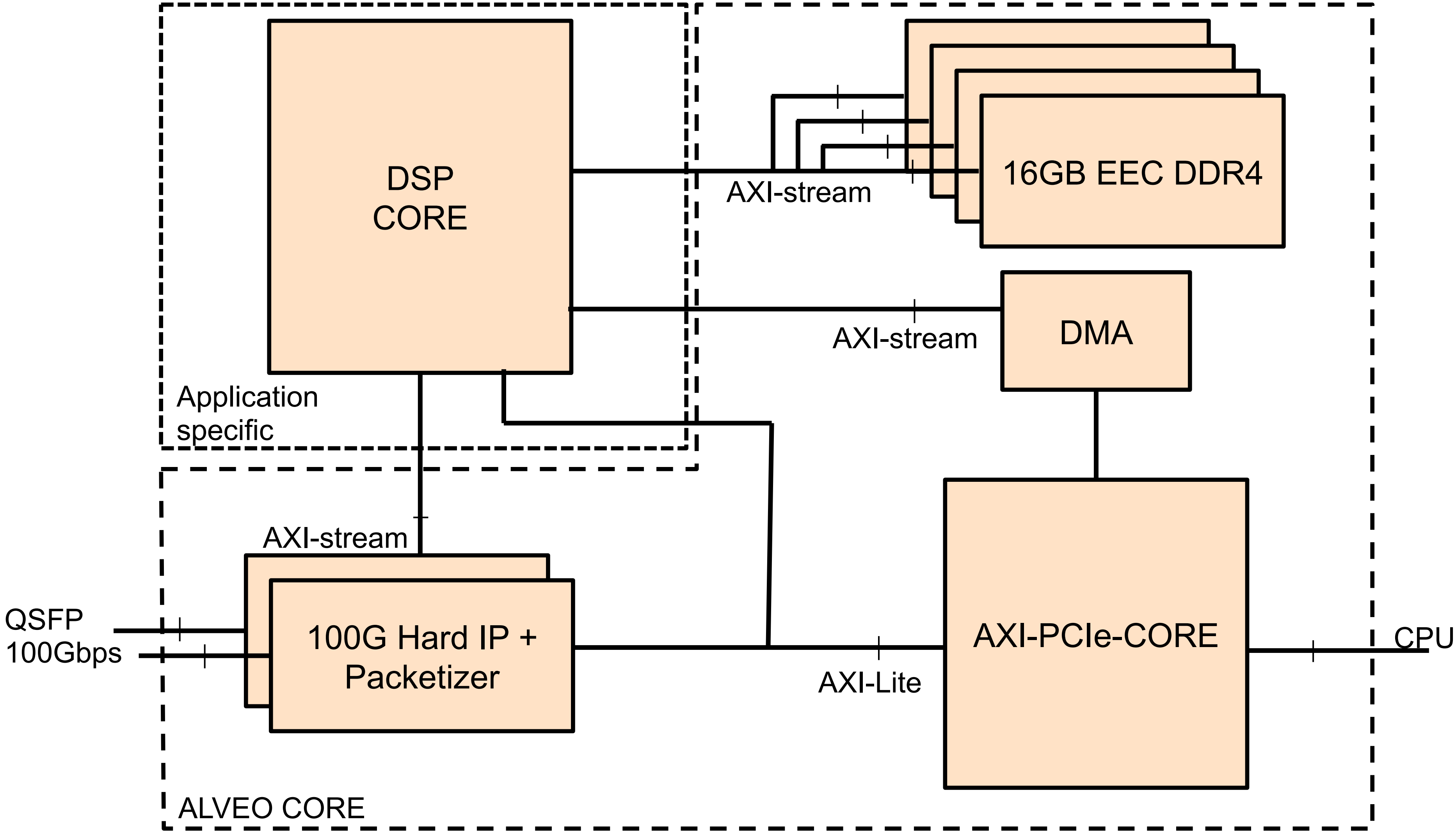
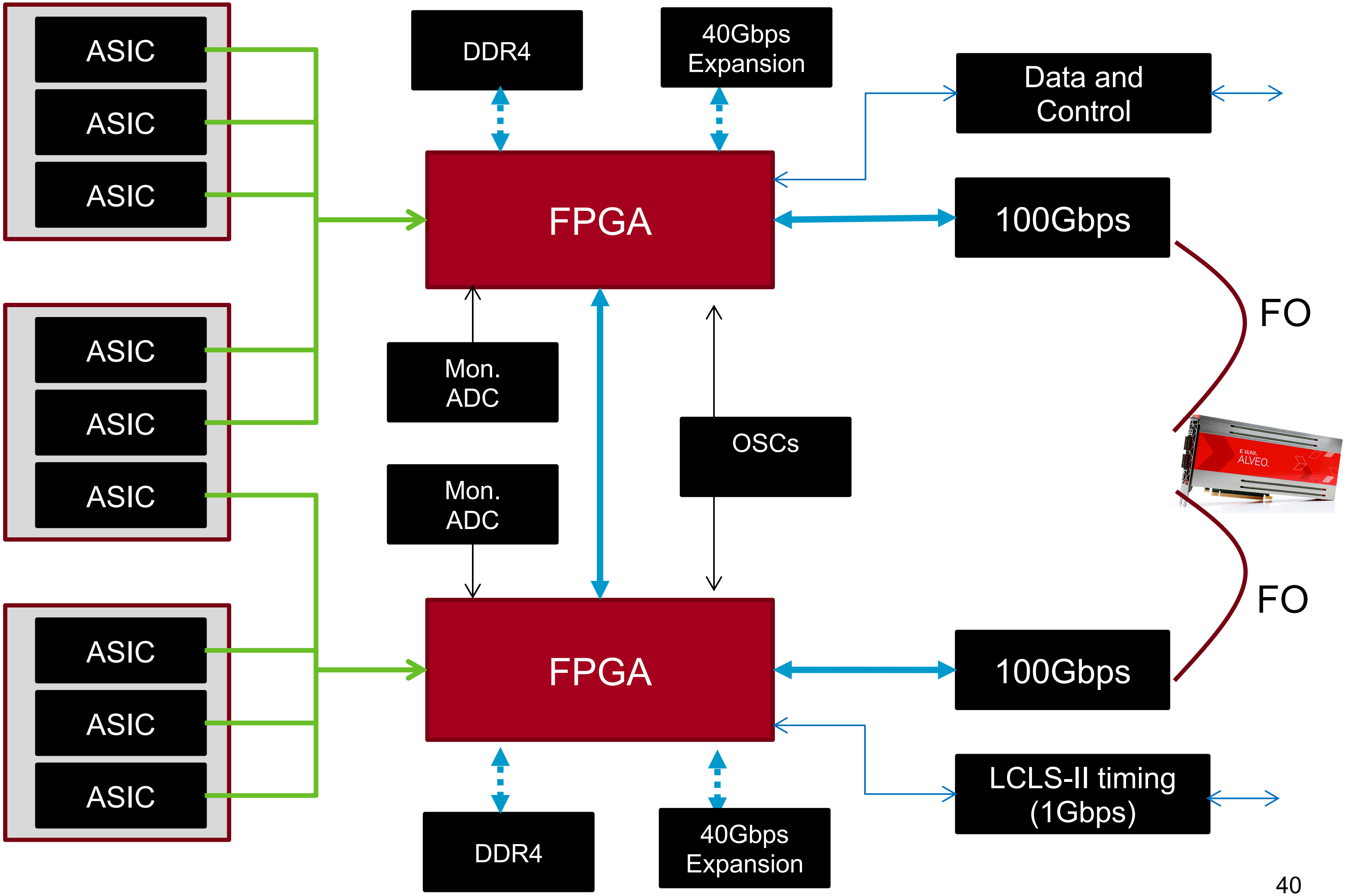
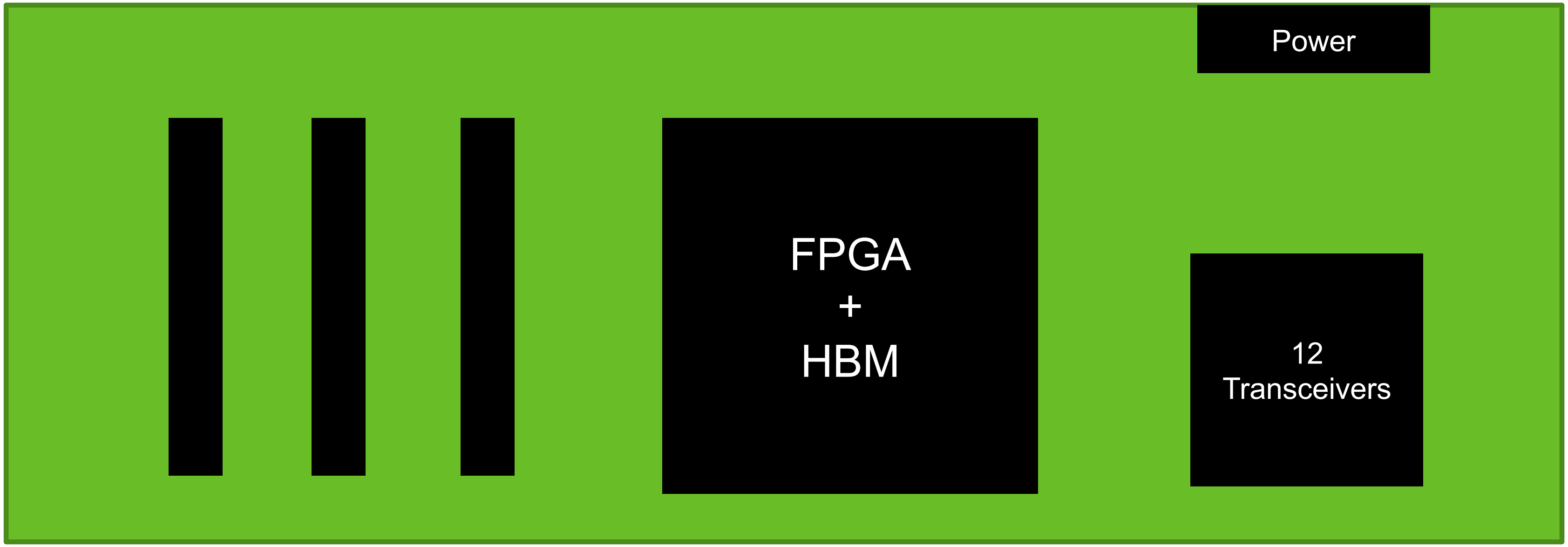


Camera data board (x2)



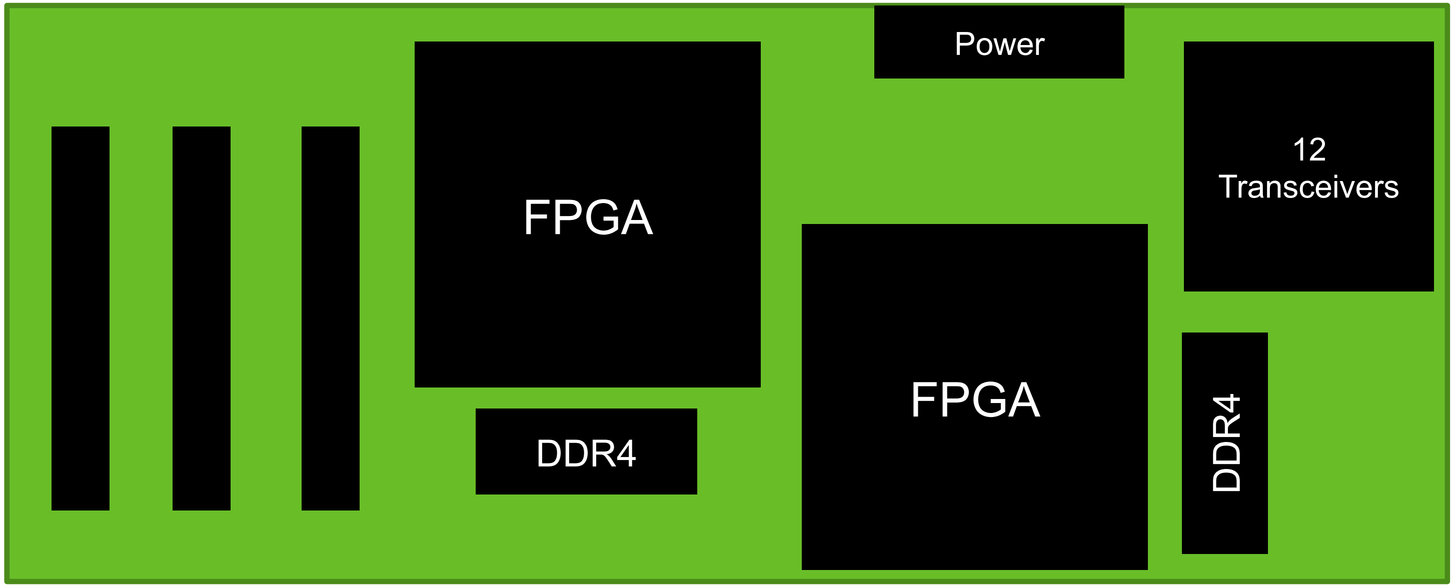
Data card

- Board dimensions
  - 60 x 175mm
- Parts placement
  - Connector dimensions (40 x 6mm)
  - FPGA dimensions (42x42mm)
  - Transceiver dimensions (25x25mm)



Data card

- Board dimensions
  - 60 x 150mm
- Parts placement
  - Connector dimensions (40 x 6mm)
  - FPGA dimensions (35x35mm)
  - Transceiver dimensions (25x25mm)



Risks and mitigation plan

- Extraction heat from the camera in vacuum
  - Mitigation
    - Thermal simulation analyses
- Transferring the data from vacuum to DAQ system
  - Mitigate
    - Test eval. board & data center card using IBERT, DMA, peak and average bandwidth analyses tools
    - https://www.pavetechnologyco.com/sealed-fiber-optic/
- Power distribution
  - High current, at ASIC voltage level
    - Mitigation
      - DCDC + LDO at the “fin” level.
  - DCDC + LDO at the carrier “fins”
    - Prototype a carrier and investigate board layout + filter for low noise
- Protocol
  - Current PGP3 does not meet requirements
    - Eval. 100GbE hard IP with lightweight wrapper. Plan B is PGP v4

Risks and mitigation plan

- Direct beam exposure (DBE)
  - Direct beam exposures is avoided or stopped when users notice the incident and move the camera and or shut the beam. At 10k events per second the dose imposed into the sensor will be 3 order of magnitude higher than current practices, but the radiation tolerance for the silicon sensor is still the same.
  - Mitigation
    - Development image processing firmware to process on the fly images to detect DBE. This information will warn users of the DBE situation by adding a flag to the image header. This flag can be the origin of a push notification at the DAQ system, instead of a pooling, increasing the chances of fast reaction time and less radiation dose due to beam exposure.

On going tests
100Gb optical vacuum to air testing

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- Data center card
  - https://www.xilinx.com/products/boards-and-kits/alveo/u200.html#buy
- Data module simulation card
  - https://www.xilinx.com/products/boards-and-kits/ek-u1-kcu116-g.html#hardware
- 25GB/s SFP transceivers
  - https://www.fs.com/products/67991.html
- Feedthrough
  - PAVE-Seal® 4626. 48 fibers per assembly

https://belilove.com/article_205_Fiber-Optic-Feedthrough.cfm

Partial results DMA to Alveo DDR4 memory
Raw Speed: 512 x 300 MHz = 64b x 2400 speed = 153.6Gb/s
Write Speed: ((300 MHz) x 8b/B (0x3fffffff + 1)B) / 0x13000034 = **129.3 Gbps** (84.2% eff) per bank
Read Speed: ((300 MHz) x 8b/B (0x3fffffff + 1)B) / 0x184f67e1= **101.1 Gbps** (65.8% eff) per bank

QSFP loopback

- Firmware enables to test the 25gbps shows links in lock
- Can be the baseline for the air-vacuum-air fiber loopback

TX	RX	Status	Bits	Errors	BER	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	BERT Reset	TX Pattern	RX Pattern	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
						0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	☑	Inject	Reset	Reset			None
MGT_X1Y44/TX	MGT_X1Y44/RX	25.781 Gbps	4.041E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	☑	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y45/TX	MGT_X1Y45/RX	25.781 Gbps	4.041E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	☑	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y46/TX	MGT_X1Y46/RX	25.781 Gbps	4.042E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	☑	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y47/TX	MGT_X1Y47/RX	25.781 Gbps	4.042E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	☑	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y48/TX	MGT_X1Y48/RX	25.748 Gbps	4.042E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	☑	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y49/TX	MGT_X1Y49/RX	25.781 Gbps	4.042E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	☑	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y50/TX	MGT_X1Y50/RX	25.781 Gbps	4.042E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	☑	Inject	Reset	Reset	Locked	Locked	None
MGT_X1Y51/TX	MGT_X1Y51/RX	25.802 Gbps	4.042E11	0E0	2.474E-12	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	Reset	PRBS 7-bit	PRBS 7-bit	☑	Inject	Reset	Reset	Locked	Locked	None

Ways to implement this camera using 40Gbps links

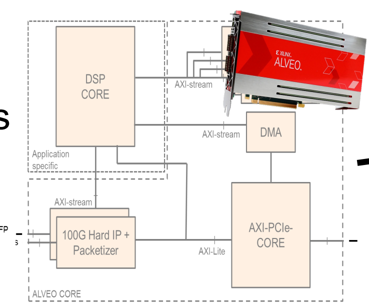
ePixM ASICs

- 0.5MPix
- 7.5kfps
- 80Gbps
- 75W

FPGA
HLS (lossless compression 2 to 4x)
40Gbps to 20Gbps

40Gbps

40Gbps

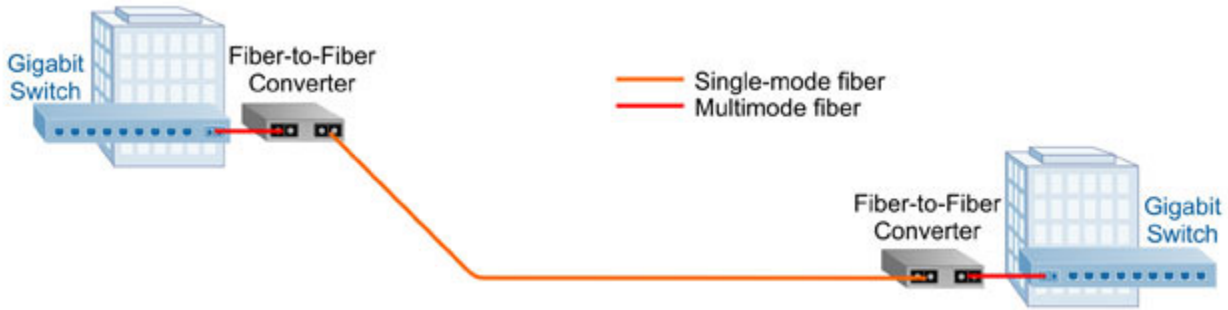


LCLS infrastructure
?

How much resources does the algorithm will require?
How much power will the algorithm consume?

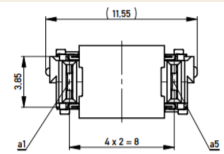
Multi mode to single mode fiber concept

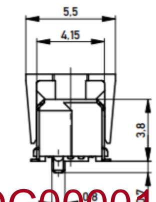
- https://www.omnitron-systems.com/products/flexpoint-unmanaged-fiber-to-fiber-media-converters.php

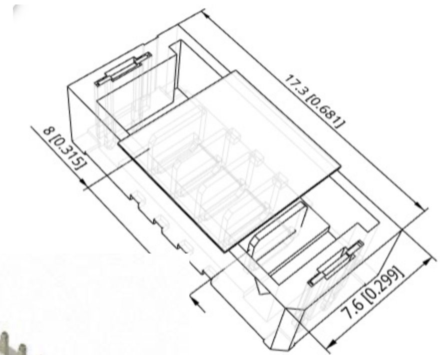


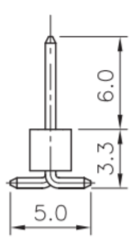
Power connector

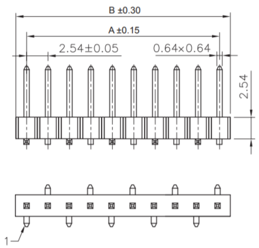
- Erni
  - 5 pin 18A/pin
  - https://www.erni.com/fileadmin/import/products/assets/DC0000110.PDF
- Samtec
  - UMPT-05-01.5-T-VT-SM-WT-K
  - 21A per pin
- JST
  - 455-1742-2-ND
  - 2A per pin
- WE
  - 732-5367-5-ND/732-2859-ND
  - 3A per pin





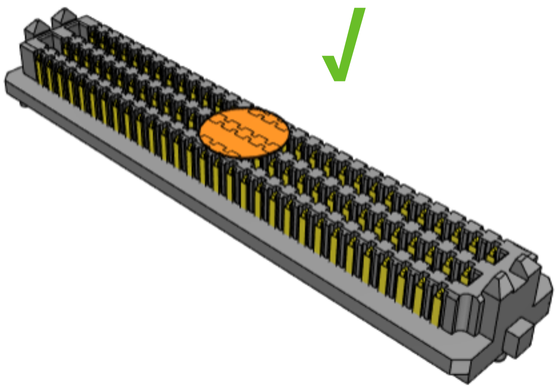






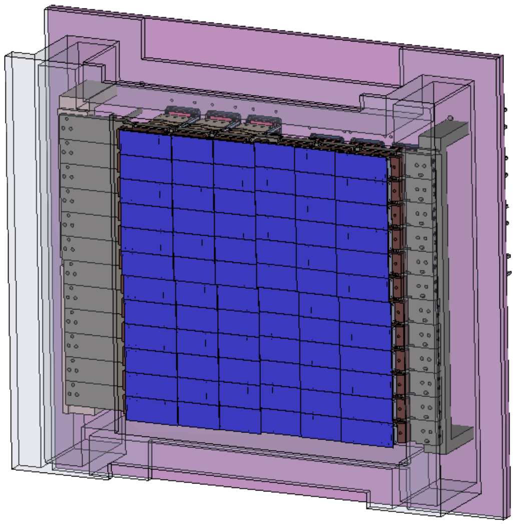
connectors

- Airborne
  - Mil standard
  - Low profile
  - Very reliable
  - Up to 100 pins
  - Cost is larger
- SEAM8 ✓
  - SEAM8-40-S02.0-L-06-2-K
    - Height is 2mm
  - 56Gpbs
  - 0.050” / 0.0315” pitch
  - Low insertion force
  - Up to 500 pins
  - Lower cost (~$15)

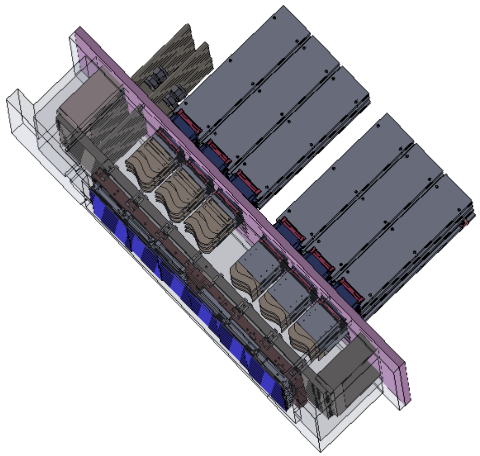


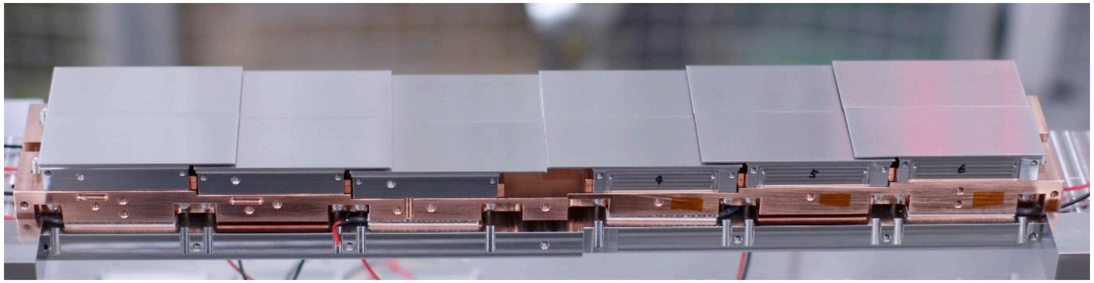
Example of a shingled camera (CITIUS - T. Hatsui)

Front view



Top view





Shingled ladder