ePixHR250M (ePixM): a soft X-ray CMOS imager for LCLS-II

LDAC 2020 – October 21st

L. Rota on behalf of SLAC Detector R&D Group

U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

Outline

- Project goals and requirements
- Detector concept
- Recommendations from LDAC 2019 review
- Progress made during the last year:
  - Thin entrance window for soft X-rays
  - ePixM Monolithic Active Pixel Sensor (MAPS)
  - ePixM back-end ASIC
- 1 Mpix ePixM shingled camera
- Risks and Mitigation
- Management Plan
- Status vs Requirements
- Take-away

Project Goal

- ePixM project aims at developing a high-rate camera for soft X-rays scattering/imaging experiments at LCLS-II

- Key detector for:
  - Soft x-ray (SXR) resonant elastic X-ray scattering (REXS) experiments in LCLS NEH 2.2
  - X-ray Photon Correlation Spectroscopy (XPCS)
  - Other Coherent Scattering (CS) experiments

Requirements table

Parameter	Threshold	Objective	REXS	XPCS	CS	1M ePixM
Pixel pitch [um]	50	50	✓	✓	✓	50
Read noise [e- rms]	15	10		✓	✓	12
Well depth [Number of 530eV photons]	1000	3000	✓	✓	✓	>1000
Quantum efficiency [%, 275eV-1500eV]	70	90	✓	✓	✓	~84
Frame-rate [kHz]	5	10	✓	✓	✓	7.5
Array size [pixels]	512x512	1024x1024	✓		✓	1152x1152
Vacuum outgassing rate [torr*L/s]	2E-8	1E-8	✓			2E-8
Cabling and cooling length [m]	2	4	✓		✓	2
Physical package envelope [WxLxD]	100x175x75 mm	75x150x50 mm	✓			100x175x75 mm
Maximum power dissipation [W]	100*	50	✓	✓	✓	250 (50*)

* Assuming a 512x512

Recommendations from LDAC 2019 review

SLAC

1. Prioritize the planned Feb 2020 **noise measurements** and work to understand any deviation from simulation. Approach simulation values as a guidepost, not as final result.

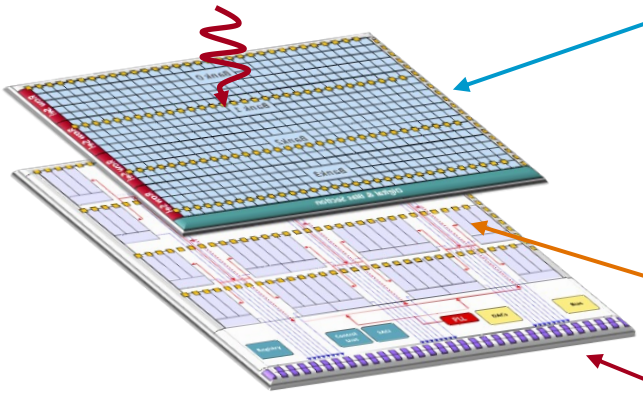
2. Describe the qualification path for **<500 eV X-ray QE** from ePixM.

3. If ePixM demonstrates promising noise and QE performance at the prototype stage, fully assess the engineering challenges and management approach for realizing the objective **1Mpix ePixM assembly** so that a well-informed decision can be made at the Nov. 2020 downselect.

Detector Concept

Standard modular hybrid approach

X-rays E_γ = 250 eV – 2keV



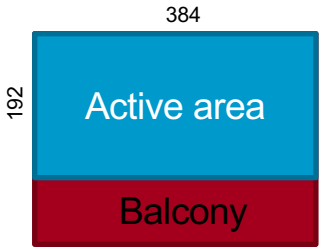
ePixM Monolithic Active Pixel Sensor (MAPS)

- On-sensors amplifier reduces noise → **demonstrated**
- Fully-depleted and back-illuminated → **demonstrated**
- Entrance window optimized for soft X-rays → **demonstrated**

Standard micro-bumps

ePixHR-M Readout ASIC (ROIC)

- 4 arrays of 192 ADCs
- Each array is a copy of the ePixHR back-end → **demonstrated**



CMOS sensor with 384 * 192 pixels.
- Size is 19.772 x 10.371 mm

ePixHR-M readout
- Size is 20.072 x 14.932 mm

ePixM MAPS: progress since LDAC 2019

LDAC 2019

1st prototype take-away

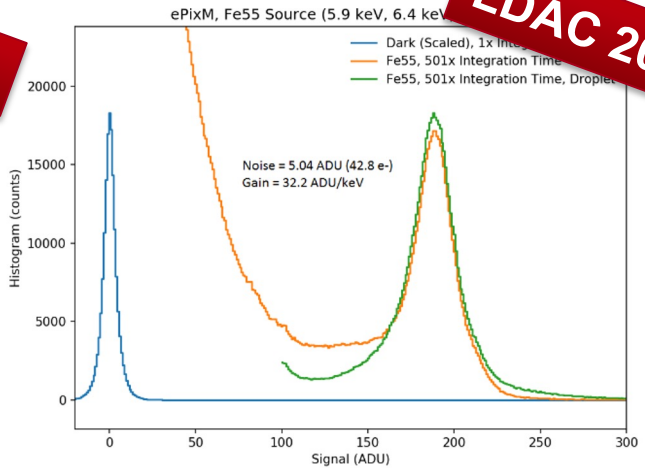
Detector R&D SLAC

First prototype works with 42 e^- noise.

Reason was discovered, design was fixed for 2nd prototype submission:

- $V_{breakdown}$= 20V versus the targeted 120V → Improved guard ring & p-stop layout
- Due to low $V_{breakdown}$, the capacitance is much larger which impacts the noise → TCAD simulations with new PDK from foundry.
- Gain stages were optimized compared to the first prototype which will result in better noise performance

LDAC 2019

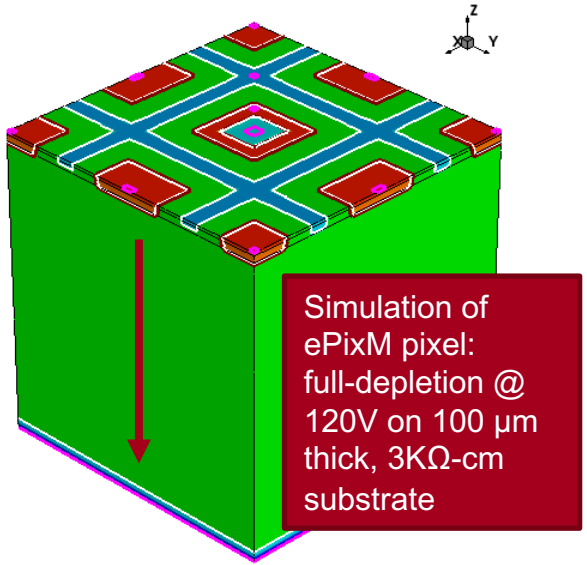


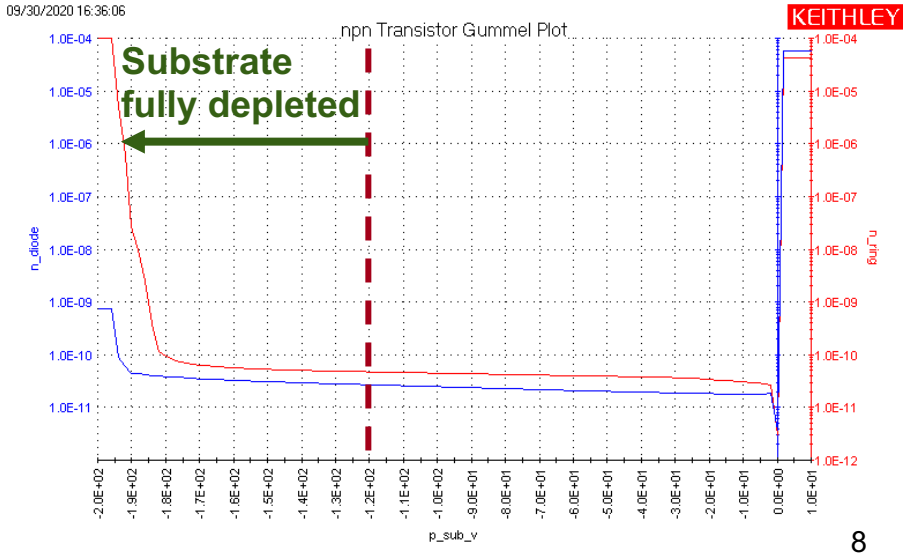
2nd prototype design efforts were directed towards:

1. Improving $V_{breakdown}$ to achieve full-depletion of substrate
2. Meeting noise performance requirements
3. Extending dynamic range through auto-gain switching

ePixM MAPS: IV curve

- Measured: 4.7K Ohm-cm substrate, backgrinded to 115 µm, implanted and MWA
- HV can be applied through different nodes:
  - pixel p-stop grid: $V_{breakdown}$ ~ 170-200 V
  - outer guard ring: $V_{breakdown}$ > 200 V
- Demonstrated: **full-depletion of substrate**

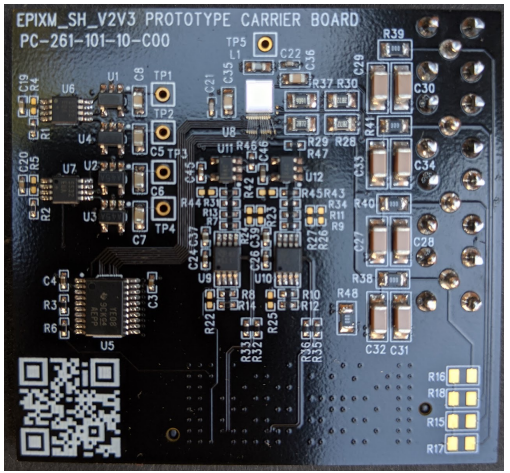




ePixM MAPS: small matrix measurements

How did we assess performance of monolithic active pixel sensor?

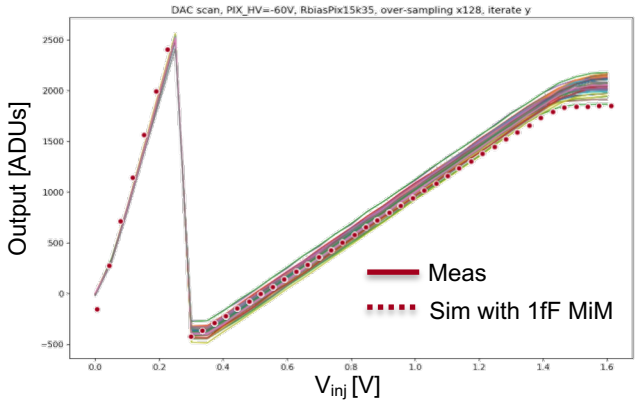
- Reticle included small prototypes with 48x48 matrix
- Wire-bonded to dedicated carrier board
- Read-out with ePixHR existing infrastructure
  - FPGA readout card
  - Firmware and software
- Three different versions, same as large-scale ones:
  - V1: no-autogain, most conservative design
  - V2: autogain, conservative design
  - V3: autogain, aggressive design
  - **All versions are fully functional**



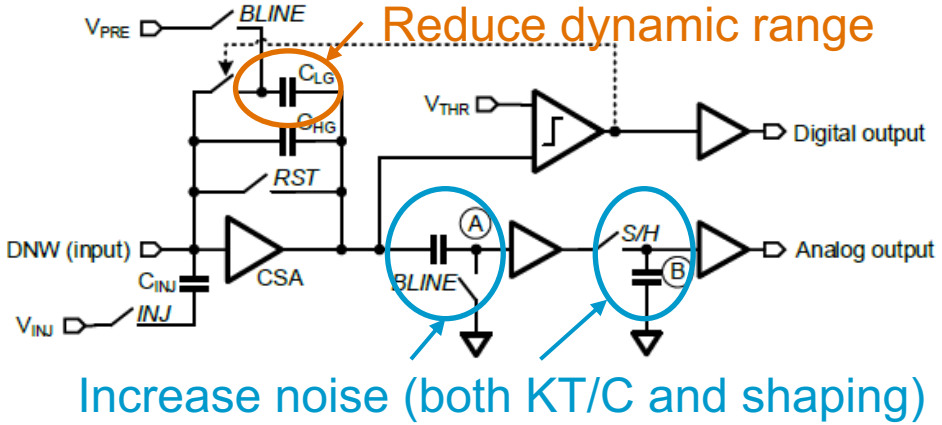
ePixM short sensor carrier board

MimCap density issue

- Pixel response from measurements did not match simulations
- Reason was discovered: wrong MIMcap density, 1fF/μm^2 instead of 2fF/μm^2
- Foundry confirmed issues during production → re-run in May, delivery in Nov 2020
- Caps are halved w.r.t. design → noise and dynamic range are severely affected
- Gain in HG not affected because capacitance is implemented as MOMcap



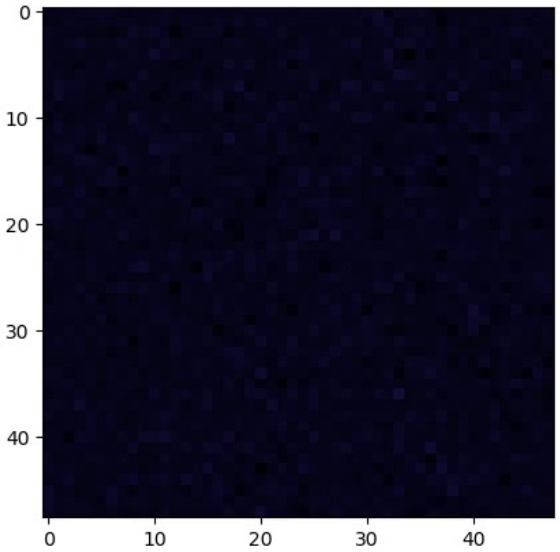
Pixel response with test-pulse injection: measurements vs simulation with 1fF MimCaps

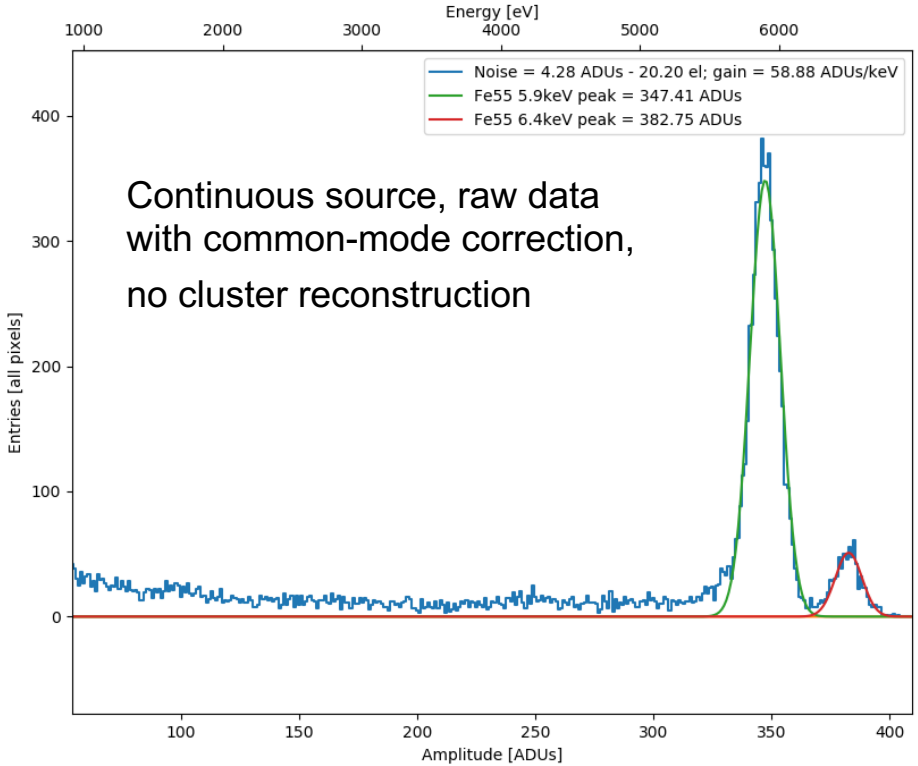


ePixM pixel schematics: capacitances implemented as MIMcaps are highlighted.

Measurements with Fe55 source

- ePixM_sh_V2 with auto-gain switchin
- Uncooled, bias = -60V
- **ENC = 15.7 e$^-$** @ *1 µs integration*



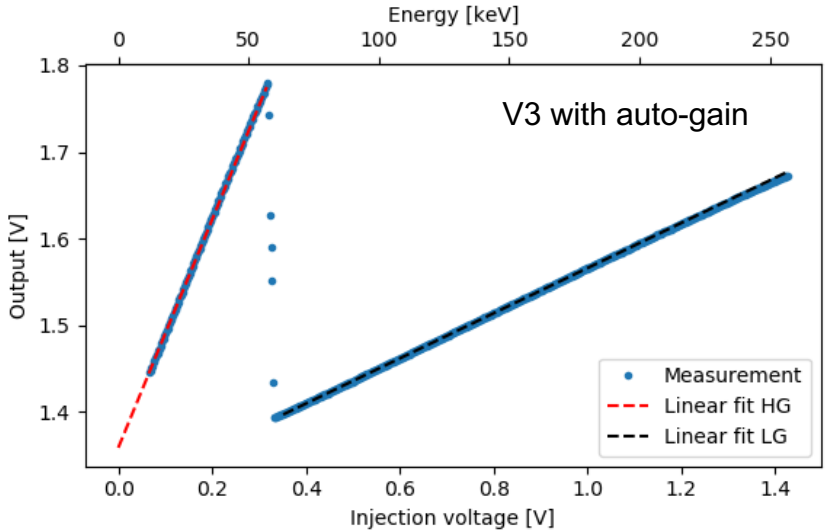


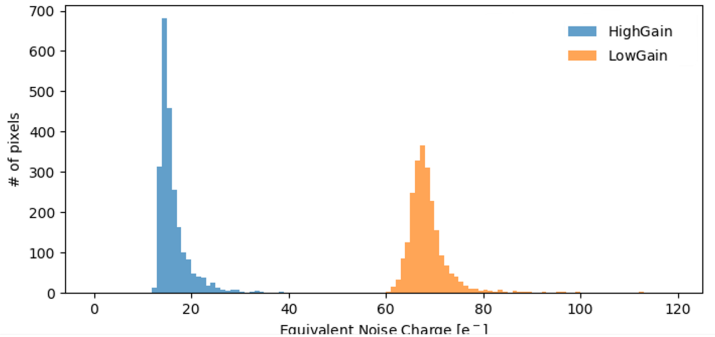
Fe55 spectrum measured with 20 µs integration time at room temperature.

Noise and dynamic range

- *Correlated pre-charging** functional: low-noise after gain switching achieved
- Good noise margin, can further extend dynamic range in LG in future versions

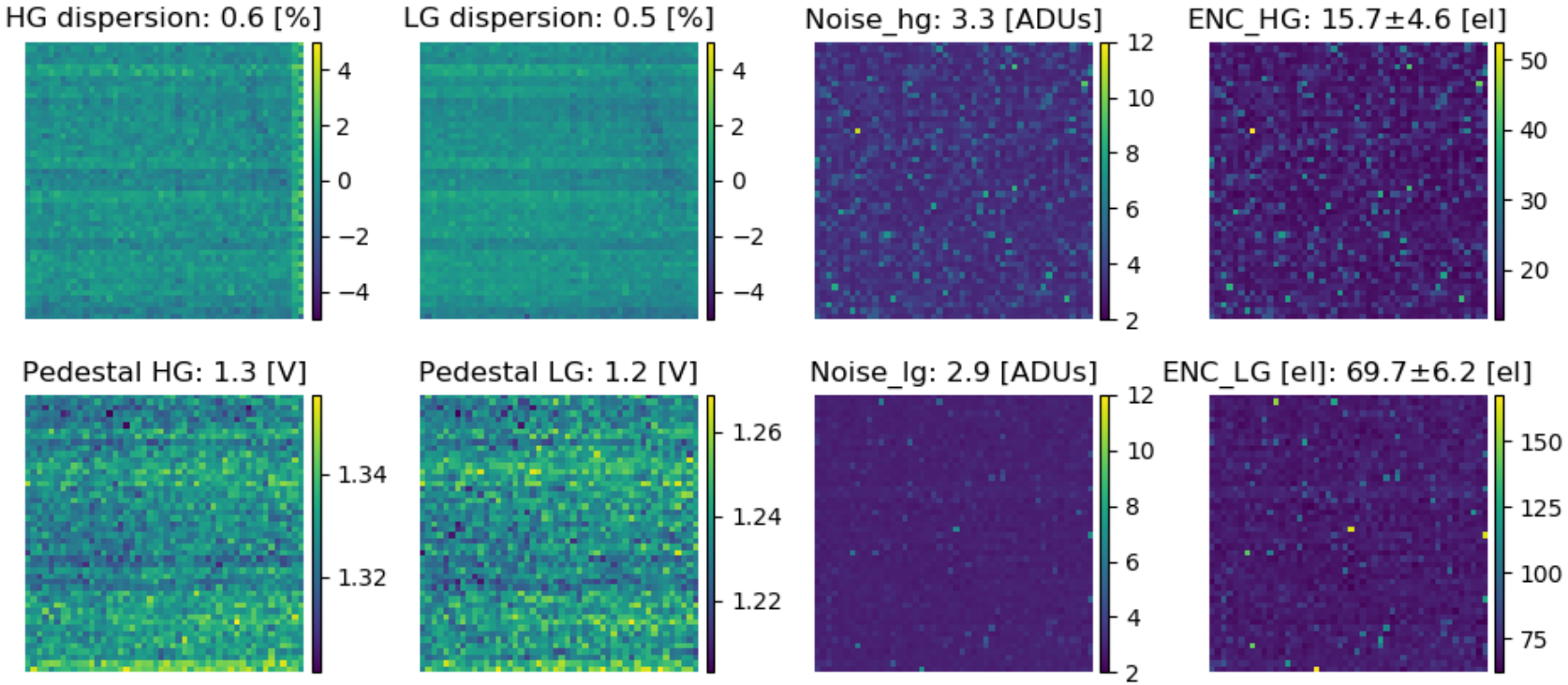
		Sim 2fF Cap	Meas 1fF cap
High gain	Range HG [keV]	50	50
	ENC [e^-]	11.3	15.7
	Single-ph. res. [e^-]	15	
Low gain	Range LG [keV]	500	250
	ENC [e^-]	90.8	60.7
	Statistical limit [e^-]	982	





*Rota L. *et al.*, Design of ePixM, a fully-depleted monolithic CMOS active pixel sensor for soft X-ray experiments at LCLS II, IWORID 2019

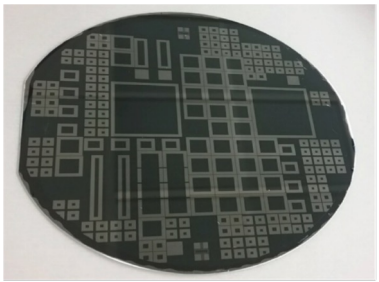
Gain uniformity: better than 1%



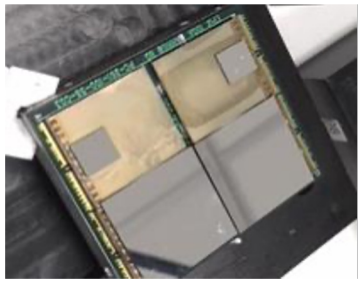
Soft X-ray entrance window

LDAC 2019

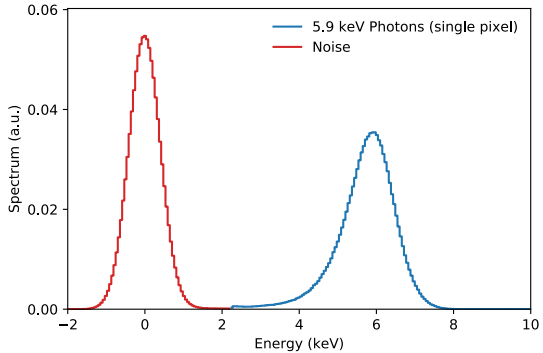
- Novel micro-wave annealed (MWA) entrance window process developed at SLAC
- Enables dopant activation without high temperature
  - Activates dopant without driving profile deeper → create shallow entrance window
  - No damage to existing structures → we can post-process at SLAC backside of foundry processed CMOS sensors
- X-ray sensor with micro-wave annealed arsenic implanted entrance window has been demonstrated (see spectrum)



Si sensor wafer for ePix detectors processed with thin-entrance window



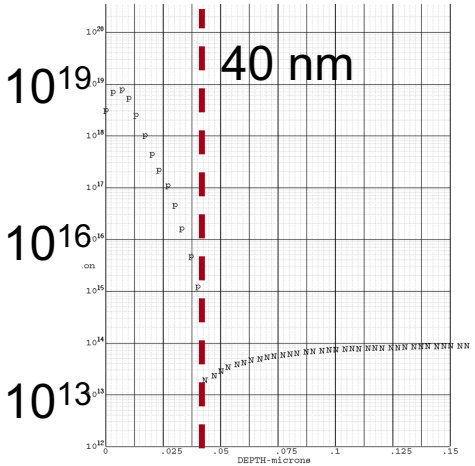
Sensors mounted on ePix250s



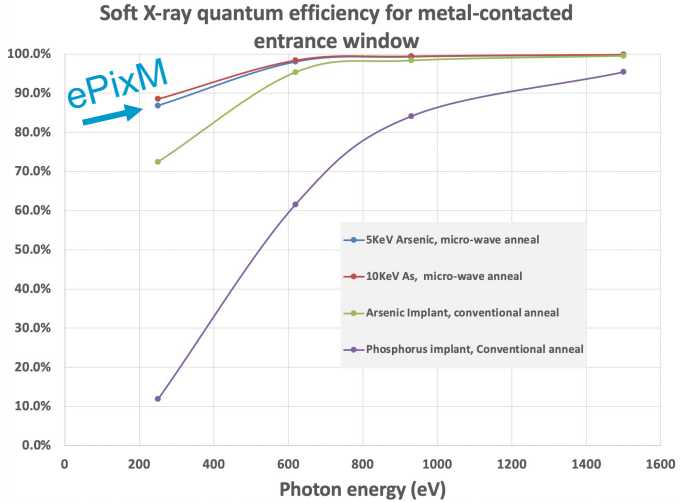
Fe-55 spectrum with MWA entrance window

Soft X-ray entrance window

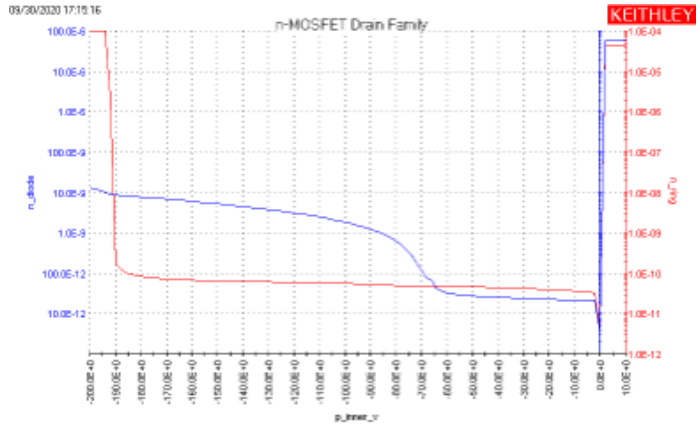
- ePixM requires Boron entrance window
- SRP of BF2 implanted on test wafer: “40 nm” entrance window achieved
- IV curve on implanted & annealed ePixM diodes/short prototypes → **no degradation**



SRP of 20KeV BF2 implanted test wafers after anneal



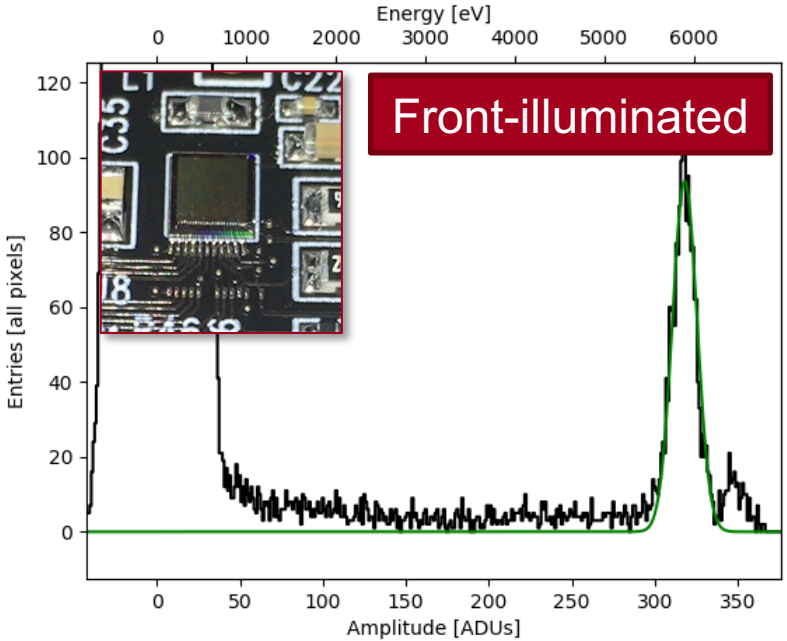
Simulated quantum efficiency for *n*-type entrance windows. ePixM BF2 profile is comparable to the 5KeV Arsenic profile.

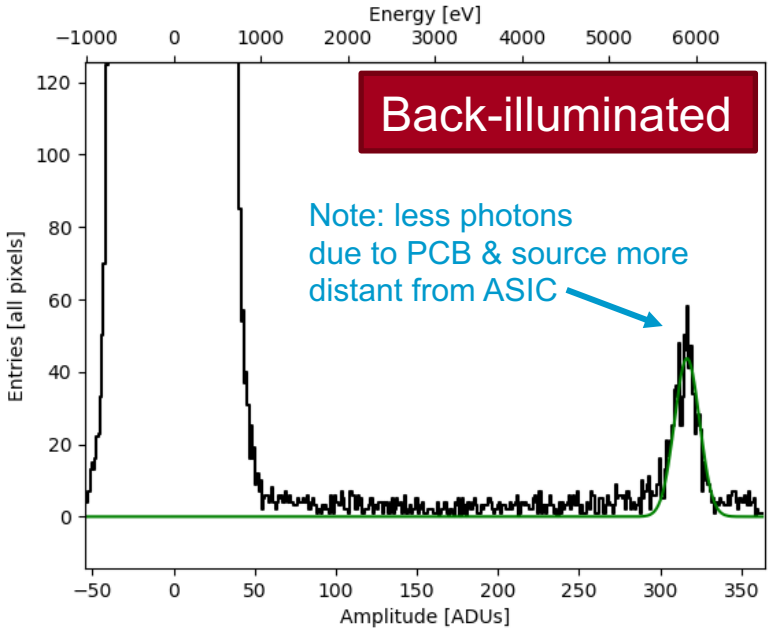


IV Curve of diode on ePixM wafer

Fe55 spectrum with thin entrance window

- Update 12 Oct: **ePixM MAPS with thin entrance window are fully functional**





Note: uncooled, -120V bias, continuous source, raw data with no cluster reconstruction

ePixM MAPS - QE characterization

ePixM devices with thin-entrance window for characterization:

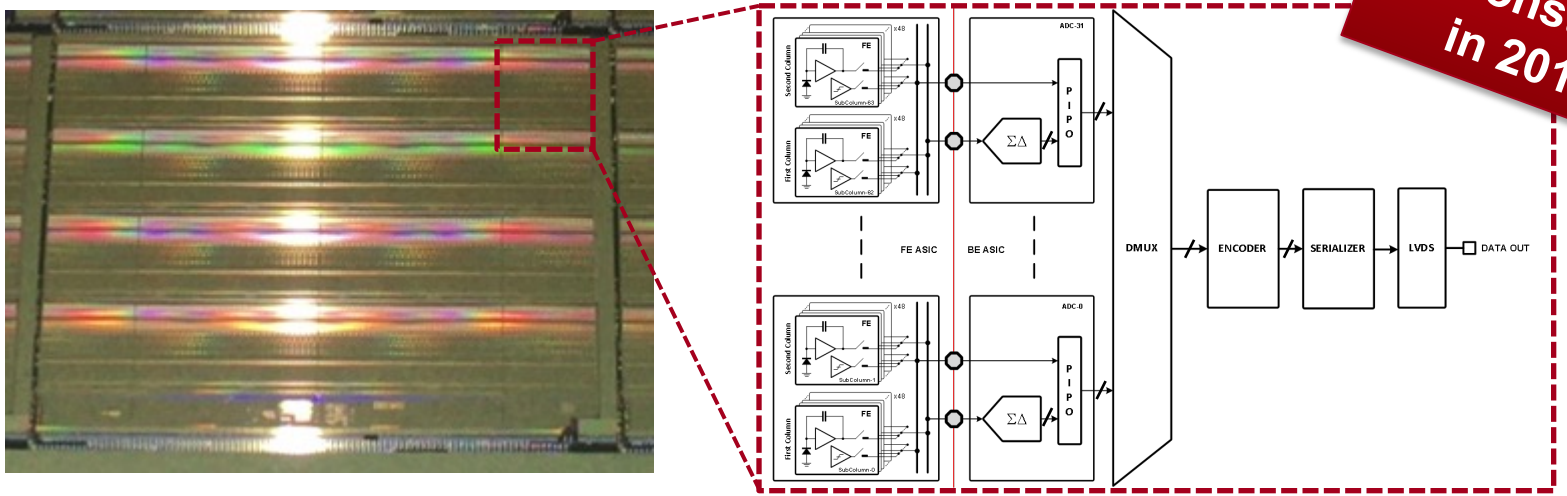
- Diodes: 1x1 mm^2
- Small matrix: 48x48 (functional)
- Large matrix bonded ePixHR-M back-end: 384x192 (in testing)

Plan for QE characterization:

- Measure QE at ALS metrology beamline against calibrated diode
- Calibrate QE uniformity
- Final flat-field calibration of the camera QE for different pixels/dies/etc.

ePixHR-M back-end ASIC

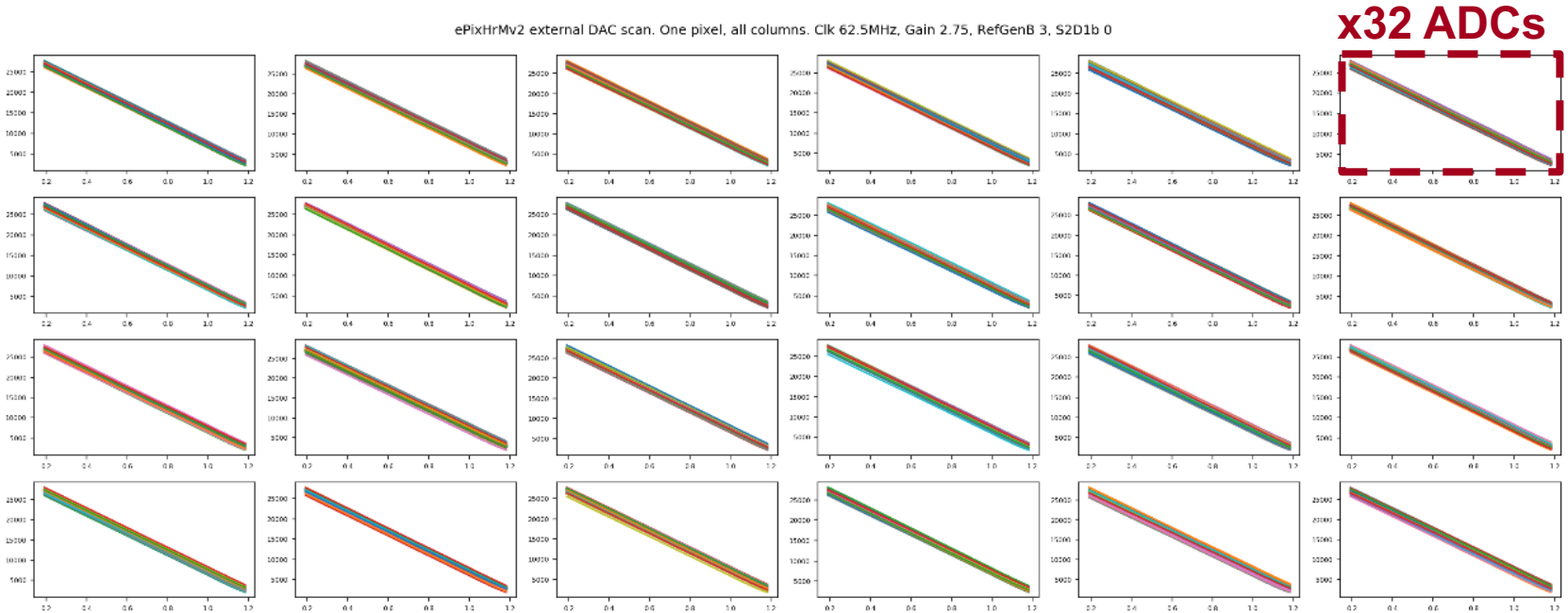
Already demonstrated in 2018



- 4 banks of 192 1-MHz, 14-bit ΣΔ Analog to Digital Converters (ADC)
  - Same ADC channel circuit/layout used for ePixHR (see ePixHR talk)
- 2 micro-bumps every ΣΔ ADC serving two column of 96 pixels
  - Simpler bump-bonding assembly than standard ePixs
- Other blocks: PLL, Control Unit, Registers, SPI interface, BGR, Bias, DACs, Pulser, etc.

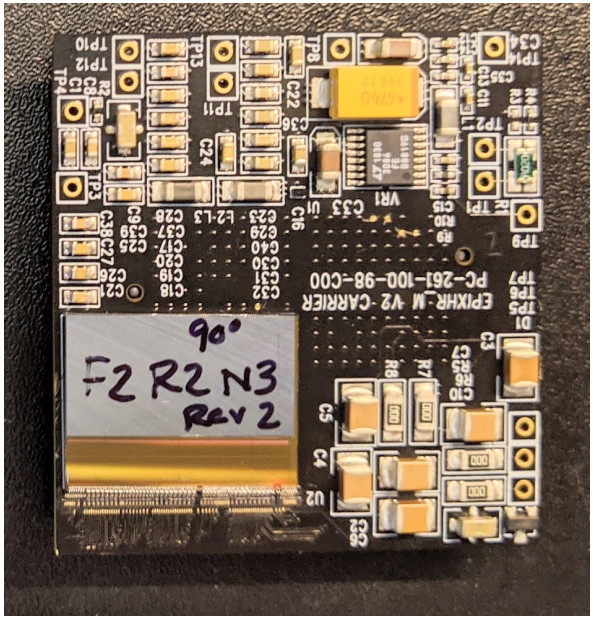
ePixHR-M back-end ASIC

- All banks (4 rows, 192 ADCs each) functional
- See ePixHR talk for more details on ΣΔ ADC performance



Assembled

- Status @ 1st Oct: received ePixHR-M back-end ASIC bump-bonded to ePixM MAPS, wire-bonded to carrier boards
- We expect first results in a few weeks



ePix carrier board with ePixM MAPS bonded on ePixHR-M back-end

1Mpix ePixM shingled camera

SLAC

LDAC 2019 – recommendation from review panel:

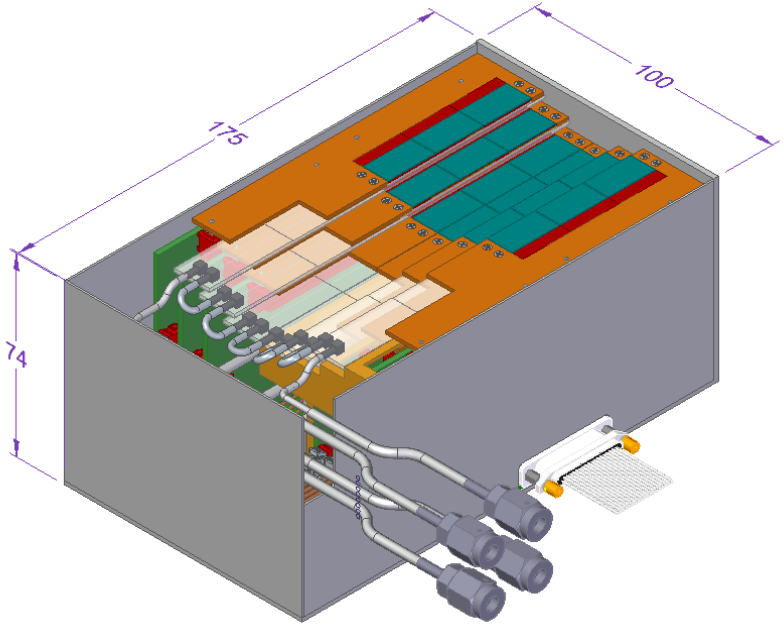
"fully assess the engineering challenges and management approach for realizing the objective 1Mpix ePixM assembly so that a well-informed decision can be made at the Nov. 2020 downselect"

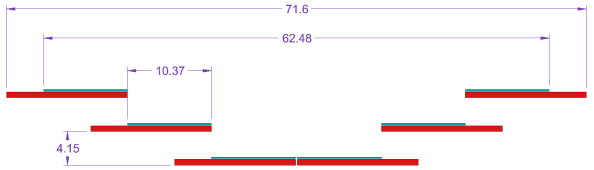
Camera design:

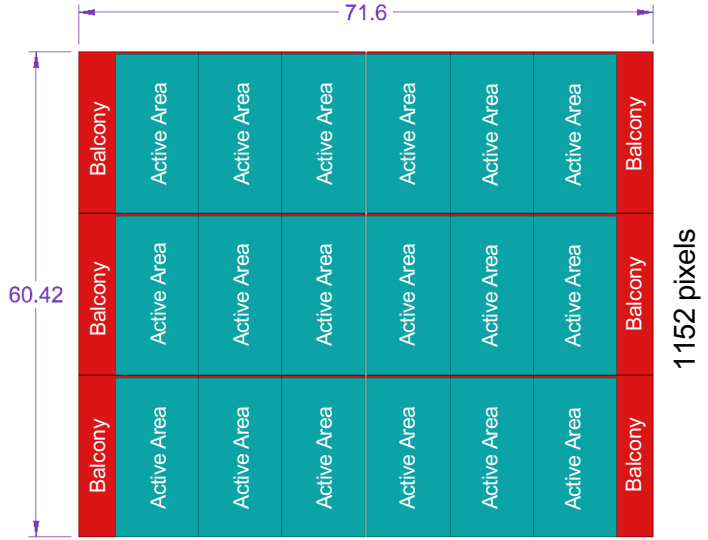
- Started design of ePixM 1Mpix shingled camera in summer 2020
- ePixM design will serve as a baseline for other ePix cameras (*e.g.* ePixHR)
- Design covers all critical aspects:
  data I/O, cooling, mechanics, cabling, integration with beamline instrumentation
- CDR started on 2nd Oct 2020 with LCLS & TID reviewers

1Mpix ePixM shingled camera

- Shingled assembly to maximize fill factor
- Overall dimensions compatible with requirements:
  175 x 100 x 75 mm

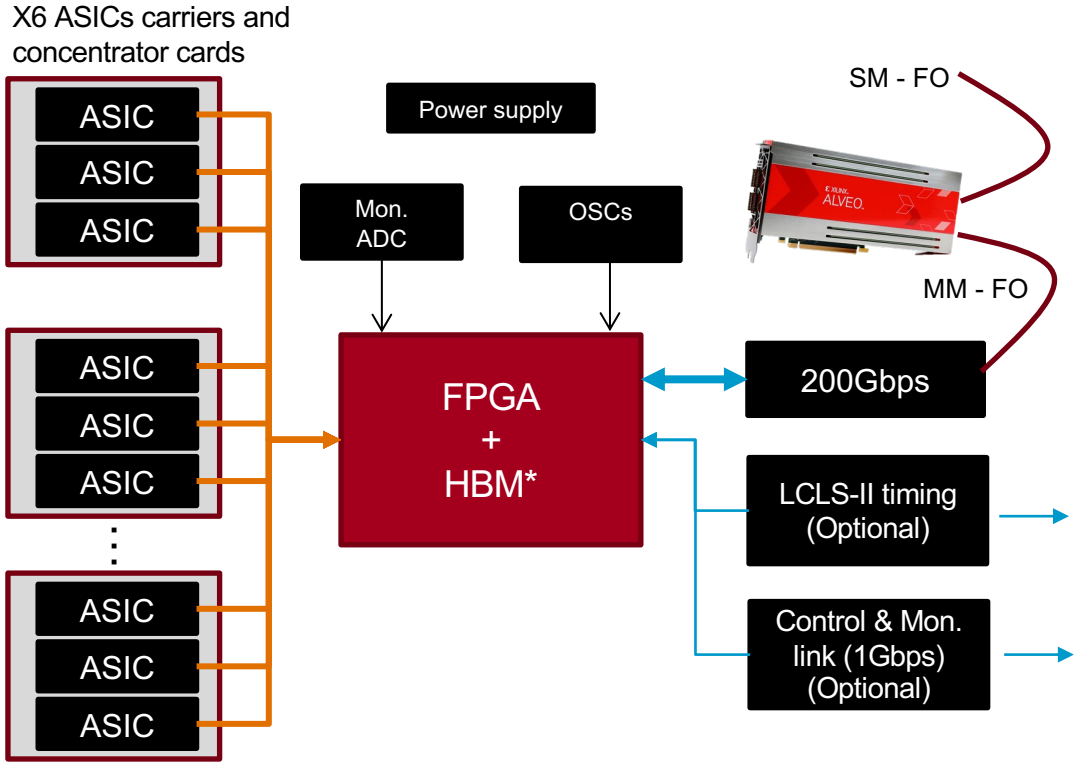






1152 (active area of ~ 57.2mmx 57.2mm)

Data flow

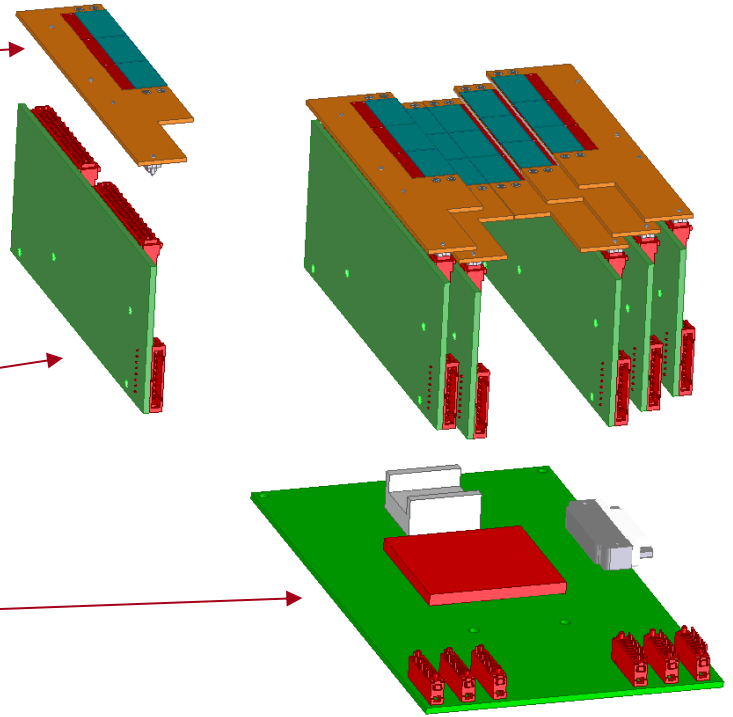


- Each ASICs carrier board is connected to a concentrator card
- Concentrator I/O requirements:
  - 144 IO/module
    (24 x 2 IOs per line x 3 ASICs x 1 modules)
  - 23 IO/module for ASIC control
  - Analog monitoring ADC IOs
  - Digital monitoring IOs
- Data volume at 7.5kFPS
  - **28Gbps/per concentrator module**
    (384*192 pixels * 3 ASICs * 16 b * 7.5kFPS, 66b/64b)
  - **168Gbps/per camera**
    (384*192 pixels * 18 ASICs * 16 b * 7.5kFPS, 66b/64b)
- Data transmission **200Gbps** out
  (8x25Gbps lanes out of 12 available lanes)

*High Bandwidth Memory can be used to improve on camera processing

Camera components

- x6 ASICs carrier boards
  - L+R versions
  - Characterized and tested independently from the rest of assembly
  - Board hosting the most delicate components → must be replaceable
- x6 Data concentrator cards
  - Analog + Digital I/Os
  - Voltage regulators
- x1 Motherboard
  - Data concentrator
  - Optical I/Os 200 Gbps



Carrier board and cold plate

Sensors/ASICs

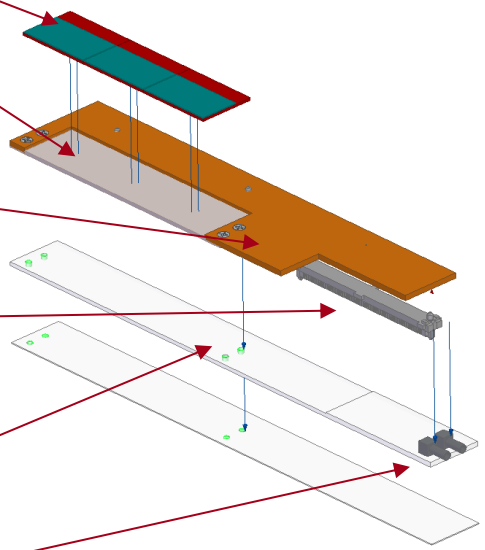
SiC thermal spreader bonded to the carrier

Kapton carrier

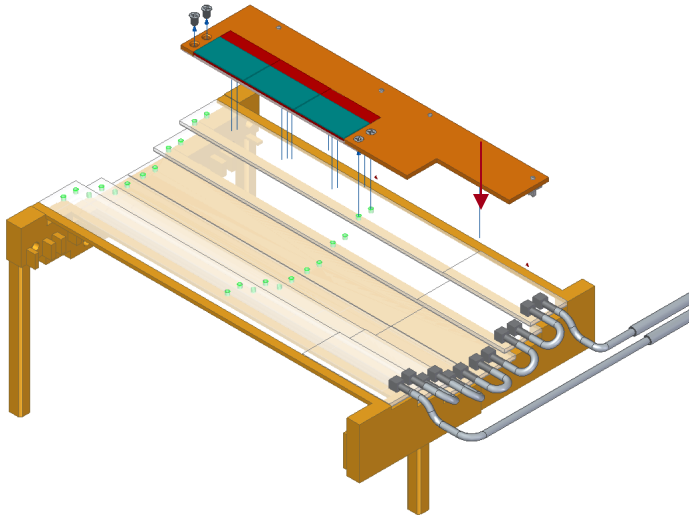
Electrical connector

Micro-channeled active spreader on the cold plate

Cooling fittings



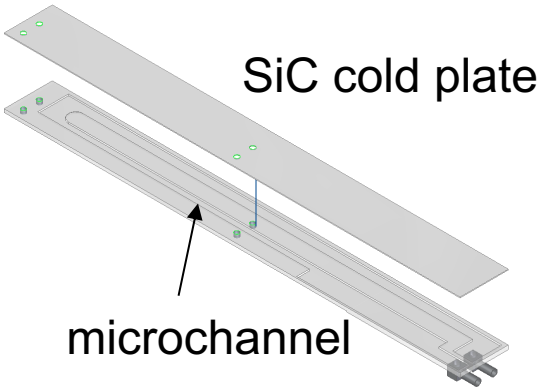
- The detector modules are individually fastened to the cold plate to allow the installation and the replacement of single units.
- The micro-channeled heat spreaders are bonded to a support structure and serially connected to the cooling manifold.

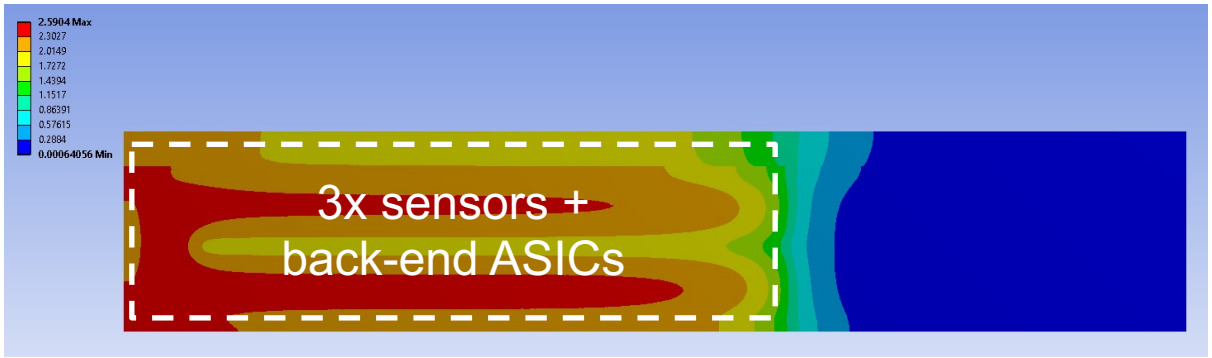


Cold plate design made of bonded low-CTE parts, ideally Silicon Carbide or SiC and Titanium.

Carrier board cooling

- Cooling requirements:
  - Cool MAPS + HRM back-end ASICs (2.4 W/cm^2)
  - Operating temperature: threshold -20°C, target -40°C (15.7 el measured @ room-temp)
- Operation in vacuum requires direct cooling, no-convection
- Technology: active evaporative cooling with microchannels directly under the sensors
- Same technology is used as baseline solution for all LHC experiments
- Similar implementation and setup done @ SLAC for ATLAS detector

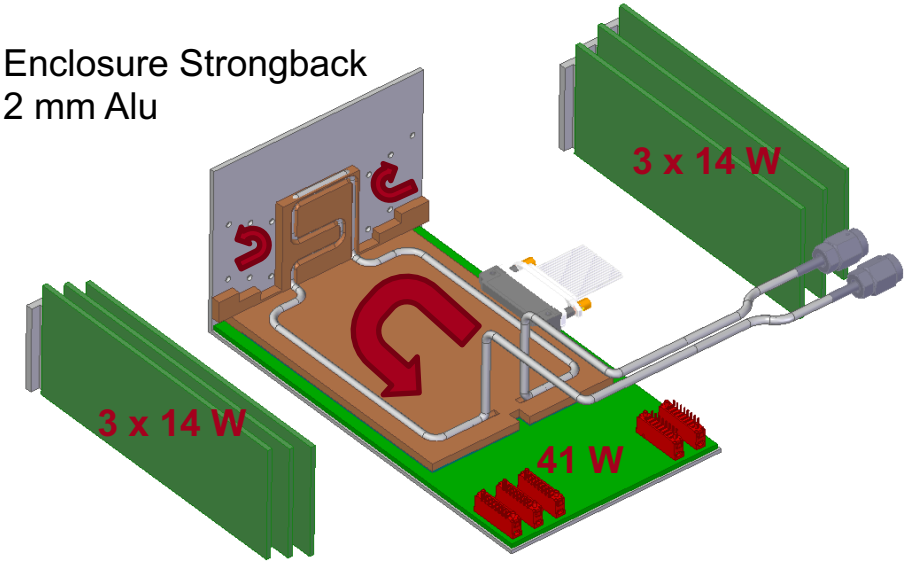


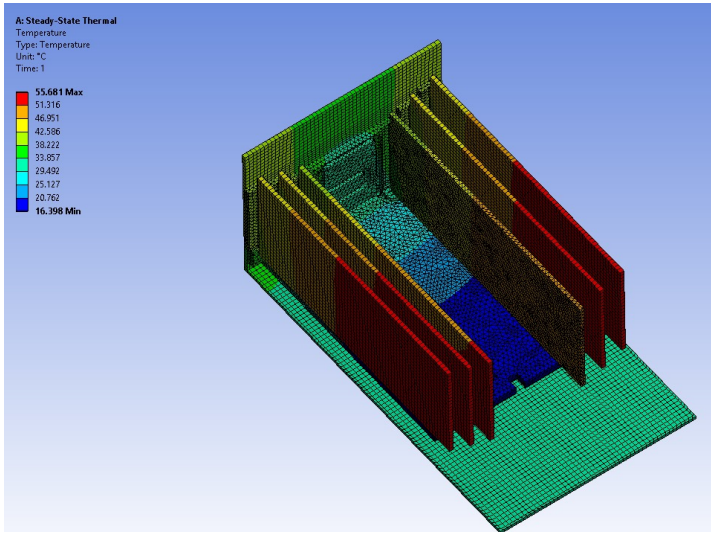


Concentrator cards & mother board cooling

- Requirement: remove heat and keep the R/O electronic below the max. op. range. ~70 C
- Total Heat load = 125 W
- Active cold plate on a cooling loop independent from the sensors primary

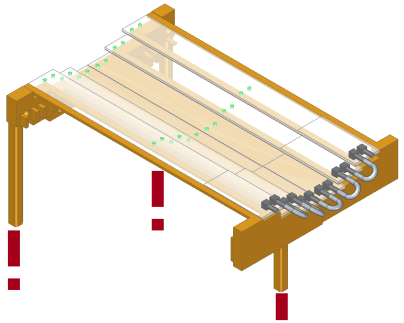
Enclosure Strongback
2 mm Alu



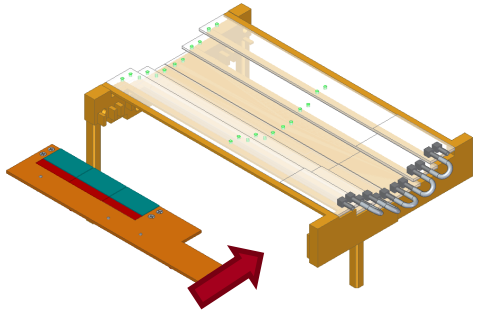


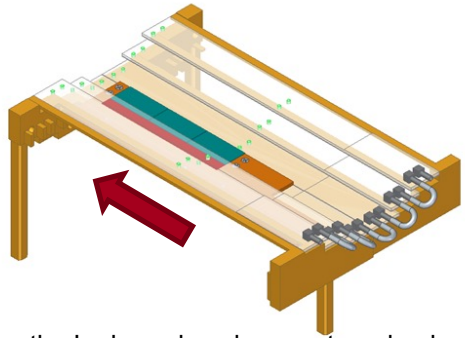
Assembly procedure (simplified)

The Detector Cold Plate is secured to the assembly fixtures (granite table) and lifted up on ~2” posts

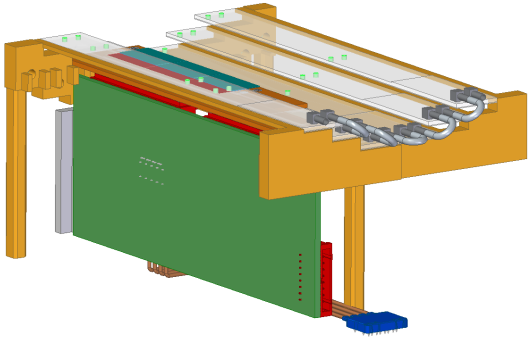


The carrier board is inserted horizontally from the two sides and brought to the final position with two lateral movements in the horizontal plan.



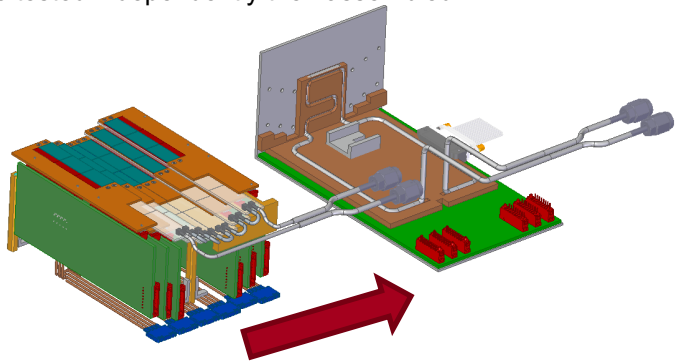


The Concentrator Board is connected once the Carrier Board is fastened to the cold plate.



...
x6

The Motherboard is pre-assembled and tested on the L-shaped enclosure strongback. The two pieces are tested independently then assembled.

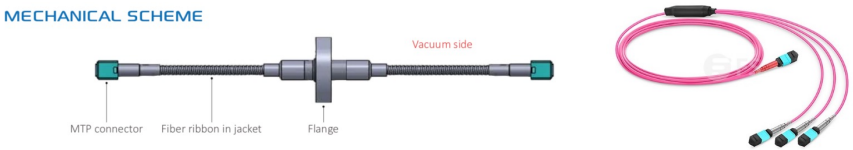


Cabling

- Selected power supply and fiber optics cables
- Compatible with requirements and in-vacuum operation

Fiber optics

RETA-RIB-CF40-12-050a-2-S48-11b



https://www.lasercomponents.com/fileadmin/user_upload/home/Datasheets/sedi/fibre-optic-ribbon-hermetic-feedthroughs.pdf

Power supply

High Temperature Cable Connector, Low Profile with Radius (PLUG)

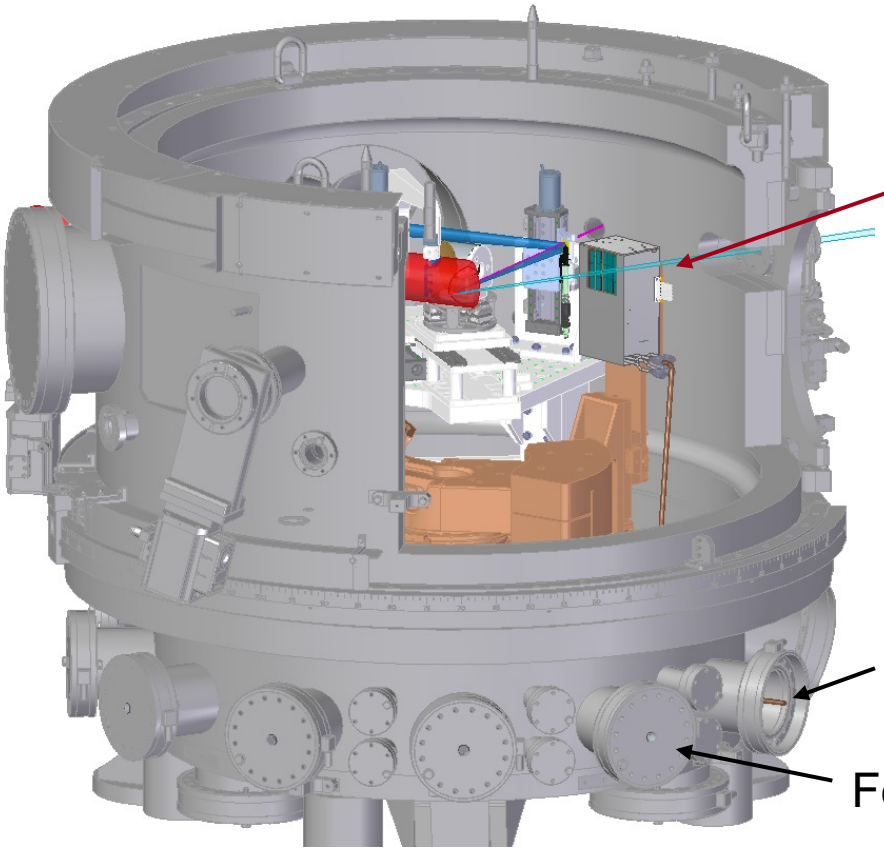
MTHT-21, 31, High Temperature Cable Connector with a Low Profile and Radius, Plug, 2, 3-Row, Sizes: 9-51 | M Series

A family of high temperature low profile male cable connectors that have 2 and 3 rows of contacts spaced at 0.050". These connectors can be located along concave surfaces such as the inside wall of a tube/pipe. They are available in sizes ranging from 9 to 51 contacts.

Vin 48V
I/supply (2 wires) <1A
Wire thickness is 26AWG

Max length of 120” (3m)
Max drop per wire of 0.4V

Integration with the RIXS instrument



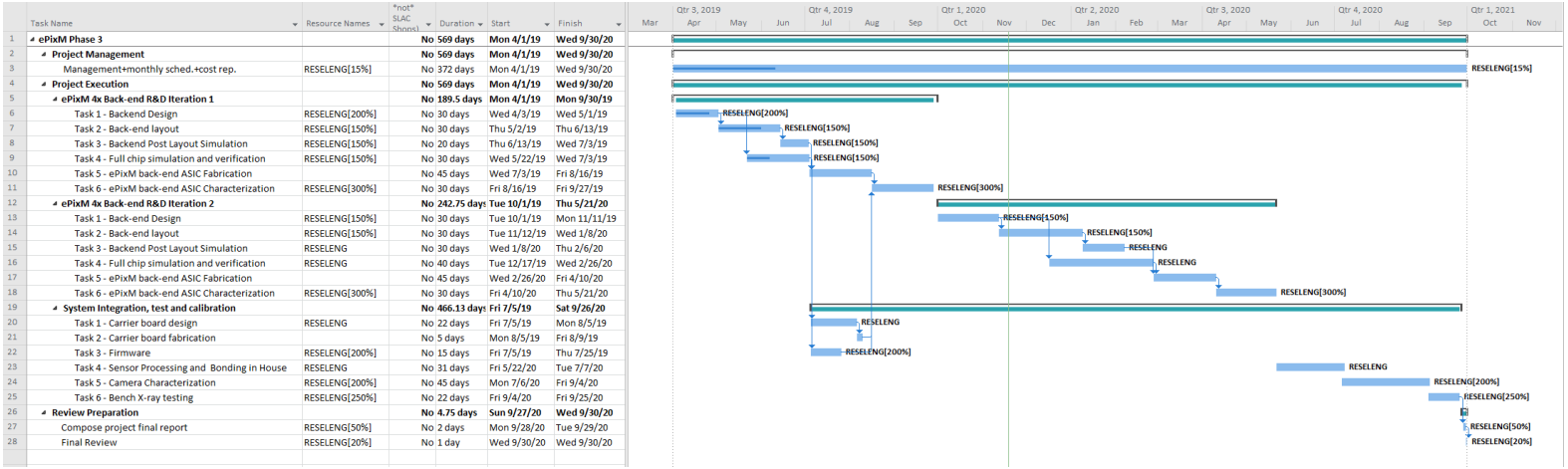
- Distance Camera-flanges ~ 1 m
- Expected +500 mm slack for the On-OFF beam motion

Feedthrough 6” Flange - Cooling

Feedthrough 6” Flange - Cables

Management plan

- SLAC Detector R&D projects follow LCLS project management guidelines
  - CDR conducted before project starts
  - Financial plan approved by the PEC before start
  - Documented using Microsoft Project
  - Bi-weekly meetings to follow status are conducted together with the project sponsor (LCLS)
  - Milestones are tracked and if requires re-baselines or the project are implemented



	Task Name	Resource Names	*not* SLAC Shops\	Duration	Start	Finish
1	ePixM Phase 3		No	569 days	Mon 4/1/19	Wed 9/30/20
2	Project Management		No	569 days	Mon 4/1/19	Wed 9/30/20
3	Management+monthly sched.+cost rep.	RESELENG[15%]	No	372 days	Mon 4/1/19	Wed 9/30/20
4	Project Execution		No	569 days	Mon 4/1/19	Wed 9/30/20
5	ePixM 4x Back-end R&D Iteration 1		No	189.5 days	Mon 4/1/19	Mon 9/30/19
6	Task 1 - Backend Design	RESELENG[200%]	No	30 days	Wed 4/3/19	Wed 5/1/19
7	Task 2 - Back-end layout	RESELENG[150%]	No	30 days	Thu 5/2/19	Thu 6/13/19
8	Task 3 - Backend Post Layout Simulation	RESELENG[150%]	No	20 days	Thu 6/13/19	Wed 7/3/19
9	Task 4 - Full chip simulation and verification	RESELENG[150%]	No	30 days	Wed 5/22/19	Wed 7/3/19
10	Task 5 - ePixM back-end ASIC Fabrication		No	45 days	Wed 7/3/19	Fri 8/16/19
11	Task 6 - ePixM back-end ASIC Characterization	RESELENG[300%]	No	30 days	Fri 8/16/19	Fri 9/27/19
12	ePixM 4x Back-end R&D Iteration 2		No	242.75 days	Tue 10/1/19	Thu 5/21/20
13	Task 1 - Back-end Design	RESELENG[150%]	No	30 days	Tue 10/1/19	Mon 11/11/19
14	Task 2 - Back-end layout	RESELENG[150%]	No	30 days	Tue 11/12/19	Wed 1/8/20
15	Task 3 - Backend Post Layout Simulation	RESELENG	No	30 days	Wed 1/8/20	Thu 2/6/20
16	Task 4 - Full chip simulation and verification	RESELENG	No	40 days	Tue 12/17/19	Wed 2/26/20
17	Task 5 - ePixM back-end ASIC Fabrication		No	45 days	Wed 2/26/20	Fri 4/10/20
18	Task 6 - ePixM back-end ASIC Characterization	RESELENG[300%]	No	30 days	Fri 4/10/20	Thu 5/21/20
19	System Integration, test and calibration		No	466.13 days	Fri 7/5/19	Sat 9/26/20
20	Task 1 - Carrier board design	RESELENG	No	22 days	Fri 7/5/19	Mon 8/5/19
21	Task 2 - Carrier board fabrication		No	5 days	Mon 8/5/19	Fri 8/9/19
22	Task 3 - Firmware	RESELENG[200%]	No	15 days	Fri 7/5/19	Thu 7/25/19
23	Task 4 - Sensor Processing and Bonding in House	RESELENG	No	31 days	Fri 5/22/20	Tue 7/7/20
24	Task 5 - Camera Characterization	RESELENG[200%]	No	45 days	Mon 7/6/20	Fri 9/4/20
25	Task 6 - Bench X-ray testing	RESELENG[250%]	No	22 days	Fri 9/4/20	Fri 9/25/20
26	Review Preparation		No	4.75 days	Sun 9/27/20	Wed 9/30/20
27	Compose project final report	RESELENG[50%]	No	2 days	Mon 9/28/20	Tue 9/29/20
28	Final Review	RESELENG[20%]	No	1 day	Wed 9/30/20	Wed 9/30/20

Risk management

Risk	Likelihood/Impact	Mitigation	Status
Unexpected complexity in the design	**Low/Medium** Schedule delay and increased cost.	**Accept without mitigation**	**Retired**
First Iteration full size CMOS sensor has bugs	**Medium/Medium** Would need to another fabrication effort which is planned in the budget.	**Multiple variants** **Second iteration in the budget.**	On-schedule to be retired by end 2020
First Iteration Back-end Design has bugs	**Medium/Medium** Would need to another fabrication effort which is planned in the budget.	**Second iteration in the budget.**	On-schedule to be retired by end 2020
Second Iterations have bugs	**Low/High** Schedule delay and increased cost.	**Accept without mitigation**	**Active**
Carrier board has defects	**Low/Low** *Negligible delay and cost increase.*	**Accept without mitigation**	**Retired**
Sensor post processing (Entrance Window)	**Medium/Medium** Schedule delay and increased cost.	**Accept without mitigation**	**Retired**
Parts reused from other projects (ePixHR)	**Medium/Medium** Schedule delay and increased cost.	**Accept without mitigation**	**Retired**
Cooling system does not meet requirements	**Medium/Medium** Schedule delay and increased cost.	**Accept, prototype demonstrator as soon as possible**	**Active**

Status vs requirements: on-track to be met

Parameter	Threshold	Objective	1M ePixM	Status
Pixel pitch [um]	50	50	50	50
Read noise [e^- rms]	15	10	12	15.7[a] (uncooled)
Well depth [Number of 530eV photons]	1000	3000	>1000	500[a]
Quantum efficiency [%, 275eV-1500eV]	70	90	~84	84% sim, to be meas
Frame-rate [kHz]	5	10	7.5	to be meas
Array size [pixels]	512x512	1024x1024	1152x1152	addressed in camera study
Vacuum outgassing rate [torr*L/s]	2E-8	1E-8	2E-8	addressed in camera study
Cabling and cooling length [m]	2	4	2	addressed in camera study
Physical package envelope [WxLxD]	100x175x75 mm	75x150x50 mm	100x175x75 mm	addressed in camera study
Maximum power dissipation [W]	100[b]	50	250[b] (50)	addressed in camera study

[a] Affected by foundry's mistake on MiMCap density. New wafers are expected in November 2020 with correct MIMCaps and better noise/dynamic range performance.
[b] Assuming a 512x512 array

Take-away

- ***Are the science requirements and detector performance parameters fully described and self-consistent?***
  - ePixM is designed to meet the requirements for REXS experiments at LCLS-II
  - Performance parameters aligned to meet requirements
- ***Is the development plan sound, with regard to mitigating technical risk and timely delivery? Are the presented results on track with the development plan? Are the management plans appropriate?***
  - Development is on track. Several risks retired, mitigation in place.
    - MAPS sensor:
      - Pixels characterized: **full depletion, noise = 15.7 el., max 500 photons** (we expect significant improvements in Nov 2020 with new wafers with correct MIMcap density), **thin entrance window @ SLAC**
      - Full-size matrix with ePixHR-M back-end ASIC: received assembled modules, in testing
    - Digital Electronics boards/mechanical prototype camera mechanical/thermal parts: ready
    - 1Mpix shingled camera study **investigated all critical aspects of design: data I/O, cooling, mechanics, etc…**
  - Project managed according to LCLS management protocol
- ***Is the choice of this type of detector consistent with the decade-level long-range development strategy, or is there a good reason why a different path has been chosen?***
  - ePixM is natively part of the ePix family and follows the long term upgrade plan