ePixHR250M (ePixM): a soft X-ray CMOS imager for LCLS-II

December 3, 2019

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U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

Outline

- Motivations
- Requirements Table
- Development
  - Concept
  - Development plan
  - Technical Approach and achievements
- Status vs Timeline
- Next steps
- Risks and Mitigation
- Outlook (Long Term)
- Management Plan
- Summary

Project Goal

- ePixM project aims at developing a high-rate camera for soft X-rays scattering/imaging experiments at LCLS-II

- Key detector for:
  - Soft x-ray (SXR) resonant elastic X-ray scattering (REXS) experiments in LCLS NEH 2.2
  - X-ray Photon Correlation Spectroscopy (XPCS)
  - Other Coherent Scattering (CS) experiments

Requirements Table

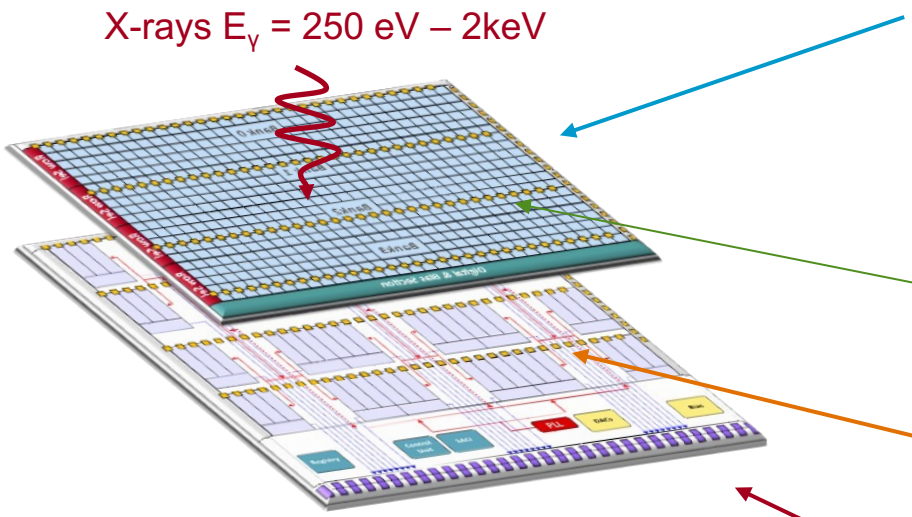
Parameter	Threshold	Objective	REXS	XPCS	CS	1M ePixM
Pixel Pitch (um)	50	50	✓	✓	✓	50
Read Noise (e- rms)	15	10		✓	✓	12
Quantum efficiency (%, 275eV-1500eV)	70	90	✓	✓	✓	~84
Frame Rate (kHz)	5	10	✓	✓	✓	7.5
Array size (pixels)	512x512	1024x1024	✓	✓	✓	1152x1152
Well Depth (Number of 530eV photons)	1000	3000	✓		✓	>1000
Vacuum outgassing rate (torr*L/s)	2E-8	1E-8	✓			2E-8
Cabling and cooling length (m)	2	4	✓		✓	2
Physical package envelope (WxLxD, mm)	100x175x75mm	75x150x50mm	✓			100x175x75mm
Maximum Power dissipation (W)	100*	50	✓	✓	✓	200 (50*)

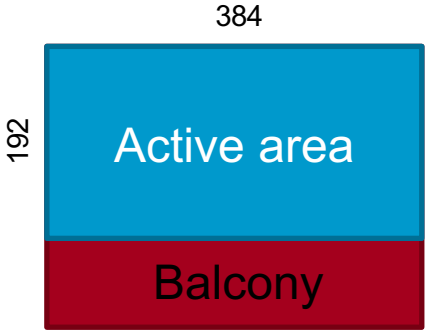
* Assuming a 512x512

Detector Concept

Standard modular hybrid approach

Core module architecture:





CMOS sensor with 384 * 192 pixels.
- Size is 19.772 x 10.371 mm

ePixHR-M readout
- Size is 20.072 x 14.932 mm

ePixM monolithic front-end

Fully depleted CMOS Image Sensor with front-end circuitry
- on-sensors amplifier reduces input detector capacitance and thus noise
- Back-thinned and back illuminated
- Entrance window optimized for soft X-rays (demonstrated)

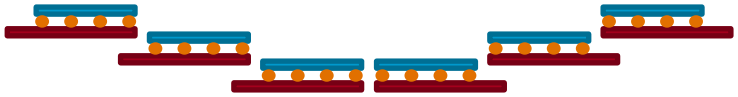
Standard micro-bumps

Readout ASIC (ROIC)

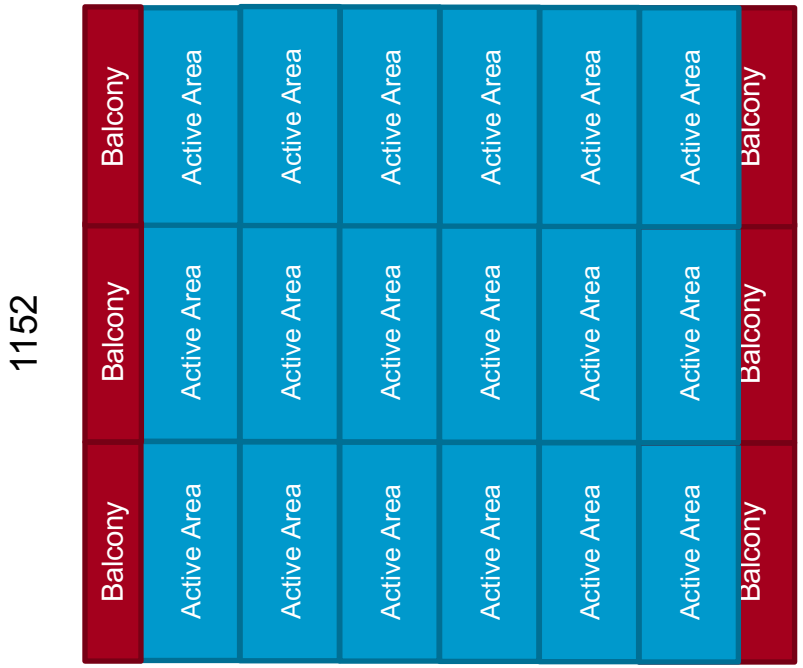
Variant of the ePixHR back-end
- 4 arrays of 192 ADCs
- Each array is a copy of the ePixHR back-end (demonstrated)

Tiling for a 1Mpix camera

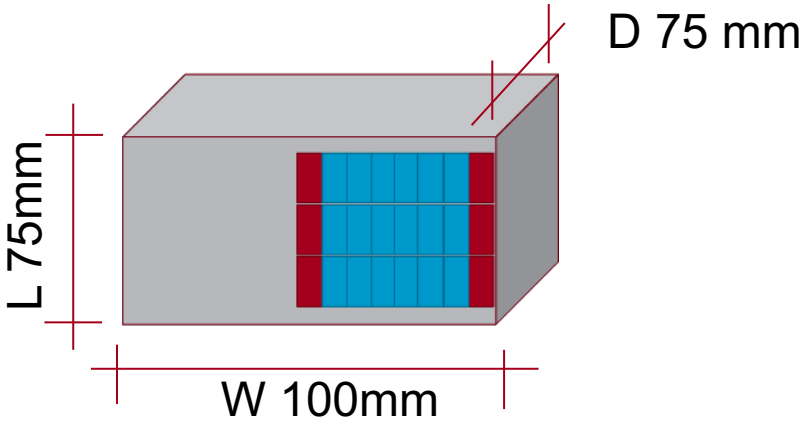
Side view



1152 (active area of ~ 57.2mmx 57.2mm)



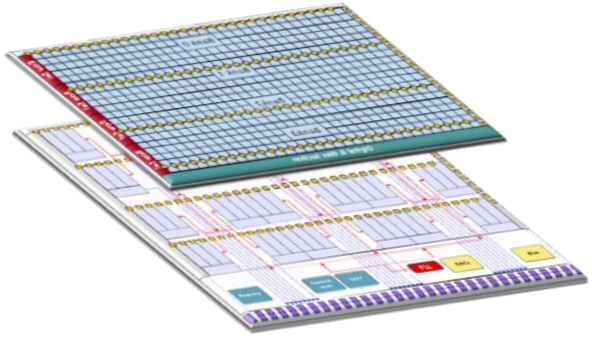
- Shingled assembly to maximize fill factor
- Overall dimensions compatible with requirements

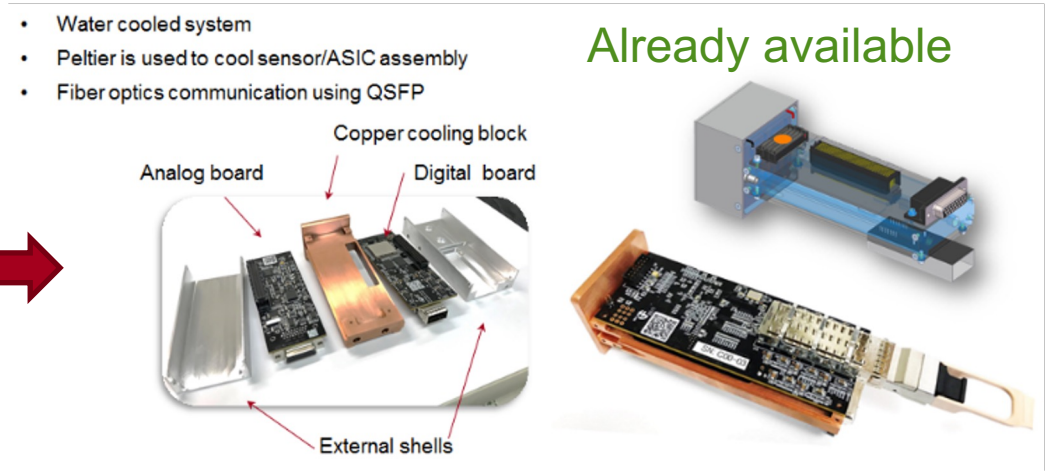


Development plan

Phased approach:

- Core Module Demonstrator assembled and characterized using ePixHR 140kPix Detector Platform + Camera Concept Study



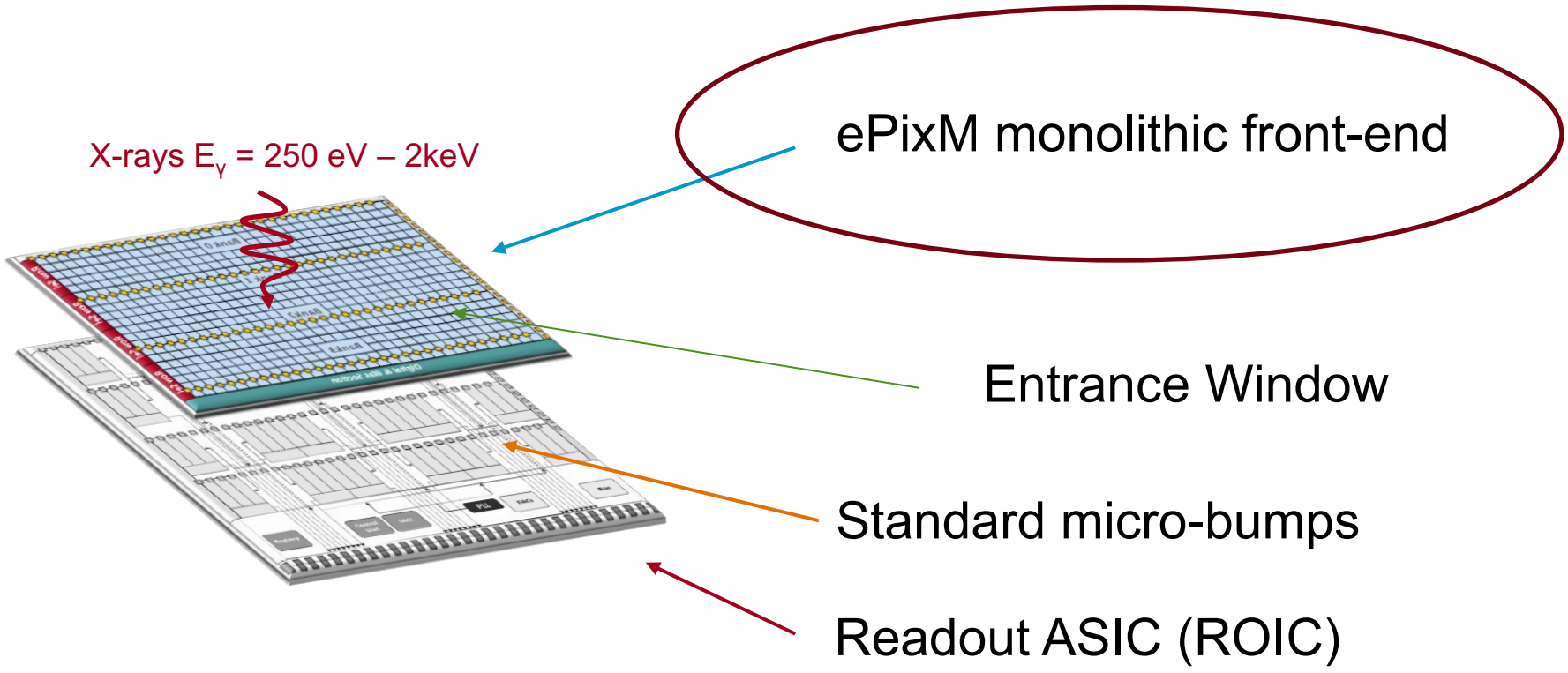


- Down-selection with VFCCD based on Demonstrator results and Camera Concept study – end of 2020

- If selected. 1MPix camera development by end of 2021

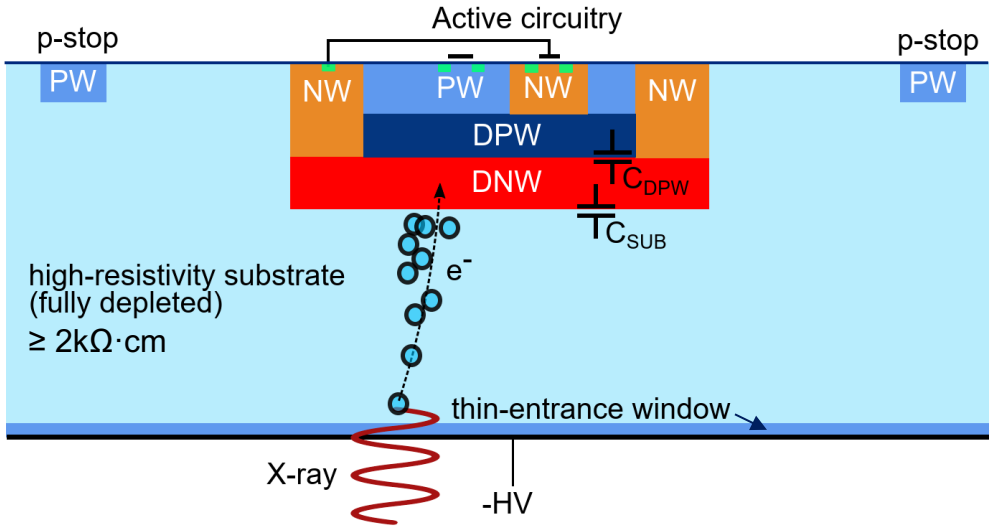
Technical approach and achievements

CMOS Monolithic front-end



- Summary of previous years
- This year achievements

Fully-depleted monolithic pixel sensor architecture



$$C_d = C_{DNW-SUB} + C_{DNW-PSUB}$$

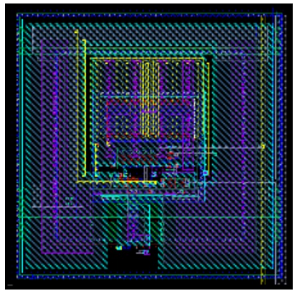
$$\text{ENC} \propto {g_m}/{C_d} \quad \text{(thermal)}$$

Trade-off:
C_D (noise) - Area (complexity)

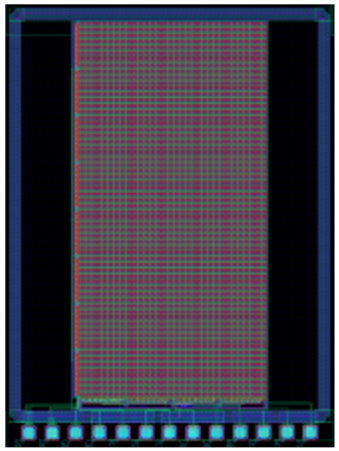
- HV applied on backside: full-depletion, charge collected by drift [1]
- Electronics sits in deep n-well (DNW), which also acts as collection node
- Additional deep p implant (PSUB) isolates NW (PMOS transistors) from DNW
- P-stop around pixels, guard rings at chip periphery
- Wafers thinned and back-processed (final thickness will depend on $V_{breakdown}$)

[1] Hemperek T., LF-MONOPIX a depleted monolithic CMOS pixel sensor in a 150 nm CMOS technology, FEE2018

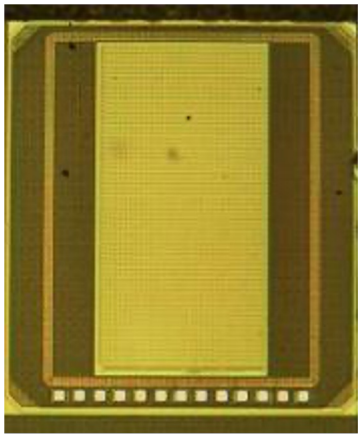
First submission: 64x32 pixel test sensor in L-Foundry Process (see LDAC 2018 for information why L-Foundry process was selected)



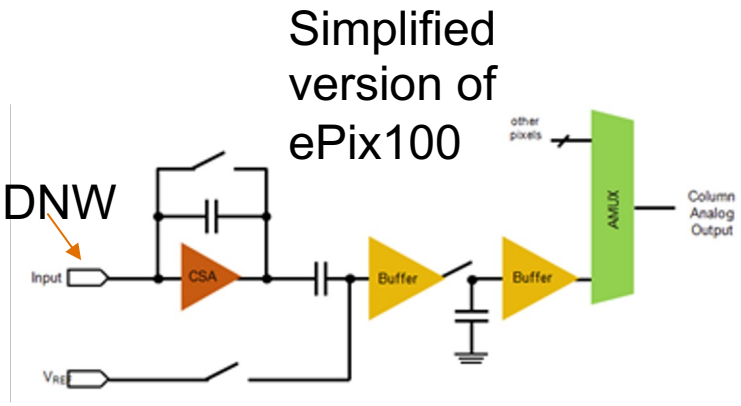
Pixel layout: ePix-like architecture (25um x 25um pixel)



64x32 pixel sensor layout



64x32 pixel sensor picture



- Prototype 64x32

-Purpose: to evaluate technology for X-ray application

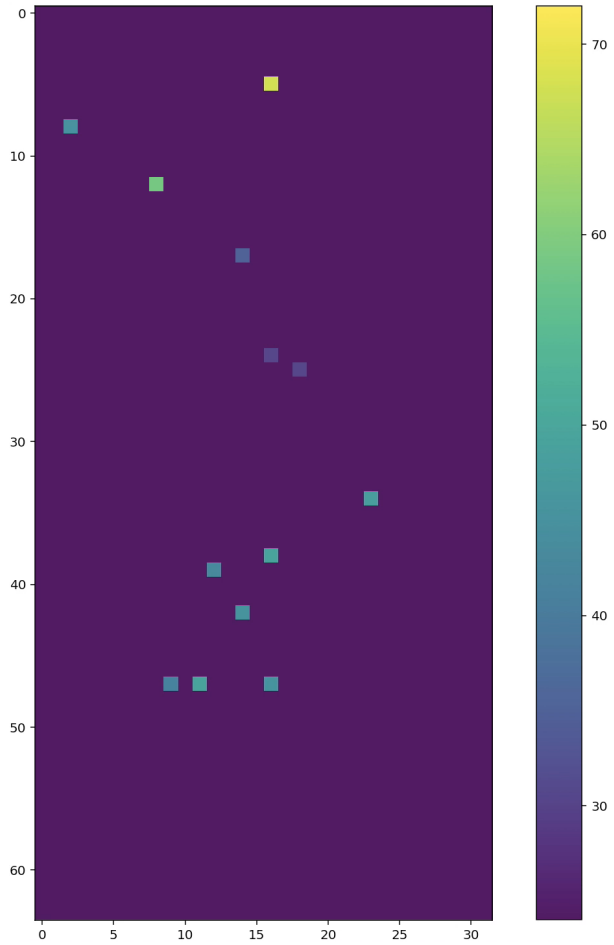
-Pixel size 25x25 um^2

-Integration <10us

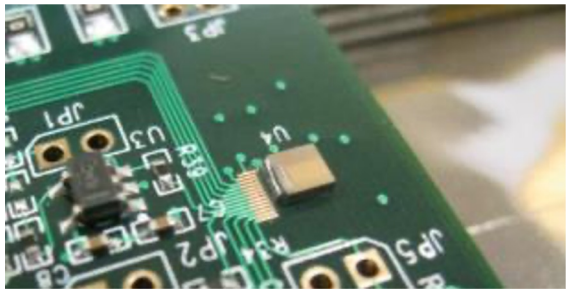
-Energy range: 250 – 2,000 eV

-Full scale: 280keV

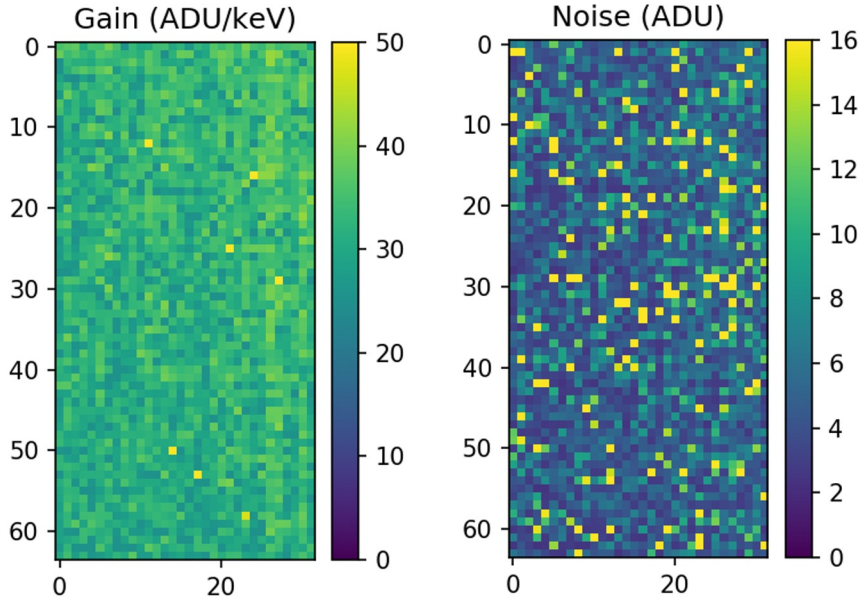
Prototype results - bench test with sources



Fe55 live acquisition



ePixM, Fe55 Source (5.9 keV, 6.4 keV)

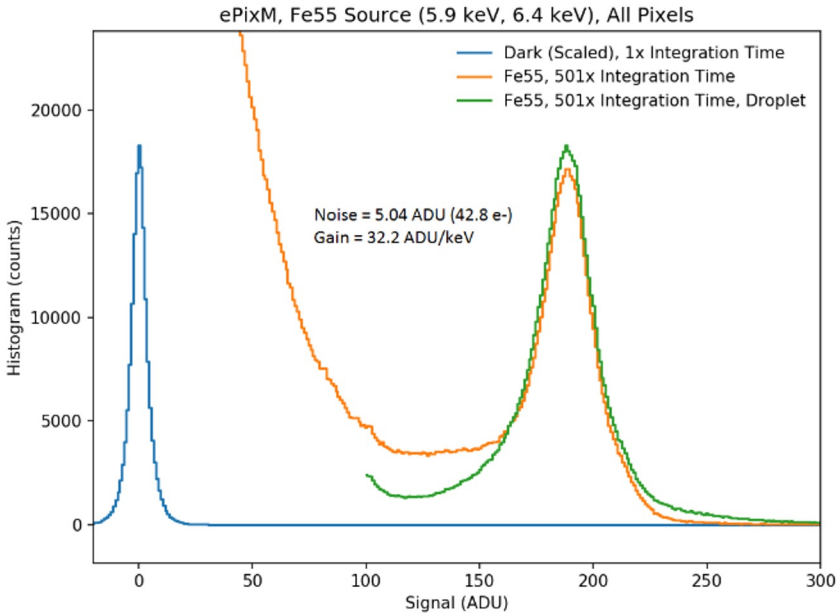


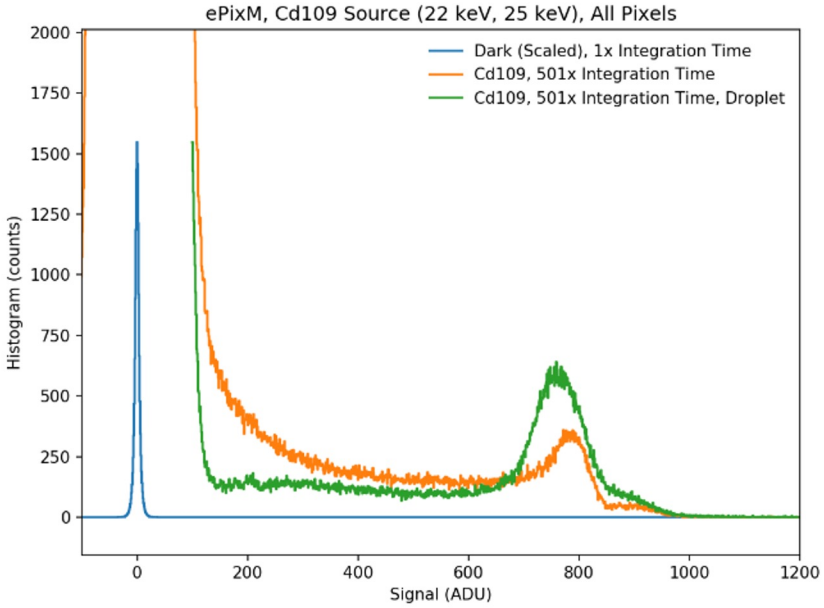
Gain = 32.2 ADU/keV

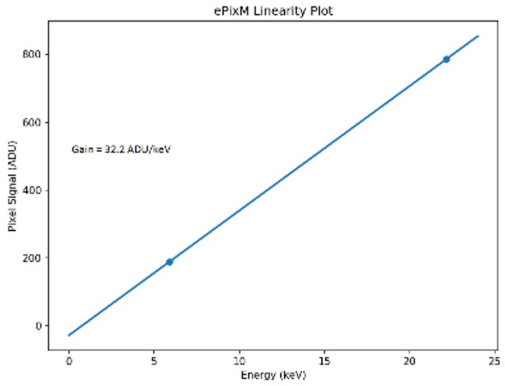
Noise = 42.8e-
(5.04 ADU)

Prototype results - bench test with sources

2.5ms Integration Time





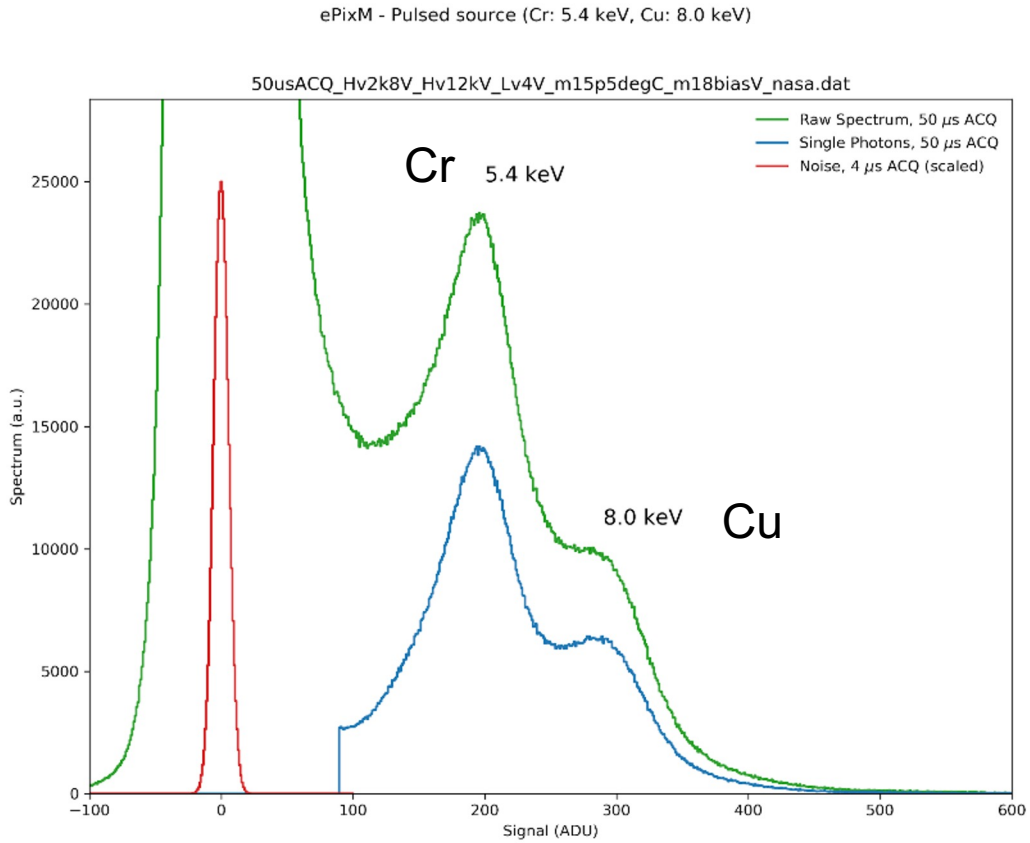


Bias voltage 20V only (instead of 120V).

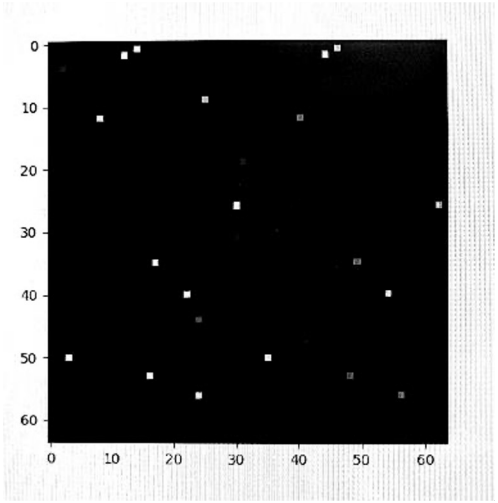
- Guarding modification required.
  - Implemented for next submission
- Not fully depleted-higher capacitance-higher noise
- Charge sharing also limits resolution

Spectra resolution affected by the long integration time 2.5ms vs 5us (expected at LCLS)

Prototype results - pulsed



- Synchronized measurement with 50us integration
- Resolution dominated by charge sharing and partial gain calibration



Noise at LCLS integration time: 42 e^- (spectra at 50 us higher noise 68e^- but n/a for LCLS)

1st prototype take-away

First prototype works with 42 e^- noise.

Reason was discovered, design was fixed for 2nd prototype submission:

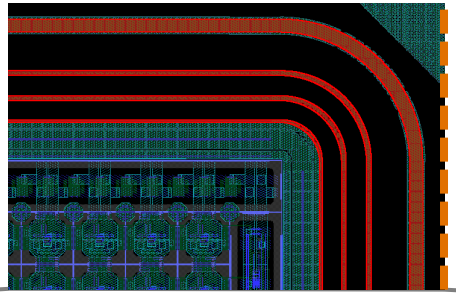
- $V_{breakdown}$= 20V versus the targeted 120V → Improved guard ring & p-stop layout
- Due to low $V_{breakdown}$, the capacitance is much larger which impacts the noise → TCAD simulations with new PDK from foundry.
- Gain stages were optimized compared to the first prototype which will result in better noise performance

2nd Prototype Main design features:

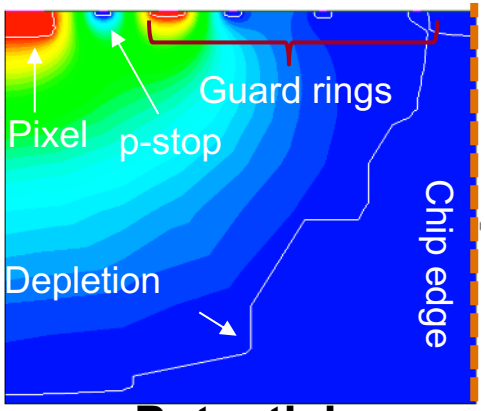
- 150 nm CMOS technology
- High-resistivity substrate
- 7.5 kHz frame-rate (expandable)
- 50 µm pixel size
- 384 x 192 pixels (tileable)
- Single-photon detection @ 250 eV
- Noise < 15 e^-
- Dynamic range > 10^3 photons
- Automatic gain-switching

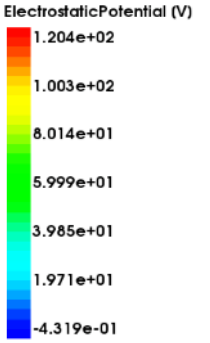
TCAD simulations: p-stop & guard rings

- Guard rings at chip boundaries to limit I_{leak}
- p-stop structures with metal overhangs to isolate each pixel
- Rounded edges at corners to reduce peak E-field

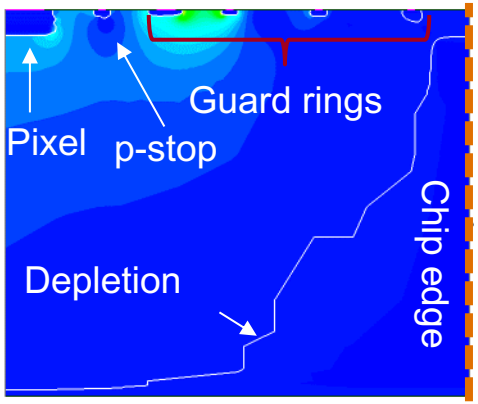


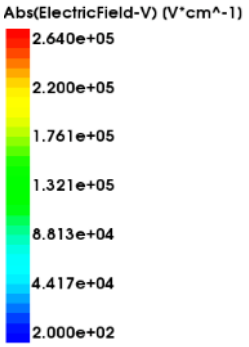
Chip edge





Potential





E-field

TCAD simulations: detector capacitance

Performed device simulations to characterize detector capacitance with:

- New TCAD design kit from foundry
- New pixel layout (2nd prototype)

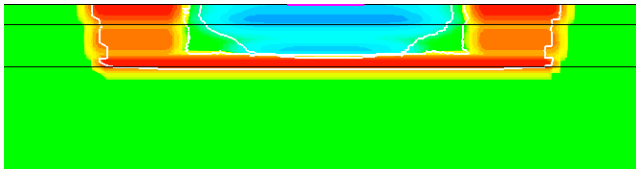
	Capacitance [fF]
total (center pix)	56
adjacent pixel (x 4)	0.16
corner pixel (x 4)	0.0038
internal p-well	45
p-guard ring	8.6
backside	2.2
Total (summed)	**56.4552**

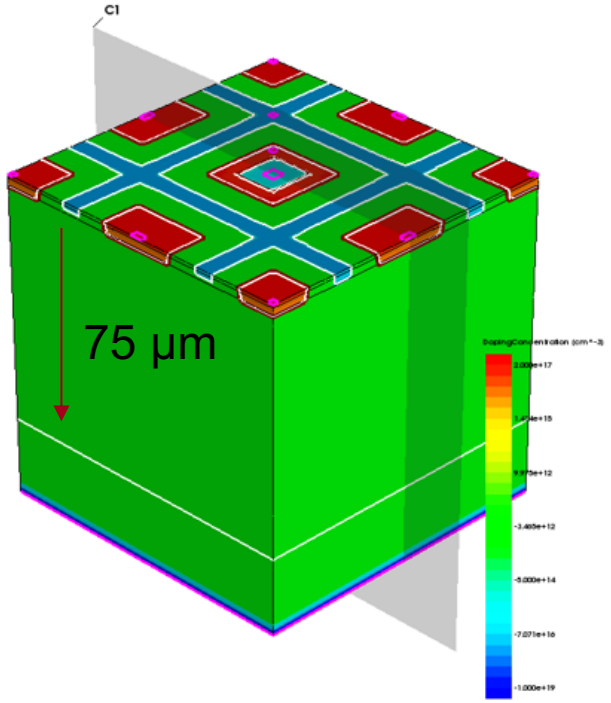
To validate results of simulations:

- Calculated capacitance of 1st prototype, repeated analog simulations

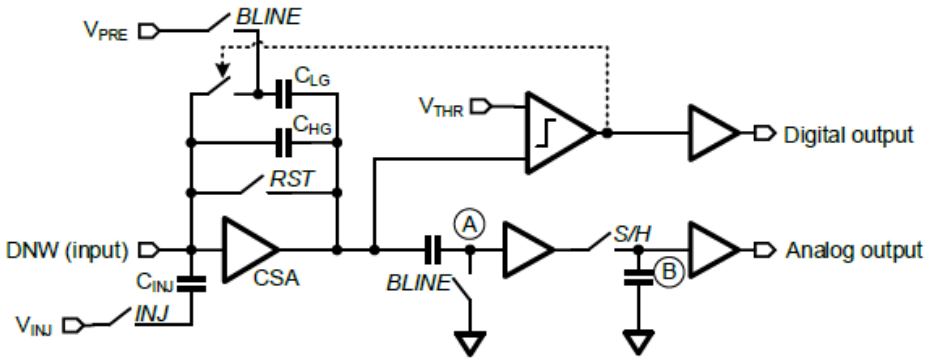
  → noise simulations matches measurements

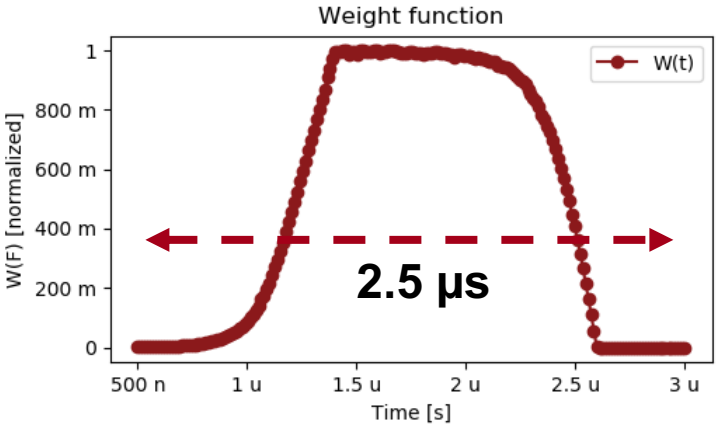
Pixel doping profile:





ePixM: pixel electronics



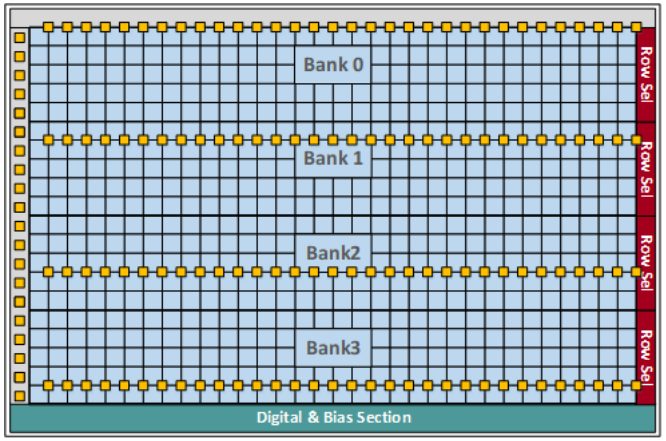


- Charge Sensitive Amplifier (CSA) with auto-ranging capability
- Injection capacitance for calibration
- Correlated Double Sampling (CDS) → quasi-trapezoidal shaping
- Pre-charge feedback cap to extend DR and reduce noise when switching gain
- Sampling stage and 2x column buffers for analog and comparator (gain) output

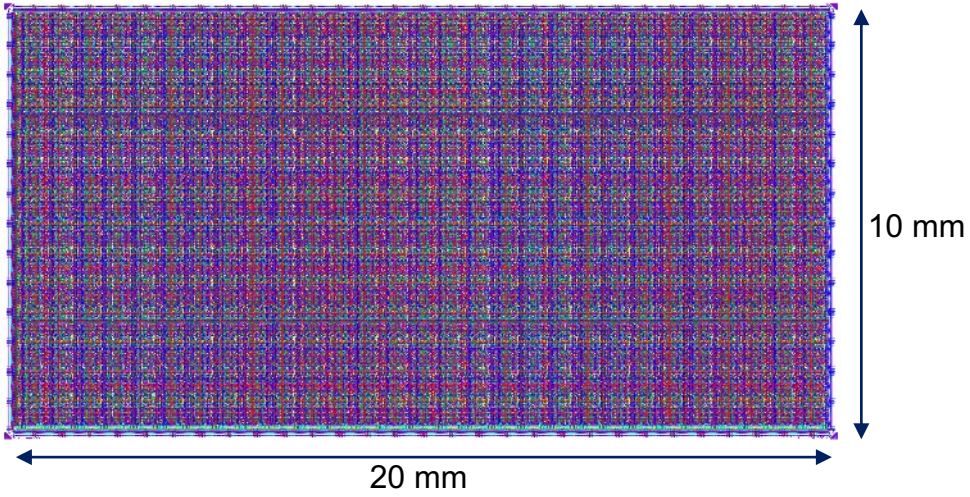
Rota L. *et al.*, Design of ePixM, a fully-depleted monolithic CMOS active pixel sensor for soft X-ray experiments at LCLS II, 21st International Workshop on Radiation Imaging Detectors, July 7-12 2019, Kolympari, Chania, Crete, Greece

Matrix: architecture and floorplan

Simplified Block Diagram



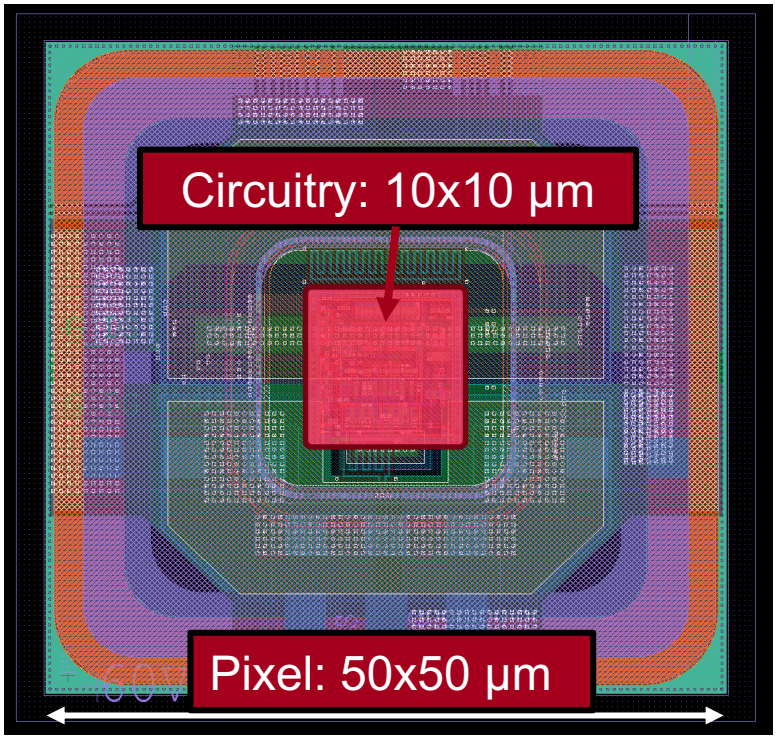
Layout

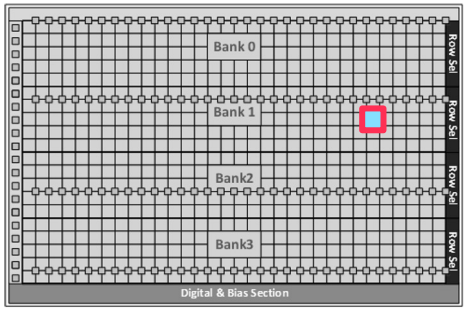


- 4 banks of 48x384 pixels for parallel readout
  - Matrix column split in 4 sections
  - x2 50um pixels columns of each section multiplexed to one 100um backend channel
- 2 micro-bumps every 2 subcolumns
- Bias and digital section at the bottom
- Sensitive area ~ 20 mm x 10 mm

Post-layout simulations: noise

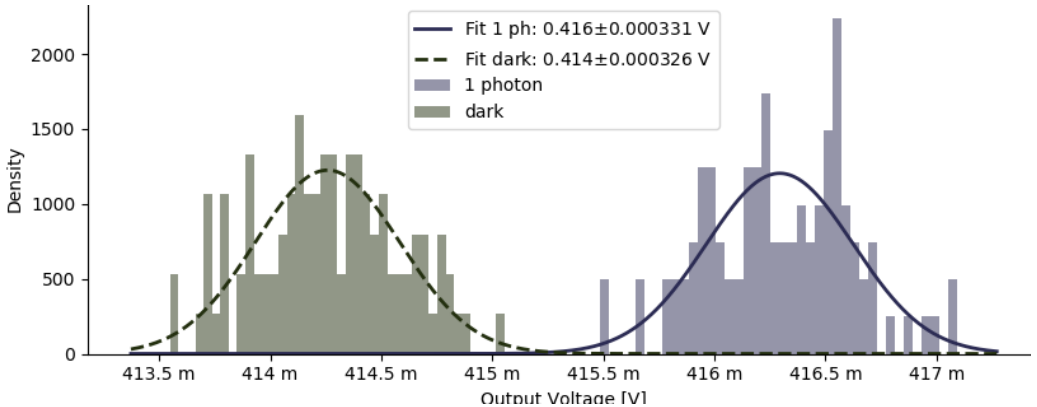
Layout of one pixel





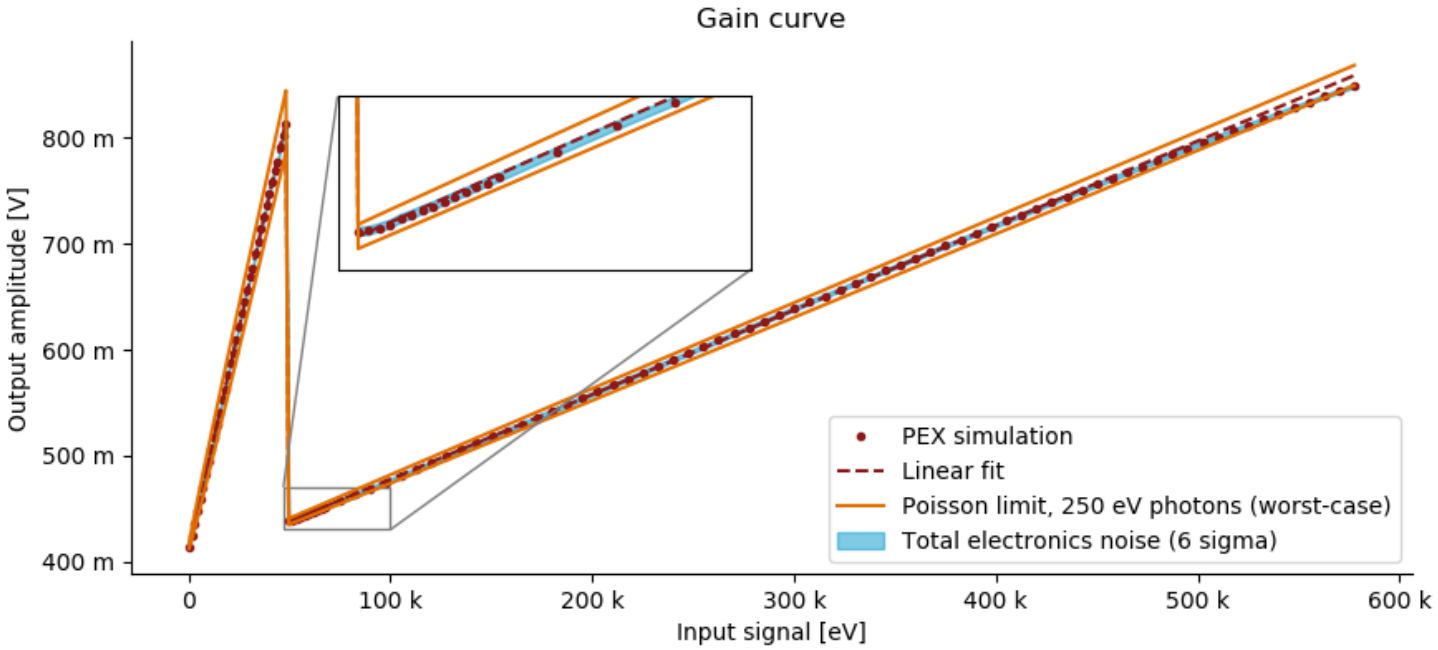
Equivalent Noise Charge (ENC) simulated at room temp, assuming C_{Det} = 70 fF:

- High-Gain = **11.3 e^-**
- Low-Gain = 90 e^-



Post-layout simulations: automatic gain-ranging

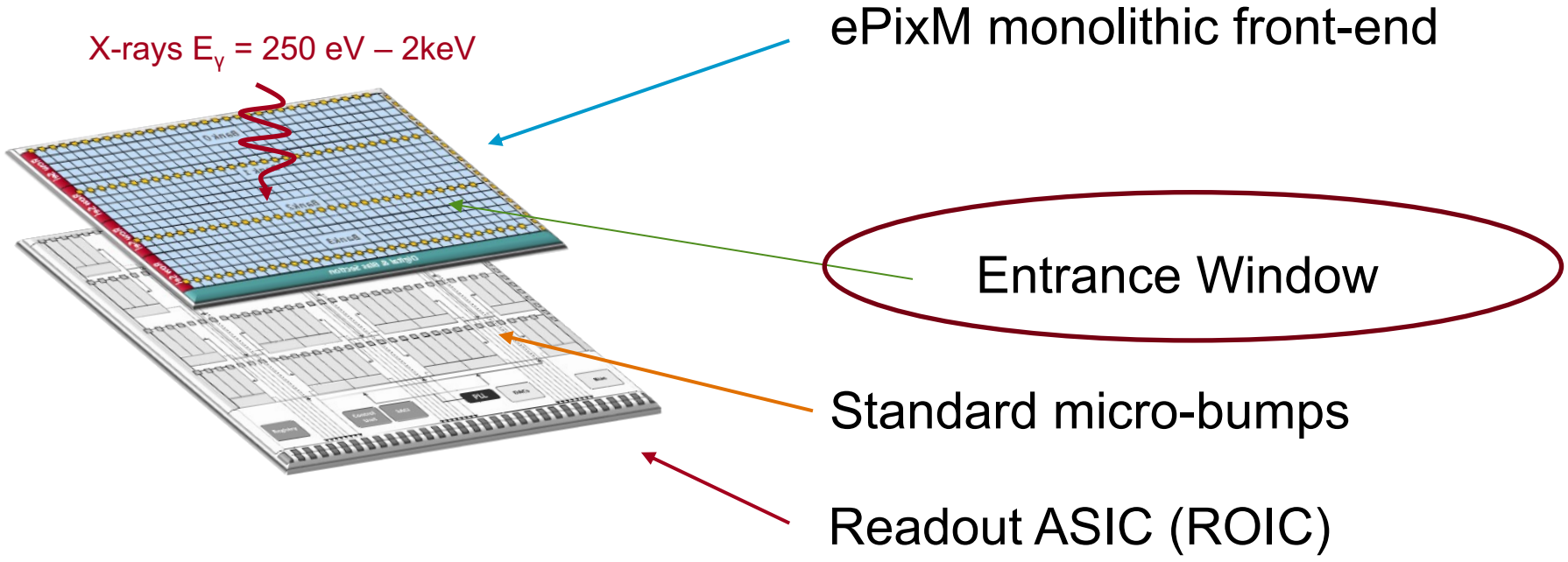
Noise and non-linearity well below Poisson limit over whole range 250 eV – 500 keV



Gain [mV/fC]	Range [keV]	ENC [e-]	Statistical limit [e-]
187	0 - 50	11.3	69.4
17	50 -500	90.8	989.9

Technical approach and achievements

CMOS Monolithic front-end back-side window



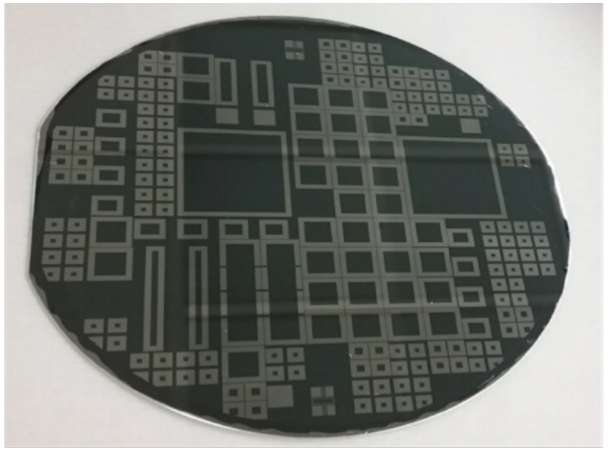
- Summary of previous years
- This year achievements
- Residual risk analysis

Soft X-Ray entrance window (demonstrated in 2018)

- Thin insensitive region near surface is critical to achieving required QE
- LFoundry wafers have been processed at SLAC to add entrance window
  - Thinned chips to 50 microns to facilitate full depletion and backside illumination
  - Implanted and annealed
- Update since last LDAC:
  - SLAC acquired low temperature micro-wave annealing machine
    - In process of installation/commissioning at SLAC
  - Allows fast turn-around in-house entrance window processing

Thin entrance window for soft X-rays

- Wafers post-processed by SLAC to form thin entrance windows on the backside
- MicroWave Annealing (MWA) process is robust, inexpensive and fast
- Sensors with thin entrance window bonded to ePix250s and ePix10k-Tender prototypes
- No degradation observed in Si sensor due to window process

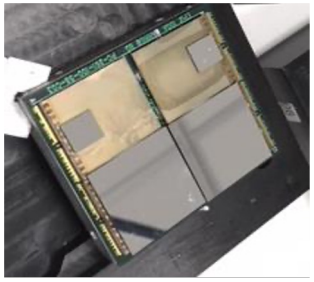


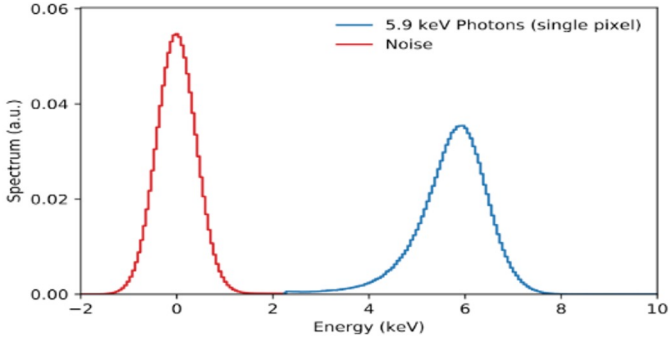
Backside of a SLAC-made sensor wafer for ePix detectors (courtesy of J. Segal, J.Hasi, L. Rosario & C. Kenney)

Results published in:

Segal J. *et al.*, Thin-Entrance Window Sensors for Soft X-rays at LCLS-II, NSS-MIC 2018

Si sensors with thin entrance window & ePix250s

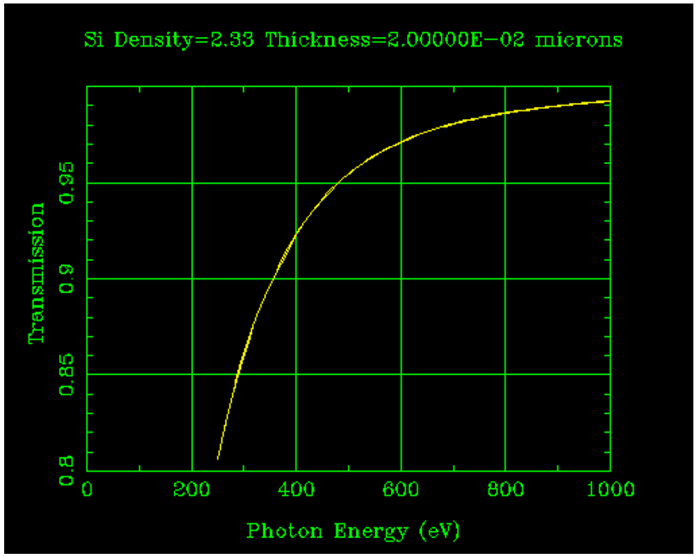


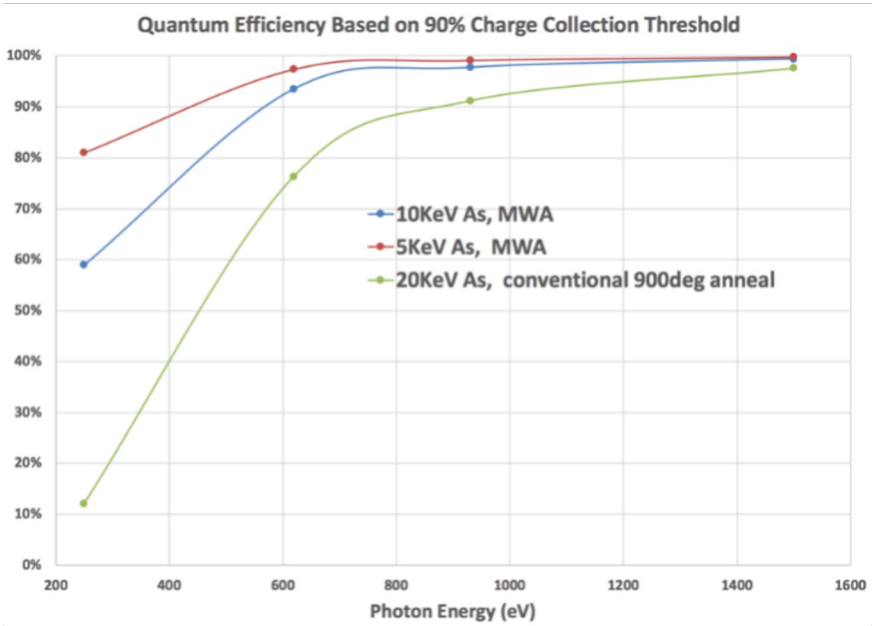


- Sensor leakage contributed 6 electrons of noise when cooled to -20C
- No damage to sensor window observed

High quantum efficiency at carbon edge >84%

- 20 nm is 84% transmission at 279 eV
- Sensors usually need a thin aluminum film deposited to block visible light or debris shield to protect detector from sample material
- Both of the above can be the dominant attenuating component

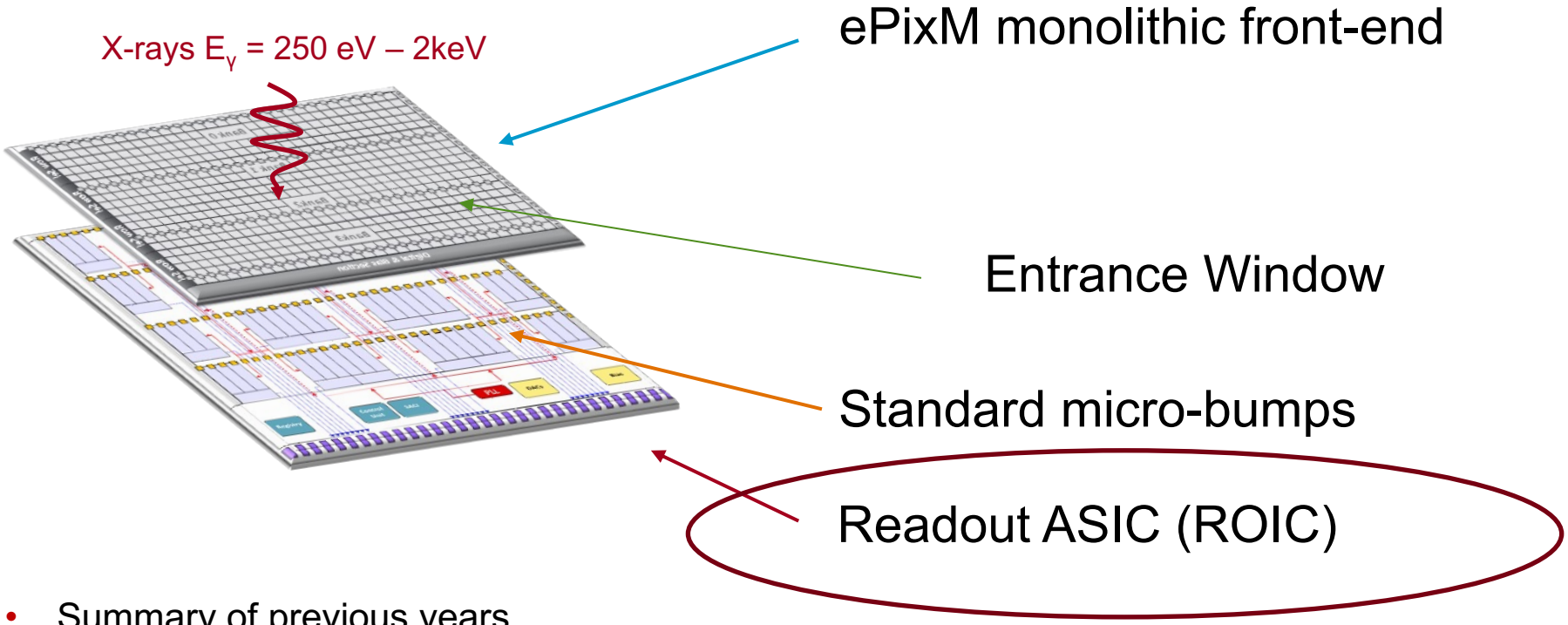




Synopsys simulations (J. Segal)

Technical approach and achievements

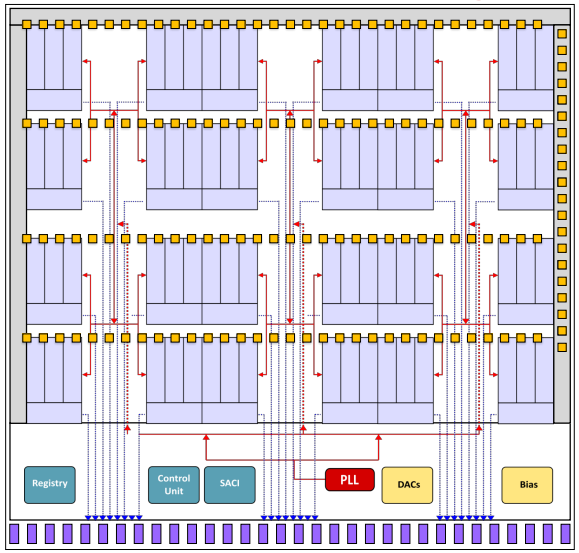
ePixHR based back-end ASIC



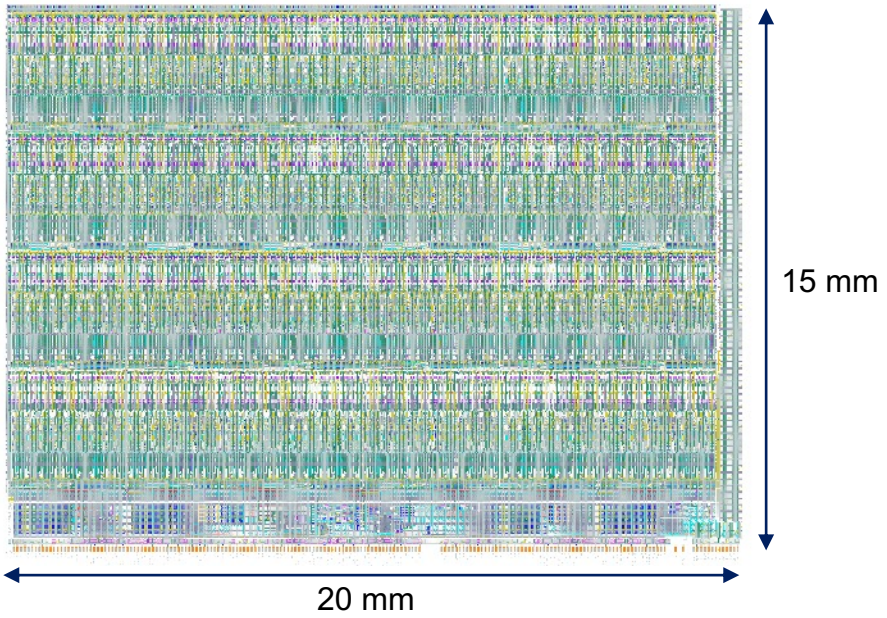
- Summary of previous years
- This year achievements

7.5 kHz frame-rate High-Rate backend ASIC for ePixM

Simplified Block Diagram

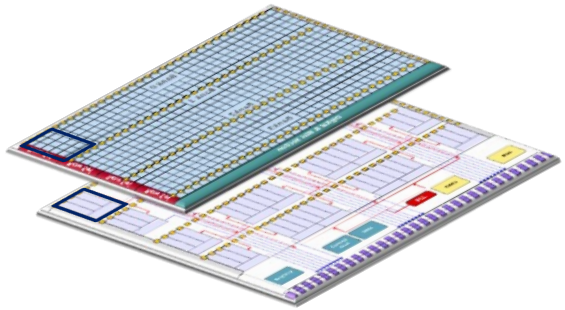


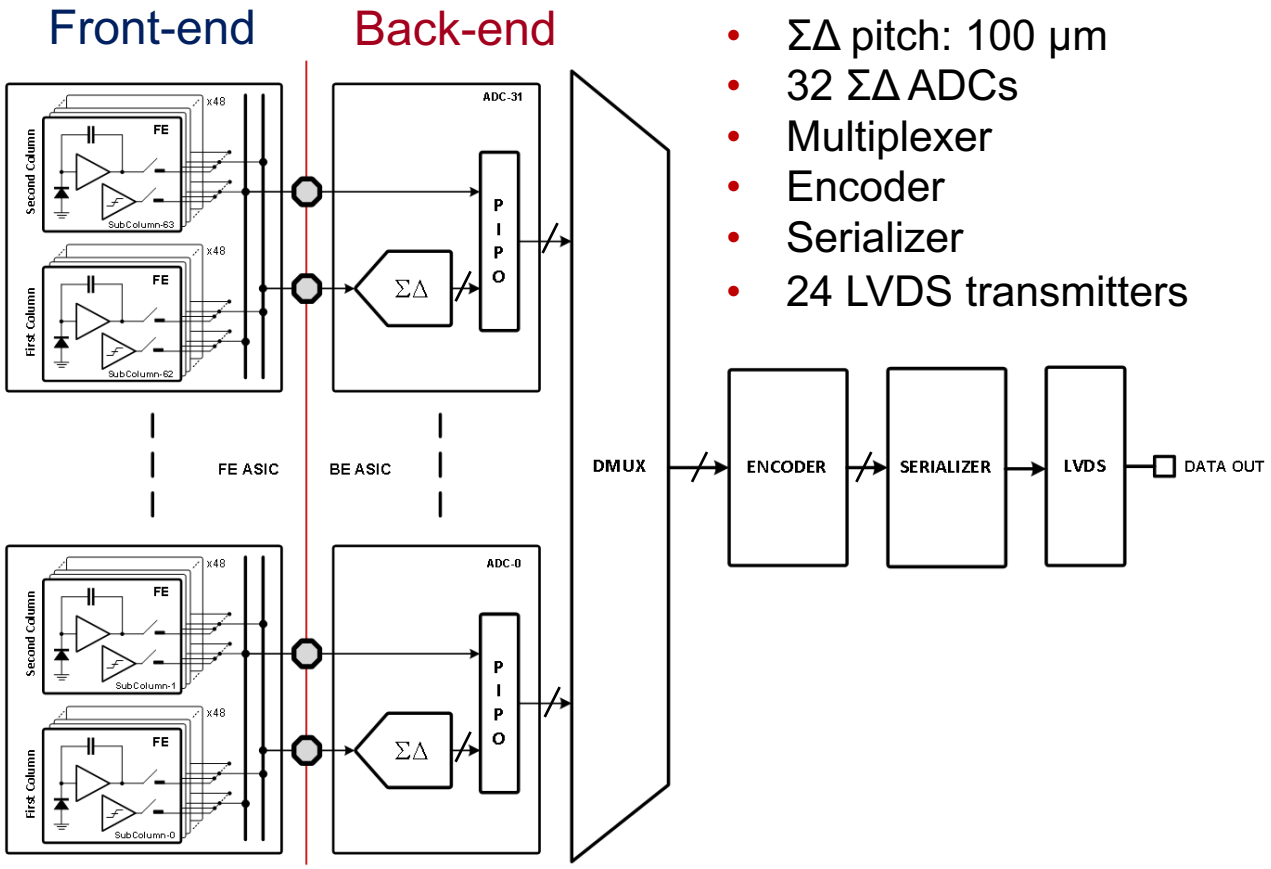
Layout



- 4 banks of 192 1-MHz, 14-bit ΣΔ Analog to Digital Converters (ADC)
  - Same ADC channel circuit/layout used for ePixHR (see ePixHR talk)
  - Already demonstrated in 2018
- 2 micro-bumps every ΣΔ ADC serving two column of 96 pixels (not multiple connections per pixel)
  - Simpler bump-bonding assembly than standard ePixs
- Other blocks: PLL, Control Unit, Registers, SPI interface, BGR, Bias, DACs, Pulser, etc.

ePixM interface between CMOS sensor and ROIC



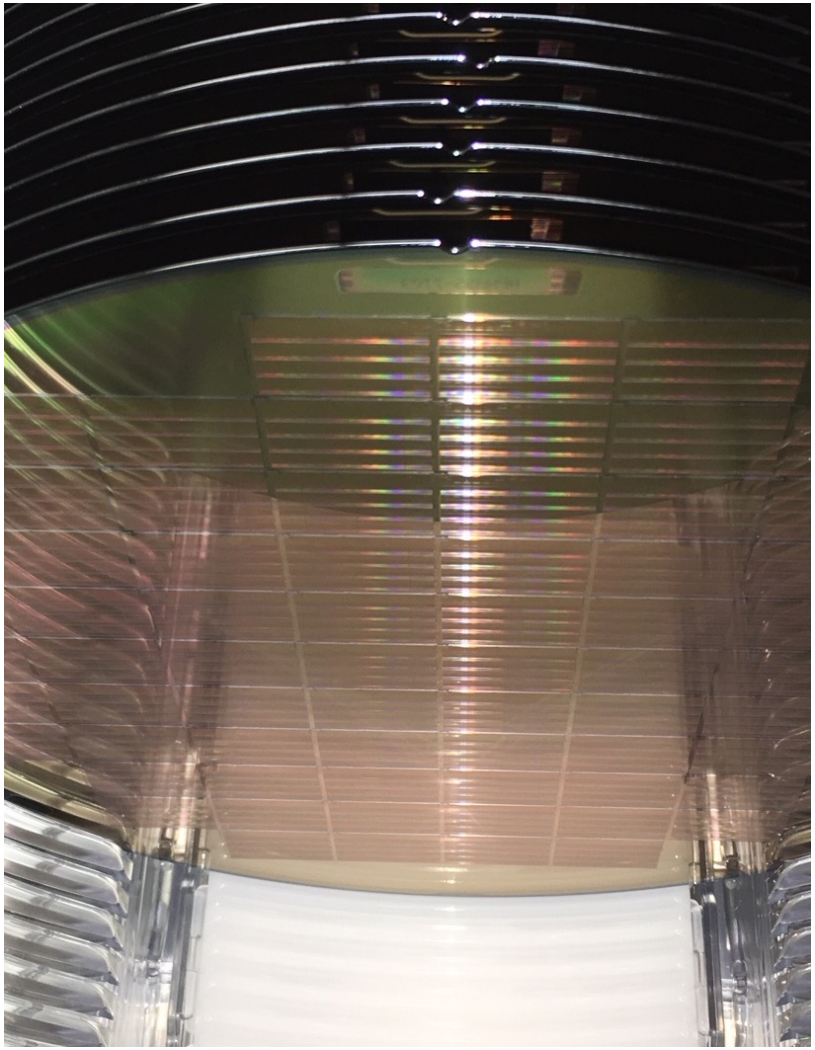


- ΣΔ pitch: 100 µm
- 32 ΣΔ ADCs
- Multiplexer
- Encoder
- Serializer
- 24 LVDS transmitters

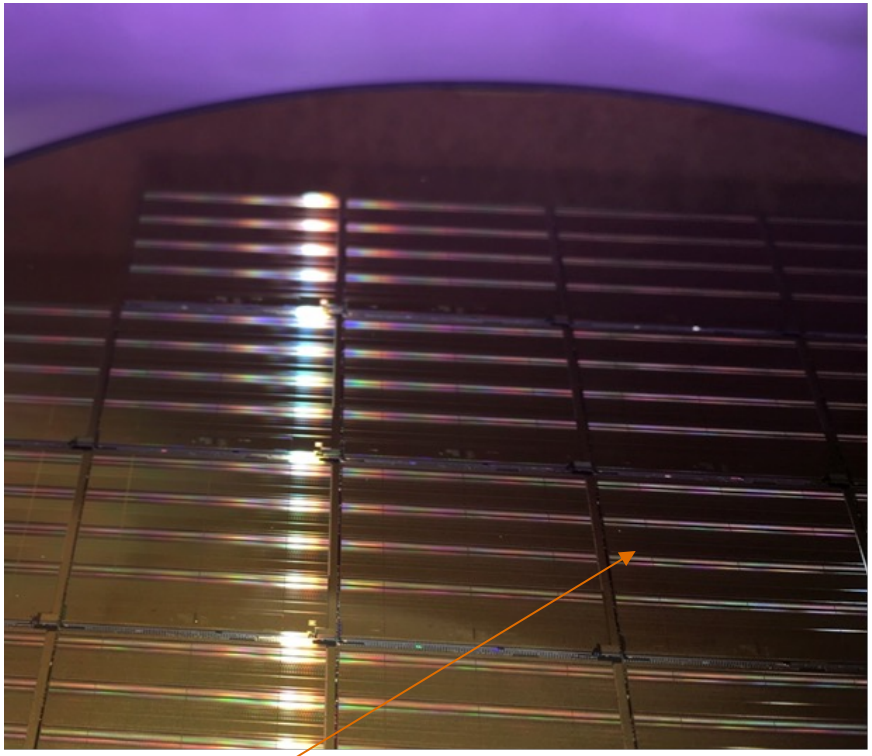
- Pixel pitch: 50 µm
- Subgroup of 48 x 2 pixels

Uses the same blocks proven in ePixHR

ePixM Backend



Chip arrived last week.



4 orders of ADCs - 768

Status (progress since last LDAC) vs timeline

CMOS sensor:

- 2nd CMOS Prototype was designed, laid out and verified
  - Results from post-layout simulations meet design specs in terms of noise, dynamic range and functionality
- Submitted to L-Foundry for fabrication first week of March 2019
- 8 months delay to fabrication start at L-Foundry due to scheduled modernization of fabrication line at factory with subsequent recalibration and process validation of their production line
- Actual start of ePixM fabrication: October 2019
- Expected deliver from fabrication: End of January 2020

ROIC:

- 1st ROIC Prototype was designed, laid out, verified and fabricated ASIC received in November 2019
- Assembled to carrier board

Despite delays project is on track for the down selection date

ePixM prototype camera: Next steps

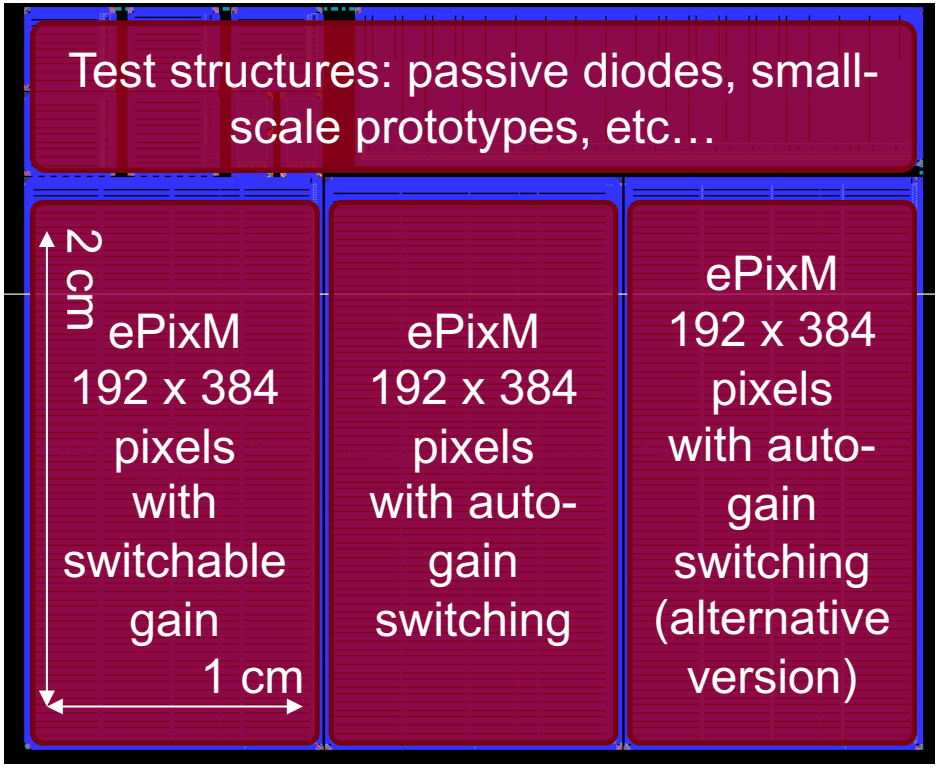
- Test ePixM back-end
  - modify/resubmit, if needed
- Test L-Foundry full-size CMOS sensor (February 2020)
  - modify/resubmit updated L-Foundry sensor, if needed
- Bump-bond to HR Backend
- Assemble in prototype camera (ePixHR)
- Camera characterization at LCLS
- Down-select end of CY2020

Risk Assessment

Risk	Likelihood/Impact	Mitigation	Risk status
Unexpected complexity in the design	**Low/Medium** Schedule delay and increased cost.	**Accept without mitigation**	**Retired**
First Iteration full size CMOS sensor has bugs	**Medium/Medium** Would need to another fabrication effort which is planned in the budget.	**Multiple variants Second iteration in the budget.**	Active
First Iteration Back-end Design has bugs	**Medium/Medium** Would need to another fabrication effort which is planned in the budget.	**Second iteration in the budget.**	Active
Second Iterations have bugs	**Low/High** Schedule delay and increased cost.	**Accept without mitigation**	Active
Carrier board has defects	**Low/Low** *Negligible delay and cost increase.*	**Accept without mitigation**	**Retired**
Sensor post processing (Entrance Window)	**Medium/Medium** Schedule delay and increased cost.	**Accept without mitigation**	**Retired**
Parts reused from other projects (ePixHR)	**Medium/Medium** Schedule delay and increased cost.	**Accept without mitigation**	**Retired**

CMOS sensor design risks mitigation

- Early prototype: demonstrated that technology is suitable for X-ray applications
- 3 variants designed:
  - Conservative fixed gains version
  - 2 auto range variants
- Set of test structures for debugging



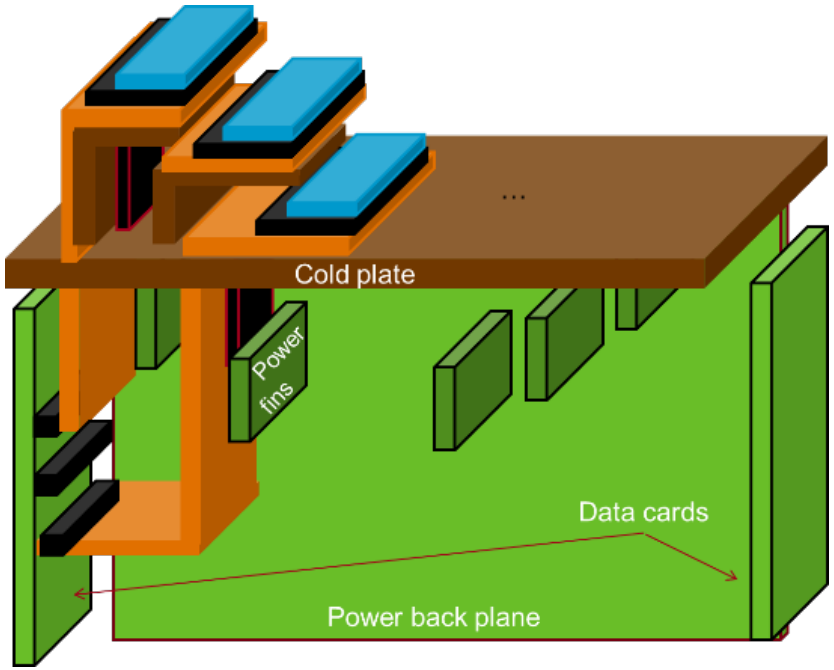
Towards a science camera

Concept study started this year based on:

- Same sensor/ASIC assemblies as for prototype camera
- New shingled mechanical/thermal structure
- Prototype camera digital electronics board circuits laid out on new printed circuit board for shingled structure
- Same interface in terms of power/control/DAQ as for prototype camera (just more fibers)
  - Completely scalable

ePixM Detector system baseline concept

- **Front end electronics:**
  - Tightly connected to ASIC geometry/shingle geometry
  - Power to ASICs/sensor
  - Control signal to ASICs
  - Data access to ASIC
  - Cooling system
- **Camera DAQ:**
  - IO to FPGA
  - Control logic
  - Data storage (full frames)
  - Data compression
  - Data transmission
- **Back end DAQ:**
  - User interface
  - Data reception
  - Data storage



Aspects to be studied:

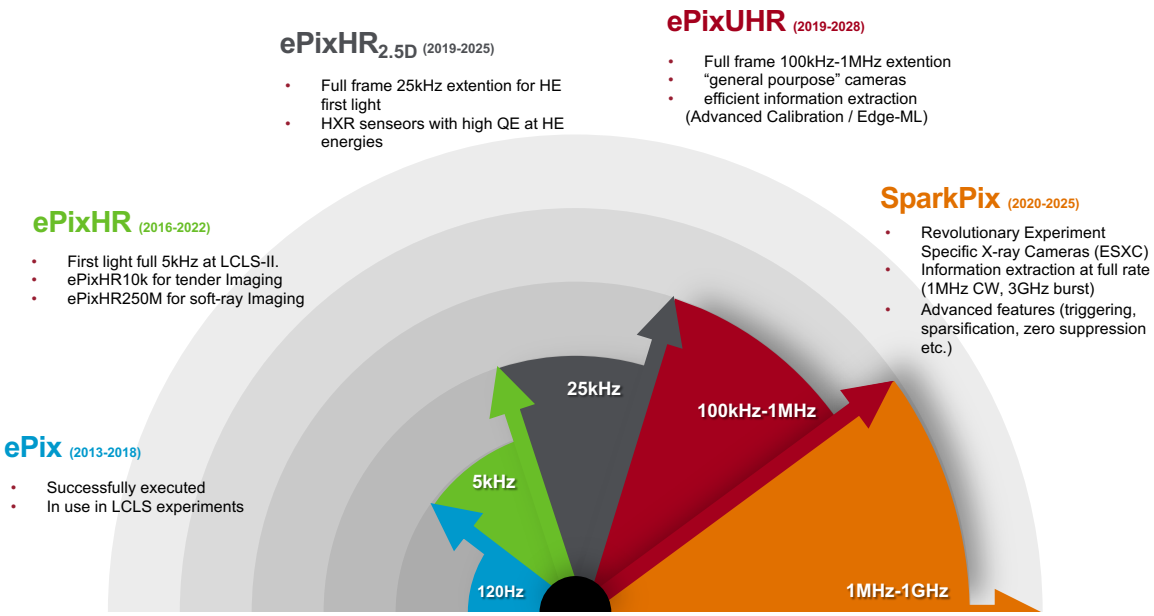
- *Mechanics*
- *Thermal dissipation*

All components of Camera are vacuum compatible

ePixM follows the same upgrade path of the ePix family

ePixM (ePixHR250M) is natively a variant of the ePixHR

- see strategy slides for general approach
  - UHR path for ePixM: ~ 50 kHz frame-rate
  - Dedicated SparkPix variants for soft-X-ray are under study

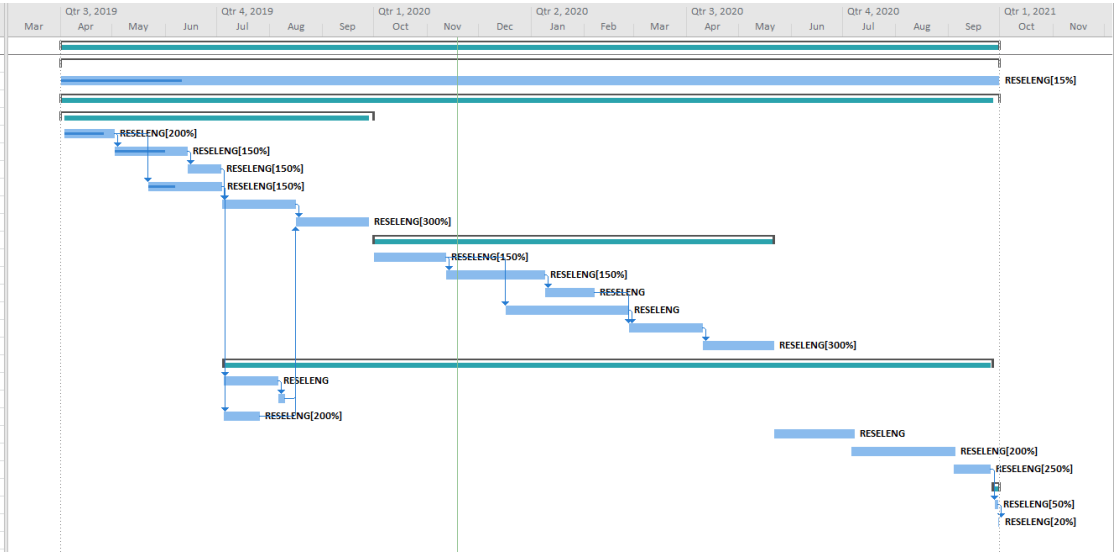


Bigger, Faster, Higher resolution and Higher Energies

Management Plan

- SLAC Detector R&D projects follow LCLS project management guidelines
  - CDR conducted before project starts
  - Financial plan approved by the PEC before start
  - Documented using Microsoft Project
  - Bi-weekly meetings to follow status are conducted together with the project sponsor (LCLS)
  - Milestones are tracked and if requires re-baselines or the project are implemented

	Task Name	Resource Names	*not* SLAC Shops	Duration	Start	Finish
1	**ePixM Phase 3**		**No**	**569 days**	**Mon 4/1/19**	**Wed 9/30/20**
2	**Project Management**		**No**	**569 days**	**Mon 4/1/19**	**Wed 9/30/20**
3	Management+monthly sched.+cost rep.	RESELENG[15%]	No	372 days	Mon 4/1/19	Wed 9/30/20
4	**Project Execution**		**No**	**569 days**	**Mon 4/1/19**	**Wed 9/30/20**
5	**ePixM 4x Back-end R&D Iteration 1**		**No**	**189.5 days**	**Mon 4/1/19**	**Mon 9/30/19**
6	Task 1 - Backend Design	RESELENG[200%]	No	30 days	Wed 4/3/19	Wed 5/1/19
7	Task 2 - Back-end layout	RESELENG[150%]	No	30 days	Thu 5/2/19	Thu 6/13/19
8	Task 3 - Backend Post Layout Simulation	RESELENG[150%]	No	20 days	Thu 6/13/19	Wed 7/3/19
9	Task 4 - Full chip simulation and verification	RESELENG[150%]	No	30 days	Wed 5/22/19	Wed 7/3/19
10	Task 5 - ePixM back-end ASIC Fabrication		No	45 days	Wed 7/3/19	Fri 8/16/19
11	Task 6 - ePixM back-end ASIC Characterization	RESELENG[300%]	No	30 days	Fri 8/16/19	Fri 9/27/19
12	**ePixM 4x Back-end R&D Iteration 2**		**No**	**242.75 days**	**Tue 10/1/19**	**Thu 5/21/20**
13	Task 1 - Back-end Design	RESELENG[150%]	No	30 days	Tue 10/1/19	Mon 11/11/19
14	Task 2 - Back-end layout	RESELENG[150%]	No	30 days	Tue 11/12/19	Wed 1/8/20
15	Task 3 - Backend Post Layout Simulation	RESELENG	No	30 days	Wed 1/8/20	Thu 2/6/20
16	Task 4 - Full chip simulation and verification	RESELENG	No	40 days	Tue 12/17/19	Wed 2/26/20
17	Task 5 - ePixM back-end ASIC Fabrication		No	45 days	Wed 2/26/20	Fri 4/10/20
18	Task 6 - ePixM back-end ASIC Characterization	RESELENG[300%]	No	30 days	Fri 4/10/20	Thu 5/21/20
19	**System Integration, test and calibration**		**No**	**466.13 days**	**Fri 7/5/19**	**Sat 9/26/20**
20	Task 1 - Carrier board design	RESELENG	No	22 days	Fri 7/5/19	Mon 8/5/19
21	Task 2 - Carrier board fabrication		No	5 days	Mon 8/5/19	Fri 8/9/19
22	Task 3 - Firmware	RESELENG[200%]	No	15 days	Fri 7/5/19	Thu 7/25/19
23	Task 4 - Sensor Processing and Bonding in House	RESELENG	No	31 days	Fri 5/22/20	Tue 7/7/20
24	Task 5 - Camera Characterization	RESELENG[200%]	No	45 days	Mon 7/6/20	Fri 9/4/20
25	Task 6 - Bench X-ray testing	RESELENG[250%]	No	22 days	Fri 9/4/20	Fri 9/25/20
26	**Review Preparation**		**No**	**4.75 days**	**Sun 9/27/20**	**Wed 9/30/20**
27	Compose project final report	RESELENG[50%]	No	2 days	Mon 9/28/20	Tue 9/29/20
28	Final Review	RESELENG[20%]	No	1 day	Wed 9/30/20	Wed 9/30/20



Take away

- ***Are the science requirements and detector performance parameters fully described and self-consistent?***
  - ePixM is designed to meet the requirements for REXS experiments at LCLS-II
    - Performance parameters aligned to meet requirements: Noise, Dynamic Range, Frame rate, QE, Consumption (green demonstrated).

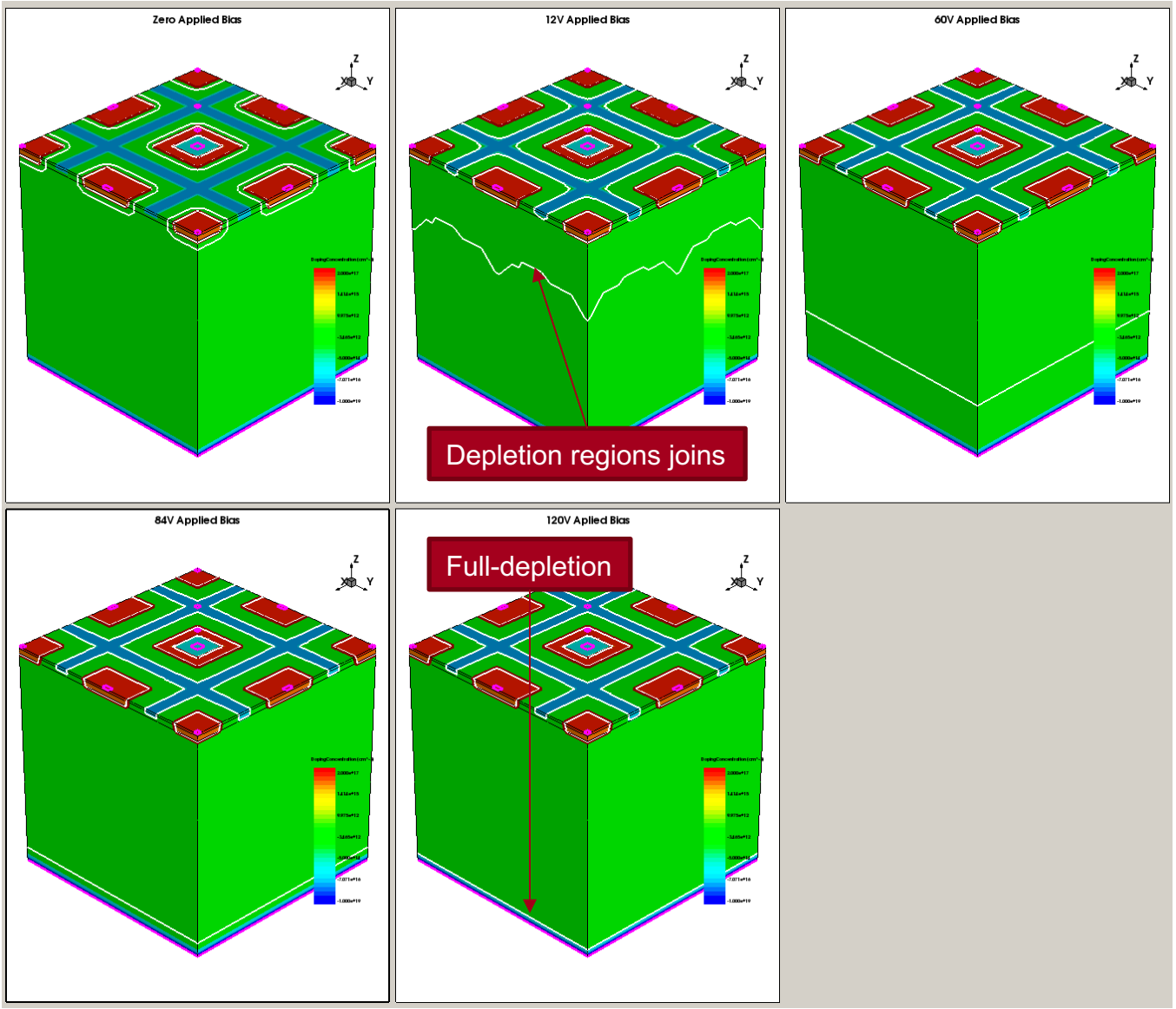
- ***Is the development plan sound, with regard to mitigating technical risk and timely delivery? Are the presented results on track with the development plan? Are the management plans appropriate?***
  - Development is on track (several risks retired. Mitigation in place)
    - Sensor:
      - Prototype (small) sensor tested
      - Full-size CMOS image sensor designed, in fabrication
    - High-Rate Backend ASIC:
      - Designed/fabricated, in testing
    - Digital Electronics boards/mechanical prototype camera mechanical/thermal parts:
      - Designed/fabricate/tested. Ready for sensor/ASIC assembly.
  - Project managed according to LCLS management protocol

- ***Is the choice of this type of detector consistent with the decade-level long-range development strategy, or is there a good reason why a different path has been chosen?***
  - ePixM is natively part of the ePix family and follows the long term upgrade plan

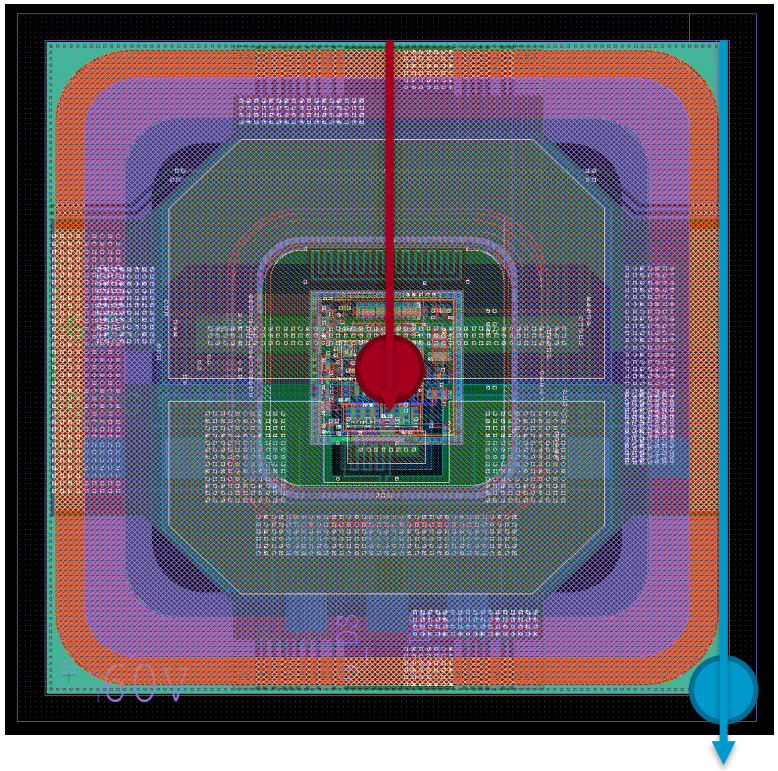
Backup

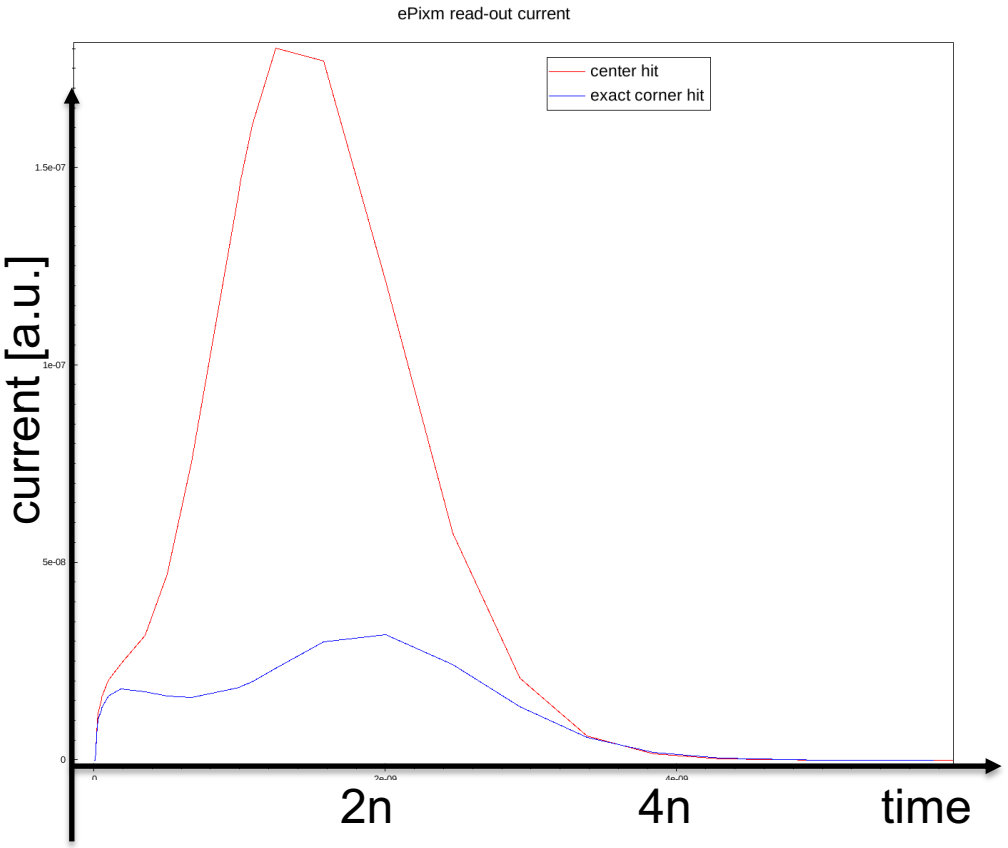
Depletion depth vs V_{bias}

Substrate params:
3K ohm-cm substrate,
100um thick



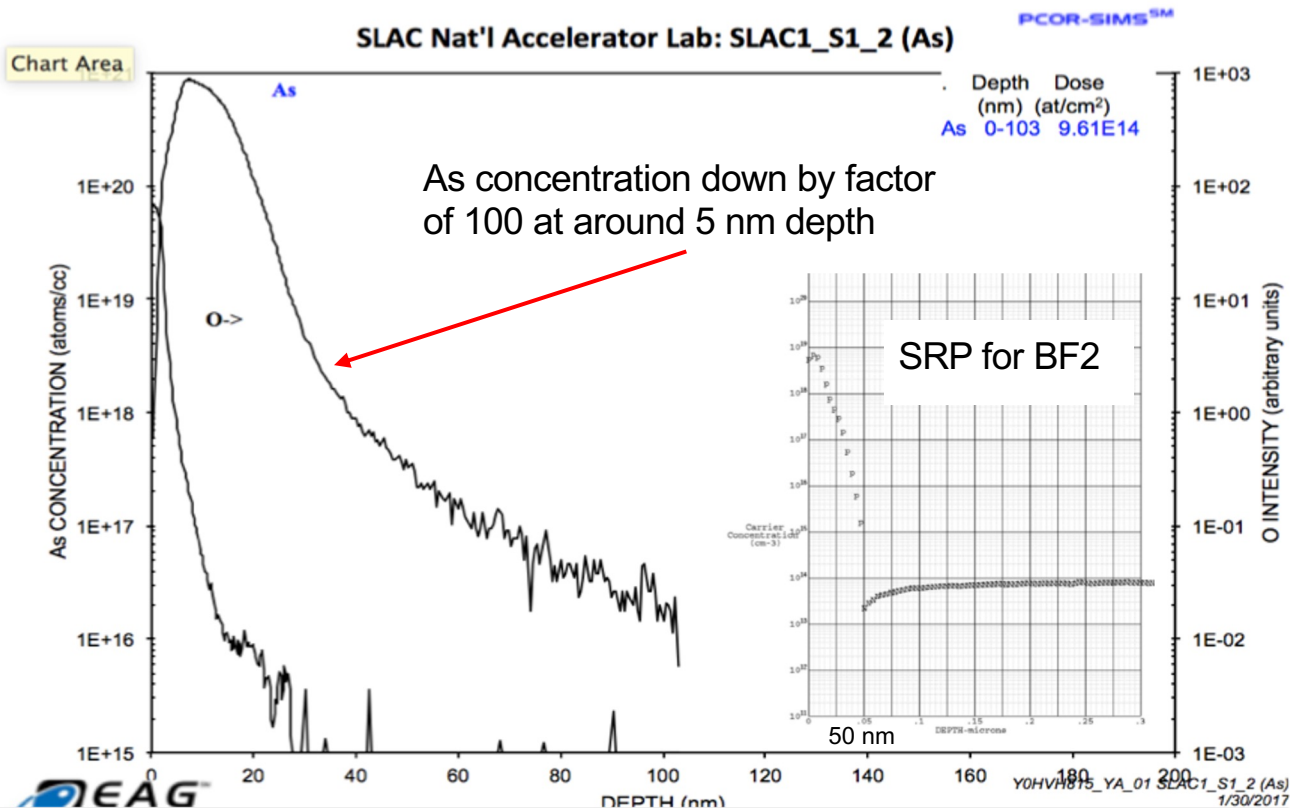
Read-out current vs position



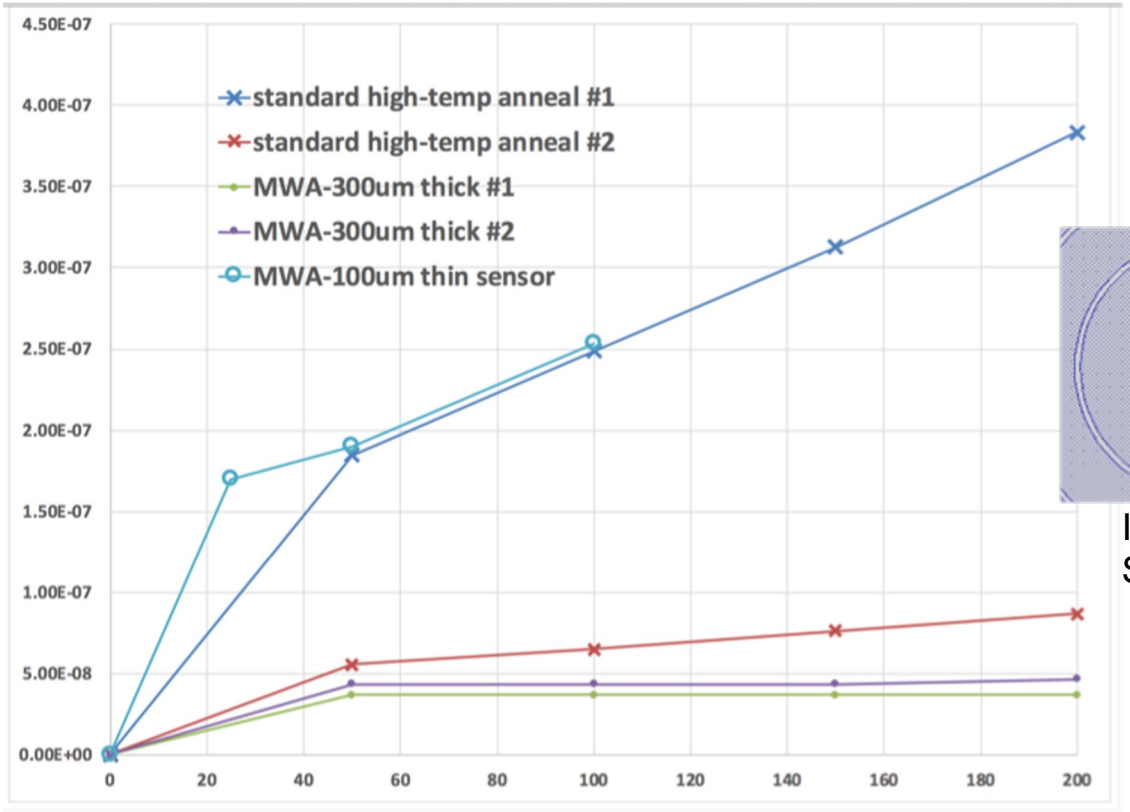


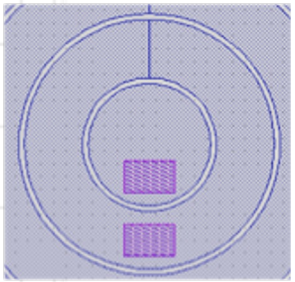
Note: in the case of corner hit, the total current will be 4x shown (shared by 4 pixels)

Shallow As distribution shown by SIMS and SRP



No degradation in sensor due to window process





IV Test Structure