SLAC X-Ray Detector R&D Program

ePixHR250M (ePixM)

a soft X-ray CMOS imager for LCLS-II

Concept Design Review – January 24th 2022

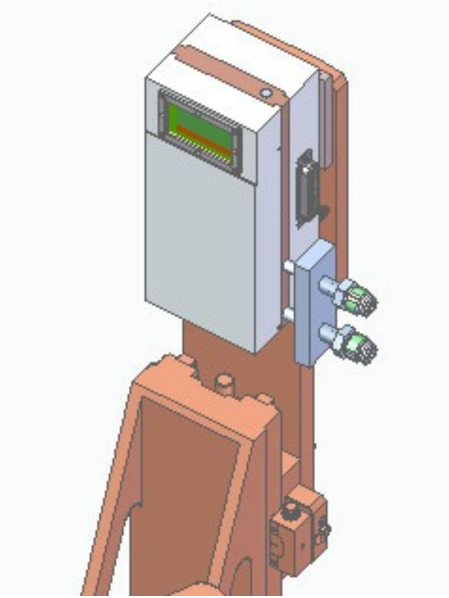
D. Doering, M. Oriunno, S. Boo, C. Kenney,
and A. Dragone on behalf of the SLAC Detector Team

U.S. DEPARTMENT OF ENERGY | Stanford University

SLAC NATIONAL ACCELERATOR LABORATORY

Review organization

- Proposed agenda
    - Introduction, speaker Angelo Dragone
    - Concept design, speaker Dionisio Doering
        - Initial request
        - Derived requirements
        - Electromechanical system concept overview
        - Camera interfaces overview
    - Mechanical system, speaker Marco Oriunno
        - Camera structure and assembly
        - Support structures
        - Cooling
            - Carrier cooling
            - Electronics board cooling
            - Cooling line air guards
    - Q&A



250KPix, >5Kfps ePix HR M detector

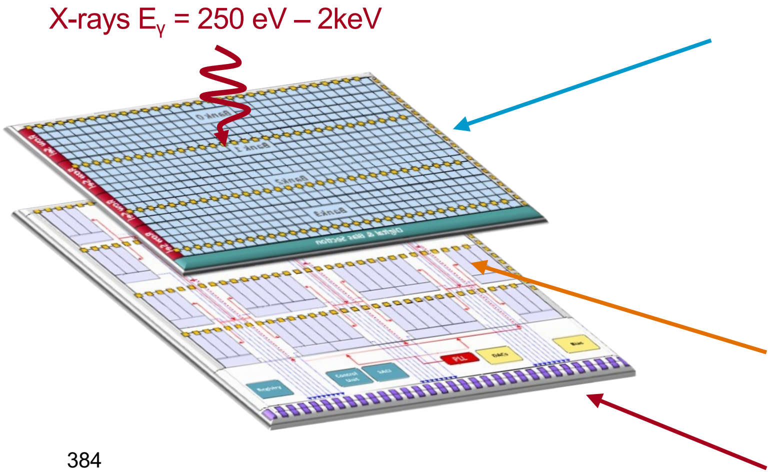
Project Goal

- ePixM project aims at developing a high-rate camera for soft X-rays scattering/imaging experiments at LCLS-II

- Key detector for:
  - Soft x-ray (SXR) resonant elastic X-ray scattering (REXS) experiments in LCLS NEH 2.2
  - X-ray Photon Correlation Spectroscopy (XPCS)
  - Other Coherent Scattering (CS) experiments

Detector Concept

Standard modular hybrid approach



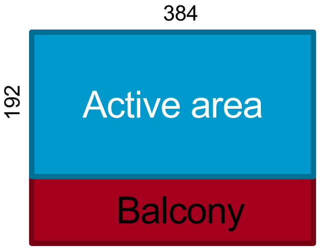
ePixM Monolithic Active Pixel Sensor (MAPS)

- On-sensors amplifier reduces noise → **demonstrated**
- Fully-depleted and back-illuminated → **demonstrated**
- Entrance window optimized for soft X-rays → **demonstrated**

Standard micro-bumps

ePixHR-M Readout ASIC (ROIC)

- 4 arrays of 192 ADCs
- Each array is a copy of the ePixHR back-end → **demonstrated**



CMOS sensor with 384 * 192 pixels.

- Size is 19.772 x 10.371 mm

ePixHR-M readout

- Size is 20.072 x 14.932 mm

Readout ASIC and Sensor status

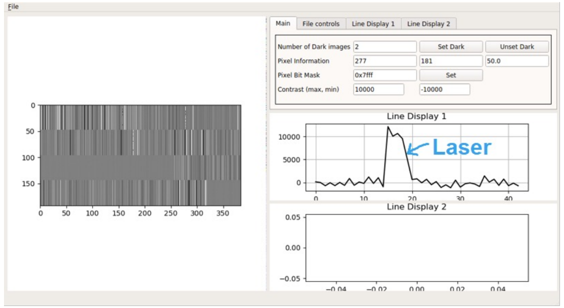
Sensor performance demonstrated with small, wire-bonded pixel matrix:

- full depletion with thin entrance window @ SLAC
- noise = 15.7 e^-, dynamic range = 10^3 photons @ 530 eV

Readout ASIC performance demonstrated

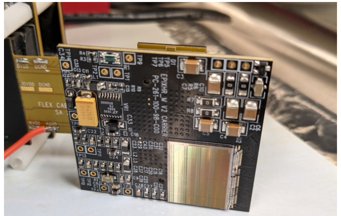
- Stand alone tests shows ADC conversions and linearity

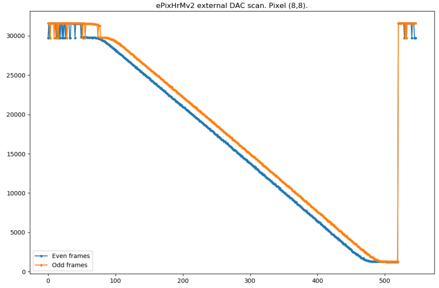
ePix carrier board with ePixHR-M back-end and sensor



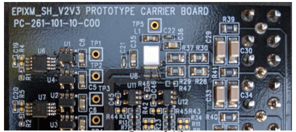
Number of Dark images: 2
Pixel Information: 277, 181, 50.0
Pixel Bit Mask: 0x7fff
Contrast (max, min): 10000, -10000

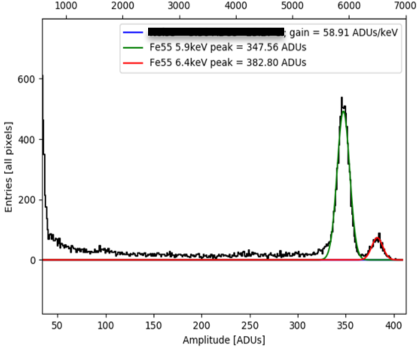
ePix carrier board with ePixHR-M back-end

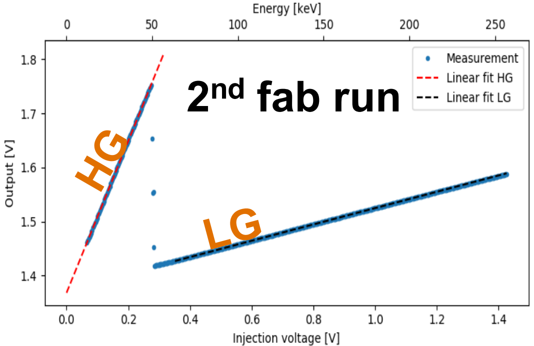




ePix carrier board with ePixHR-M sensor

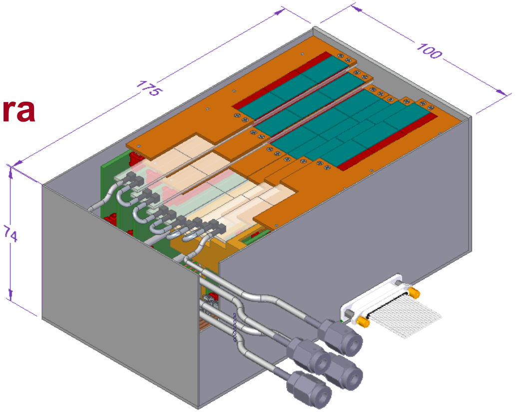




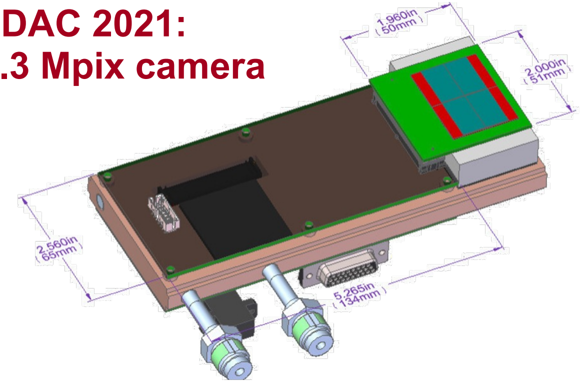


Evolution of ePixM camera designs

May 2021:
1 Mpix camera



LDAC 2021:
0.3 Mpix camera



- Down-selection in May 2021: we presented the design of a 1 MPix shingled camera
- Following advice from the LDAC review panel, LCLS decided that a smaller camera would be a better solution towards a science-ready camera in 2023
- Concepts developed for ePixM shingled camera re-used in TXI camera

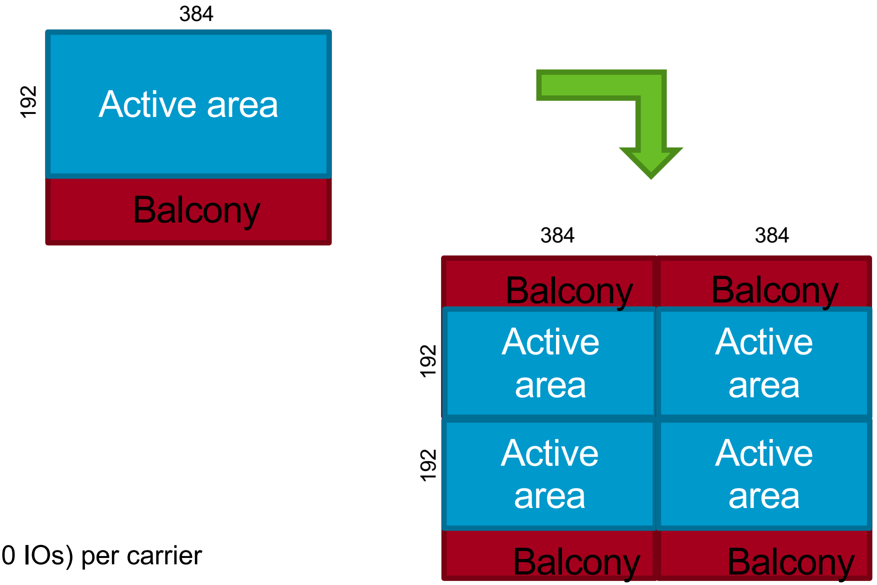
Requirements table

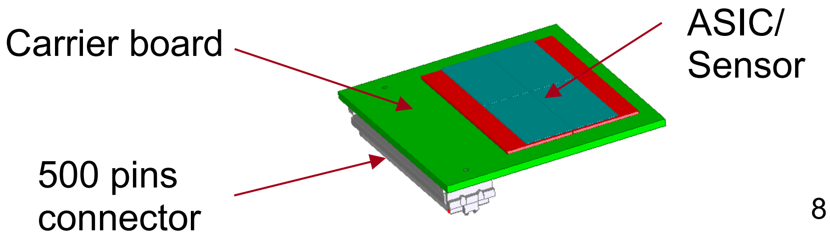
Parameter	Threshold	Objective	REXS	XPCS	CS	0.3 Mpix ePixM
Pixel pitch [um]	50	50	✓	✓	✓	50
Read noise [e^- rms]	15	10		✓	✓	12
Well depth [Number of 530eV photons]	1000	3000	✓	✓	✓	>1000
Quantum efficiency [%, 275eV-1500eV]	70	90	✓	✓	✓	~84
Frame-rate [kHz]	5	10	✓	✓	✓	7.5
Array size [pixels]	512x512	1024x1024	✓		✓	768 * 384
Vacuum outgassing rate [torr*L/s]	2E-8	1E-8	✓			2E-8
Cabling and cooling length [m]	2	4	✓		✓	2
Physical package envelope [WxLxD]	100x175x75 mm	75x150x50 mm	✓			75x175x58 mm
Maximum power dissipation [W]	100*	50	✓	✓	✓	75

* Assuming a 512x512

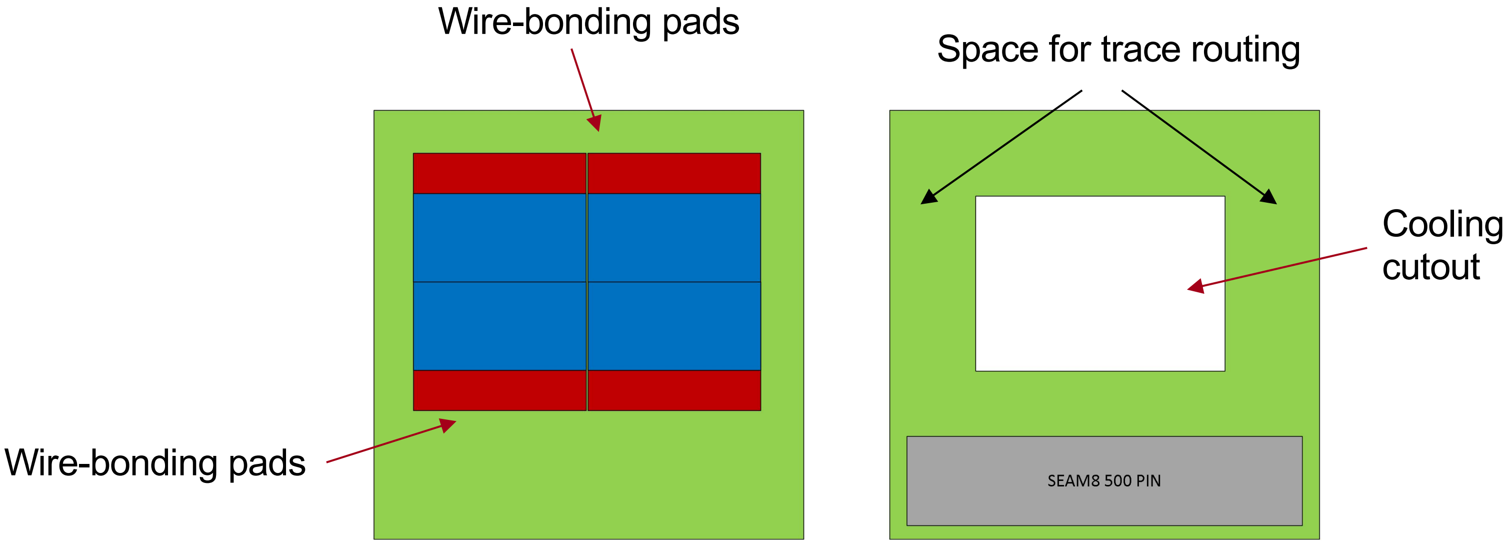
ASIC requirements

- **ePixM single ASIC (7.05W):**
  - 2.5V analog current 1.6A (4W)
  - 2.5V digital current 0.5A (1.25W)
  - 1.8V sensor (analog) current 1.0A (1.8W)
- **ePixM 4 ASICs (28.2W)**
  - 2.5V analog current 6.4A
  - 2.5V digital current 2.0A
  - 1.8V sensor (analog) current 4.0A
- **Other ASICs power requirements**
  - Bias (Guard ring, ...)
  - HV sensor bias (external supply)
- **IO requirements**
  - ePixM 24 outputs/ASIC or 120 differential pairs (240 IOs) per carrier
  - Readout clock 4 pairs (8 IOs)
  - Single ended controls (>20 IOs)
  - SACI (8 IOs)
  - Temperature sensor and serial number (5)
  - Power and ground pins (>50)
  - Total ~330 IOs





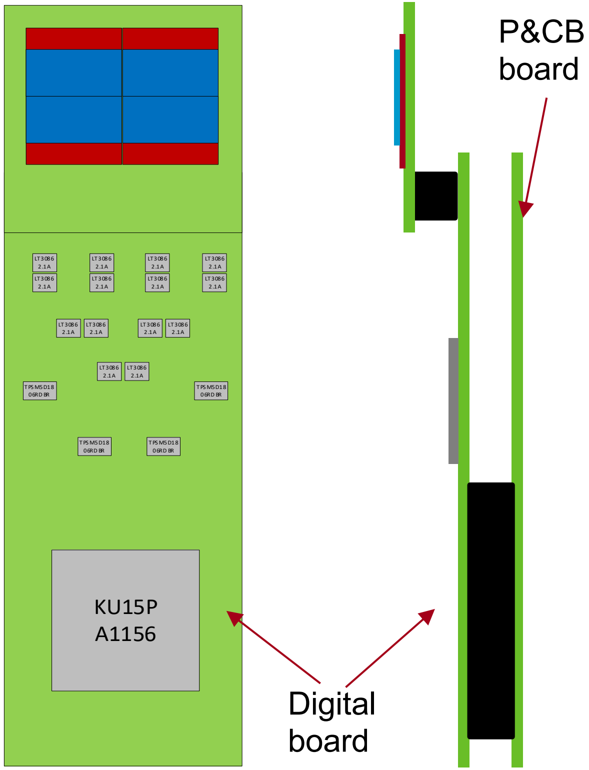
Carrier board (top/bottom)



- Dead area on the sides
- Drawing shown width ~50mm, but may need to go wider for routing signals to 2 upper ASICs

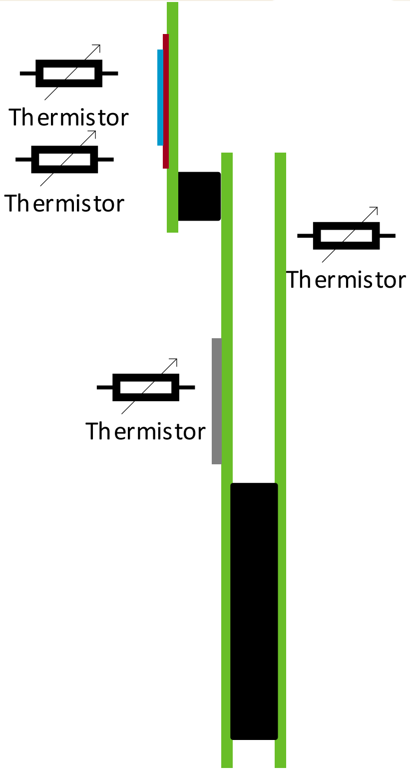
Camera boards stack-up

- Digital board (FPGA) moved to the top
- Carrier board connected directly to the digital board (high number of IOs)
- ASIC power supply (DCDCs+LDOs) on the digital board
- Power and communication board
    - Optical transceiver (QSFP, Leap-on, Samtec)
- Additional components to allocate to lower or upper board:
    - Power input connector
    - Monitoring ADCs
    - DACs



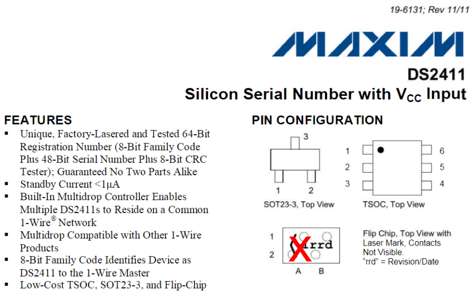
Temperature reading

- Carrier Thermistors
  - 1 to analog ADC to monitor temperature via FPGA
  - 1 routed to the external connector
- Digital board Thermistor
  - 1 to analog ADC to monitor temperature via FPGA
- P&CB Thermistor
  - Just routes carrier thermistor out to the external controller



Serial number

- All serial numbers report to the FPGA
- Together with FW number they compose the camera ID
  - NAME_FwSN_SN_SN_CarrierSN
- Carrier board
  - 1 serial number IC 64 bits
- Digital board
  - 1 serial number IC 64 bits
- P&CB board
  - 1 serial number IC 64 bits



19-6131; Rev 11/11

DS2411

Silicon Serial Number with V_{CC} Input

FEATURES

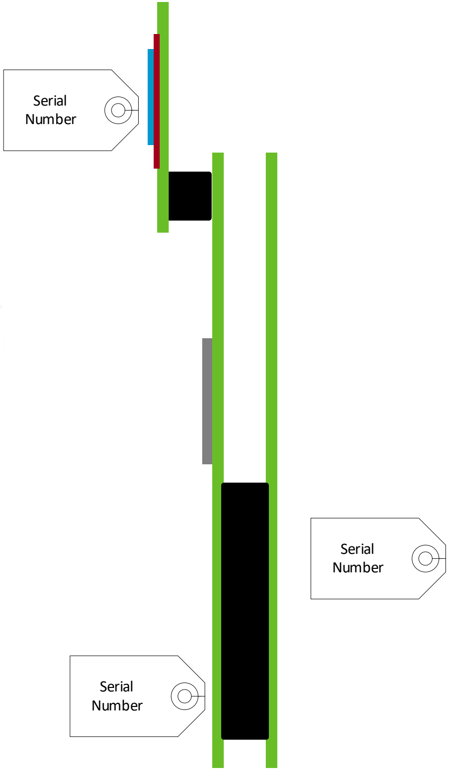
- Unique, Factory-Lasered and Tested 64-Bit Registration Number (8-Bit Family Code Plus 48-Bit Serial Number Plus 8-Bit CRC Tester); Guaranteed No Two Parts Alike
- Standby Current <1µA
- Built-In Multidrop Controller Enables Multiple DS2411s to Reside on a Common 1-Wire® Network
- Multidrop Compatible with Other 1-Wire Products
- 8-Bit Family Code Identifies Device as DS2411 to the 1-Wire Master
- Low-Cost TSOC, SOT23-3, and Flip-Chip

PIN CONFIGURATION

SOT23-3, Top View

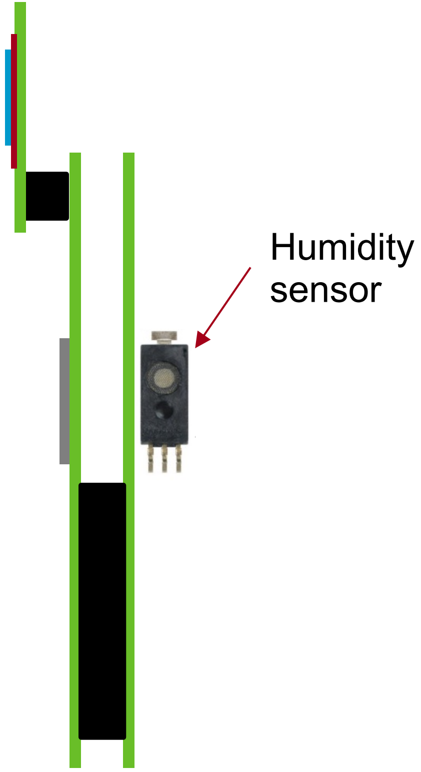
TSOC, Top View

Flip Chip, Top View with Laser Mark, Contacts Not Visible.
"rrd" = Revision/Date



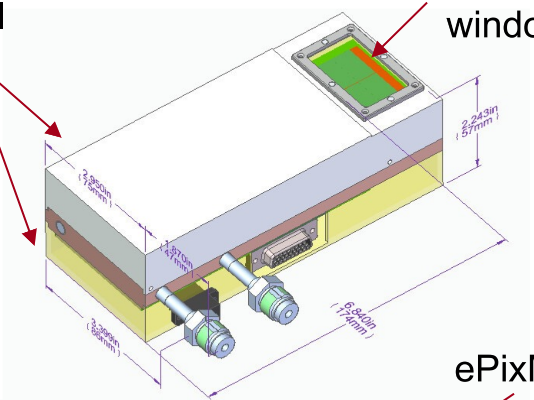
Humidity Sensor

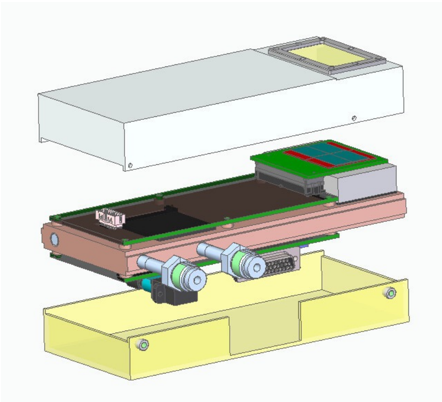
- One humidity sensor per system
  - HIH_5031_001 will be constantly monitored using an independent stream that contains

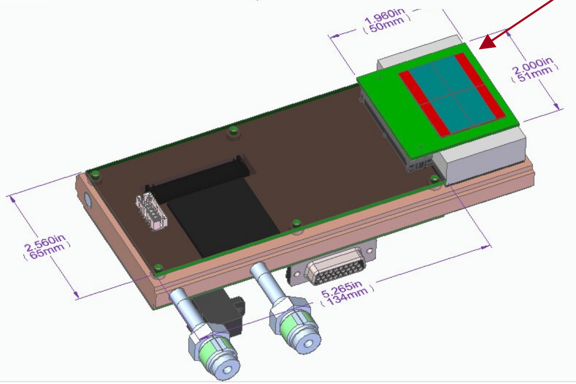

Humidity sensor

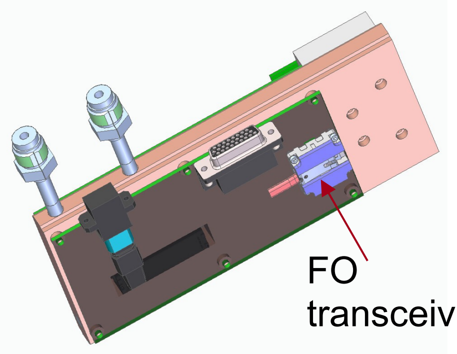
Electro-mechanical system

- Overall dimensions
  - 75x175mmx58 (100x175x75mm)
- Side entrance window
  - With removable shield
- Cooling lines
  - One inlet and one outlet
  - Flexible roses to enable better integration with vacuum chamber

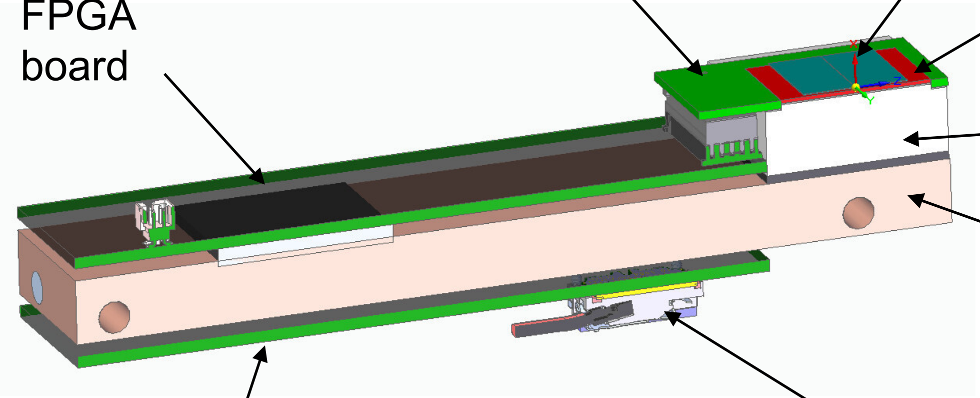








Electro-mechanical system



ePix M – sensor

ePix M – readout

Carrier board

FPGA board

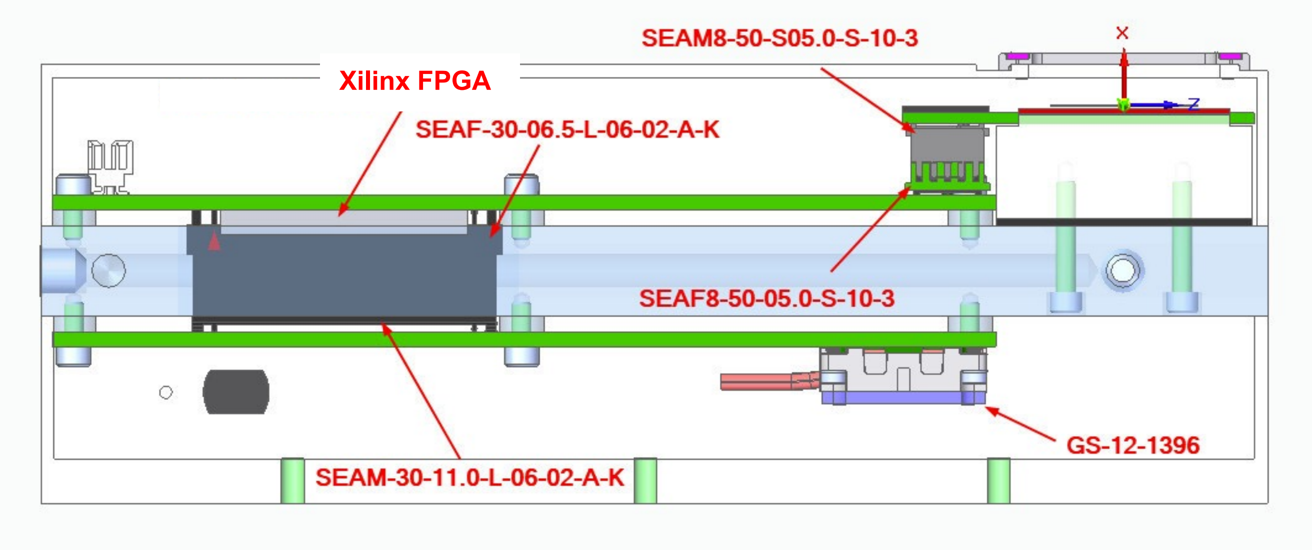
Silicon Carbide strong back

Copper cooling block

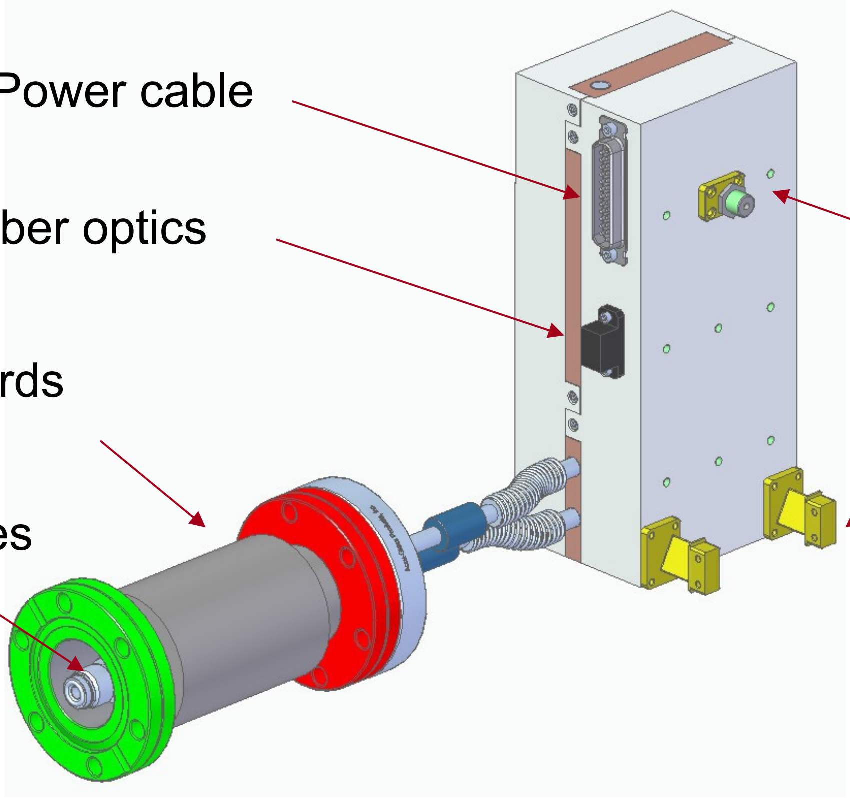
Power and Communication board

Transceiver

Board to board connector interfaces



Interfaces



Power cable

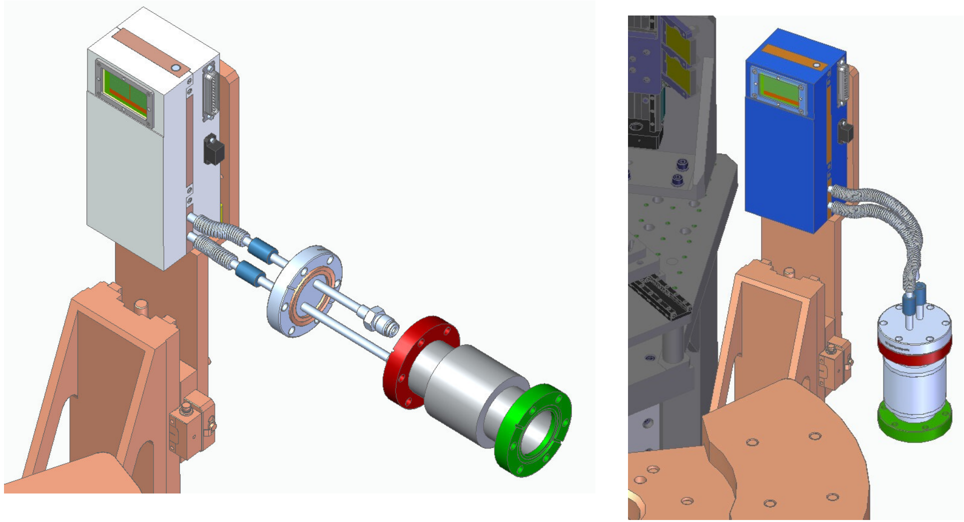
Fiber optics

Air-guards

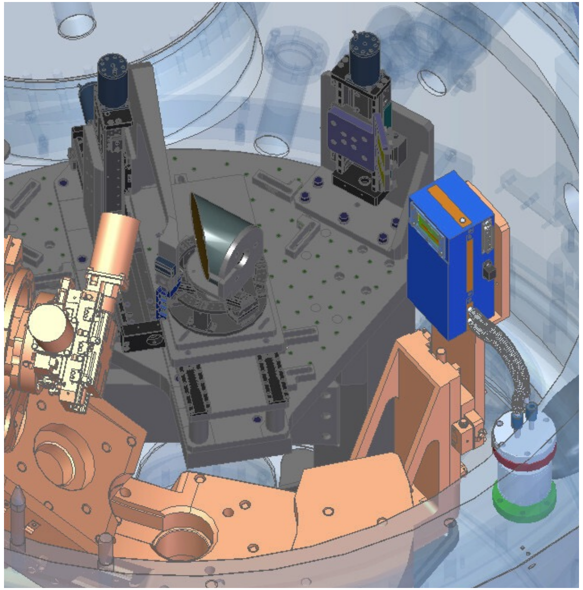
Cooling lines

Kinematic
Support structure

Preliminary Integration study with the RIXS

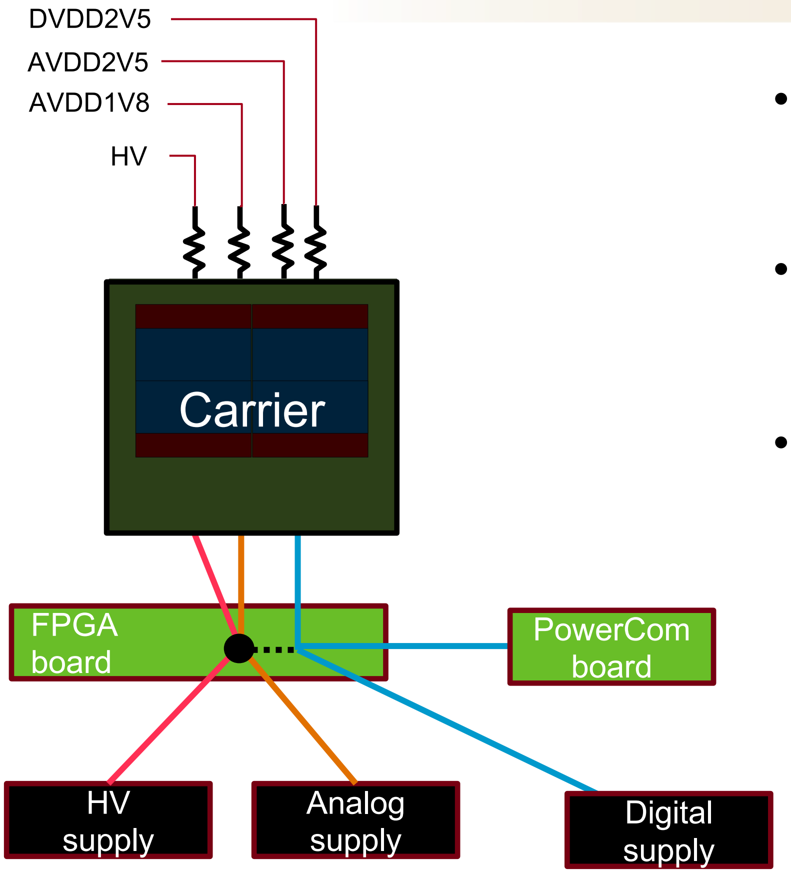


Flexible cooling lines

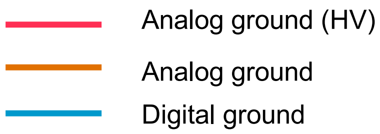


Integration with
experimental chamber

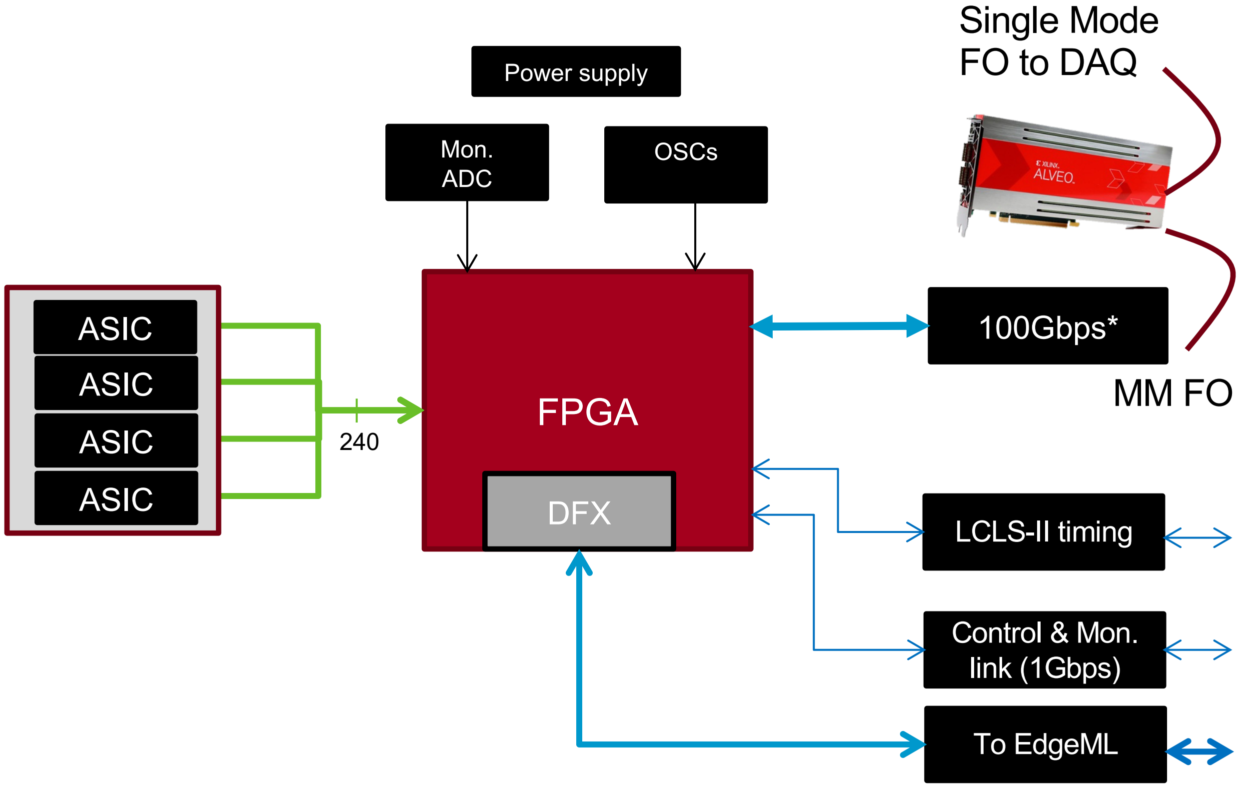
Grounding diagram



- Analog supply should be isolated from digital supply
- Bias return is common with matrix return (cleaner)
- Digital and analog ground are connected at the analog board via zero ohm resistor



Camera data flow

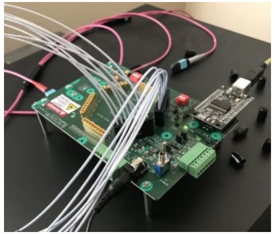


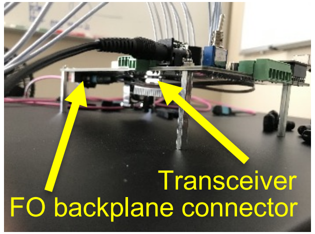
- ePixM 7.5 kfps
  - ePixM 384x192 pixels/ASIC
  - ePixM data rate
    - 384*192*16*4*7500*66/64 = 36.5-Gbps
- ePixM 25 kfps (Forward compatibility)
  - ePixM 384x192 pixels/ASIC
  - ePixM data rate
    - 384*192*16*4*25000*66/64 = 121.7-Gbps
- Dynamic Function eXchange (DFX)
  - enables dynamic optimization of the data pre-processing
  - Image acquisition and control static
  - Can be tailored for custom user application or edgeML needs
  - Not part of this project

*On this camera it will be limited to 4x16.3Gbps due to FPGA transceivers restrictions

Interface – Fiber opticst communication

- Fiber optics testing
  - 12 x 25Gbps
    - Data, timing and control
  - PRBS
    - PGP2b at 3 Gb/s (ok)
    - PGPv4 at 6 Gb/s (ok)
    - PGPv4 at 10 Gb/s (ok)
    - PGPv4 at 12 Gb/s (ok)
    - PGPv4 at 15 Gb/s (ok)
    - PGPv4 at 25 Gb/s, max rate (ok)

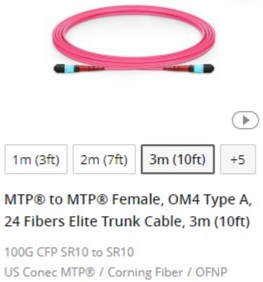




ed speeds already meet experiment requirements

Amphenol
300 Gbps (12 x 25Gbps), 25 x 25 x 8 mm

https://www.amphenol-icc.com/product-series/leap-on-board-transceiver.html

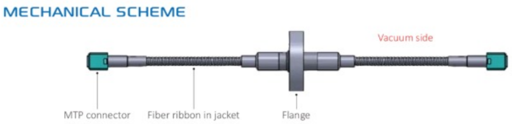


MTP® to MTP® Female, OM4 Type A, 24 Fibers Elite Trunk Cable, 3m (10ft)

100G CFP SR10 to SR10
US Conec MTP® / Corning Fiber / OFNP

Customized MTP® 24 Fibers OM4 Multimode Conversion Harness Cable

RETA-RIB-CF40-24-050a-2-S70-11b



https://www.lasercomponents.com/fileadmin/user_upload/home/Datasheets/sedi/fibre-optic-ribbon-hermetic-feedthroughs.pdf; https://www.sedi-ati.com/

Management plan

- SLAC Detector R&D projects follow LCLS project management guidelines
  - CDR conducted before project starts
  - Financial plan approved by the PEC before start
  - Documented using Microsoft Project
  - Bi-weekly meetings to follow status are conducted together with the project sponsor (LCLS)
  - Milestones are tracked and if requires re-baselines or the project are implemented

	Task Name
1	ePixHR250M 320kPix REXS/SXR
2	Management
5	Flip Chip Hybridization
6	Sensor Thin Window fabrication
7	Pos, layouts, tehnical discussions with vendors
8	Modules bonding 1st Batch
9	Module Bonding 2nd Batch
10	Engineering Design
11	Mechanical Design (Optimization from HR)
12	Mechanical design intermediate review
13	Design of the cooling structure (Optimization from HR)
14	Design of the enclosures and windows
15	Electronics Design (Optimization from HR)
16	Schematics
17	PCBs layout
18	Electro-mechanical Integration
19	Thermal Analysis
20	Manufacturing Readiness Review
21	Mechanical Components Procurement
25	Electrical Components Procurement
35	Modules Assembly
40	REXS Camera Assembly
44	SXR Camera Assembly
48	Firmware Optimization
51	X-Ray Tests and Support for LCLS Testing
52	Produce Documentation
53	Transfer Cameras to Operations
54	Detector Engineering Calibration
55	Closeout Review

Construction Plan: Milestones and Deliverables

- Schedule is aggressive and represents the best we can do to meet the experiment schedule.
- At the same time this is feasible within assumptions added to the risk table
- **Deliverables:** x2 ePixHR250M 0.3 MPix cameras (1 for REXS and 1 for XPCS)

Key Milestones	Planned Date	Goal
Electro-mechanical design started	06/16/2021	Detector concept development including hutch integration
Preliminary Design Review	01/24/2022	Concept review
Detailed Electro-mechanical design completed	03/15/2022	Complete Detector design
Final Design Review	04/15/2022	Manufacturability review
Component's fabrication starts	04/18/2022	Parts fabrication and procurement
Firmware Design completed	08/08/2022	Fully operational boards
Component's fabrication completed with qualification	07/01/2022	Parts fabricated and qualified
Modules and Detector Assembled	01/30/2023	Assembled deliverables
Detector Characterization and Integration	02/24/2023	Parameter optimization and hutch integration
Detector Delivery Starts	03/06/2023	Transfer to operations
Project closeout	04/10/2023	

Summary

- Sensor: meet requirements, 2nd fab run to build stock and small improvements
- Back-end ASIC: new version is being tested, updates soon…

- Assembled module prototypes:
    - Identified faulty electrical connections on bumps
    - Issue investigated
    - Next steps: dense mechanical bump array plus solder bumps on existing sensors by IZM

- Camera design: priority shifted from 1 Mpix shingled design to 0.3 Mpix camera
- Design on-track for camera delivery

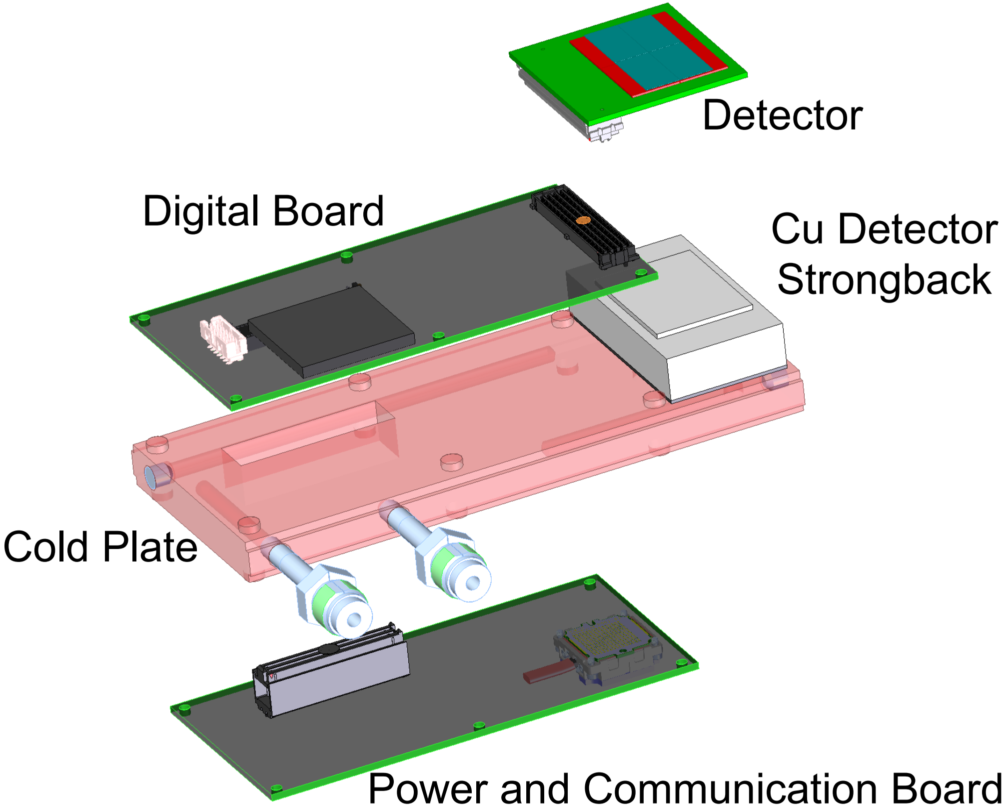
BACKUP

Cooling loads (remove)

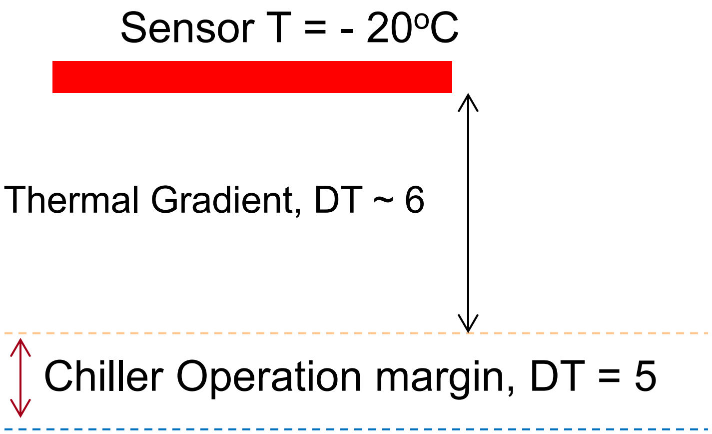
ASICs and Sensors, 28 W (7 W/each)

Digital board, 36 W
- 10 W LV regulator
- 26 FPGA

Power and Communication Board, 10 W
- 6 W Transceiver
- 4 W other comp.



Coolant choice (for details, see Marcos' talk)



Sensor T = - 20^{o}C

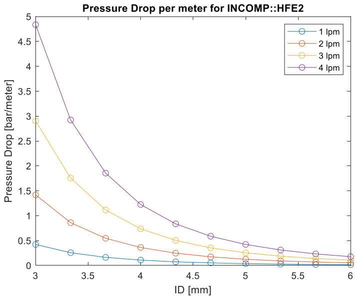
Thermal Gradient, DT ~ 6

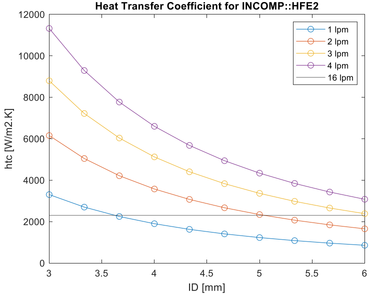
Chiller Operation margin, DT = 5

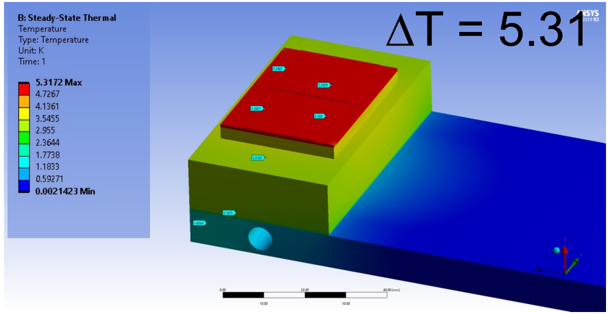
T Coolant required < - 30^{o}C

3M HFE-7000 refrigerant

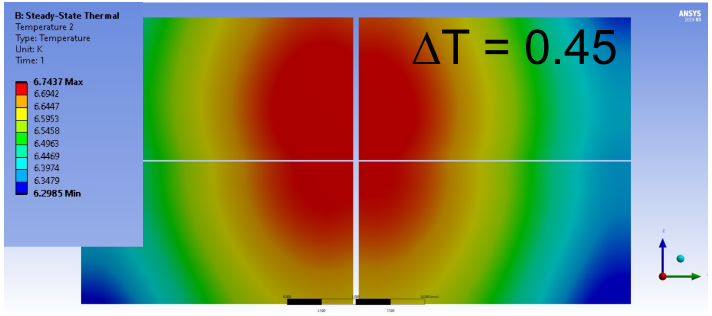
low viscosity, low pressure drop







ΔT = 5.31

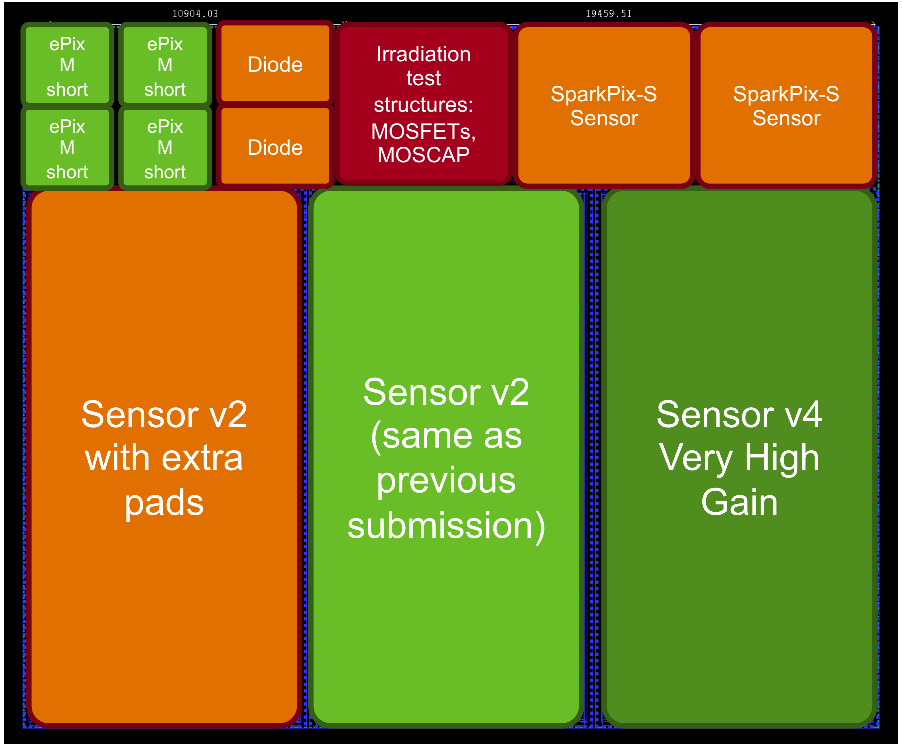


ΔT = 0.45

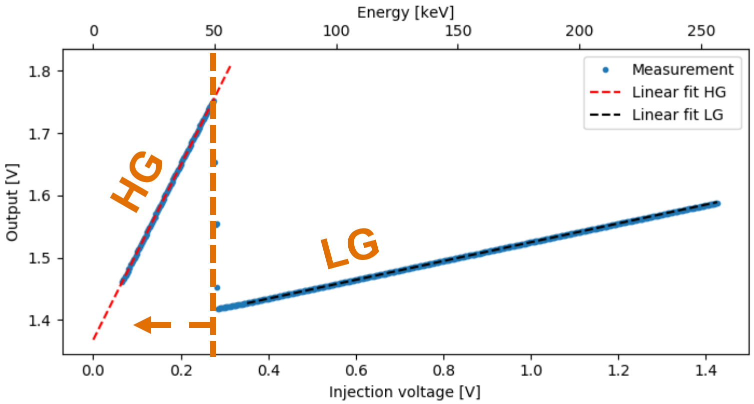
New production run

- New tape-out with LFoundry 150 nm in August 2021 to have additional sensors for production
- Delivery: March 2022

- **Floorplan:**
  - Sensor v2 (current design)
  - Sensor v2 with Very High Gain
  - Sensor v2 with extra pads
  - Small matrixes
  - Test structures



Gain & switching point optimization

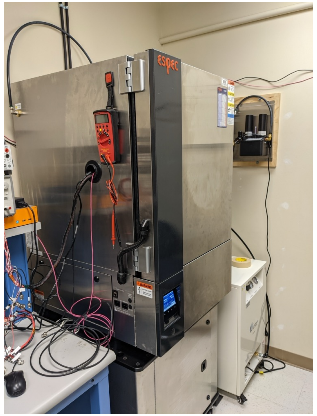


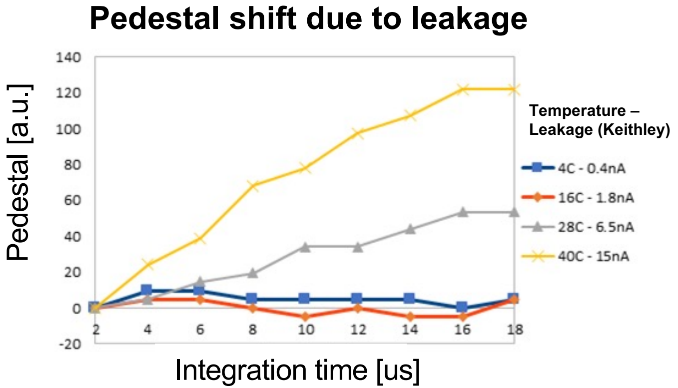
		Sensor v2	Sensor VHG
High gain	Range HG [keV]	50	25
	ENC [e^-]	15.7	< 15
	Single-ph. res. [e^-]	15	
Low gain	Range LG [keV]	500	
	ENC [e^-]	< 140*	
	Statistical limit [e^-]	982	491

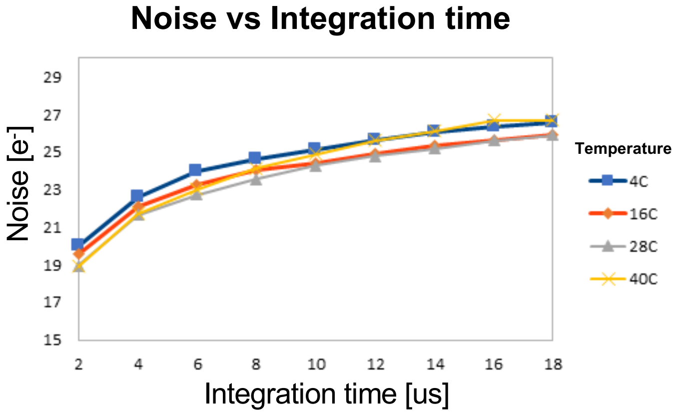
* Includes calibration signal noise

- Current design: switching point HG → LG @ 50 keV
- Conservative: novel “correlated pre-charging” technique to reduce noise in LG, never tested
- Works as expected: **noise in LG is well below the Poisson statistical limit**
- One flavor of large/small sensors in new tape-out with Very High Gain mod (smaller C_{fb}):
  - move switching point to lower energy (~25 keV)
  - reduce impact of downstream readout stages (SF, ADC) on noise in HG region

Operating temperature

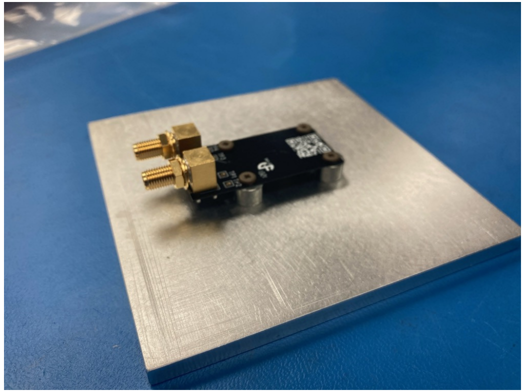




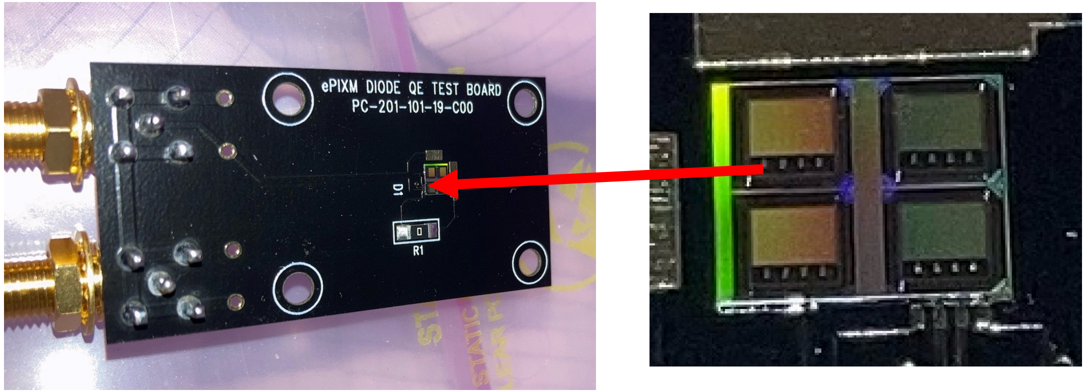


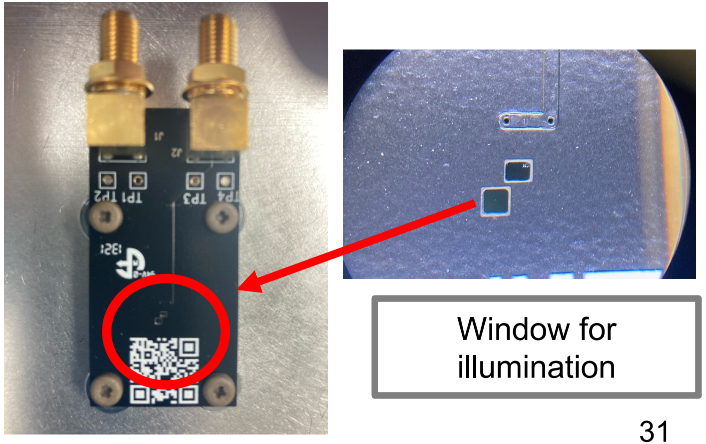
- Installed environmental chamber to study performance vs temperature
- Noise slightly higher change with lower temperature
  - → more tests needed, possibly due to different bias
- Sensor does not require -20°C → **cooling specs can be relaxed**
- Final operating temperature to be determined with assembled module tests

QE Measurement for Entrance Window to confirm simulation results



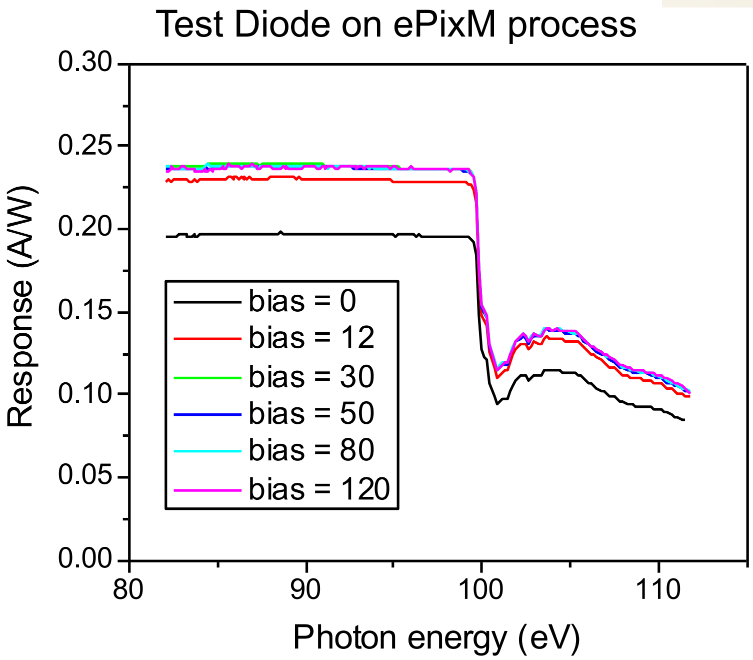
- System tested at ALS beamline 6.3.2 (Eric Gullikson)
- Test diodes from ePixM sensor wafers, thinned to 115 um with shallow BF2 entrance window (microwave annealed)
- Same wafer as the Fe-55 spectrum was acquired with

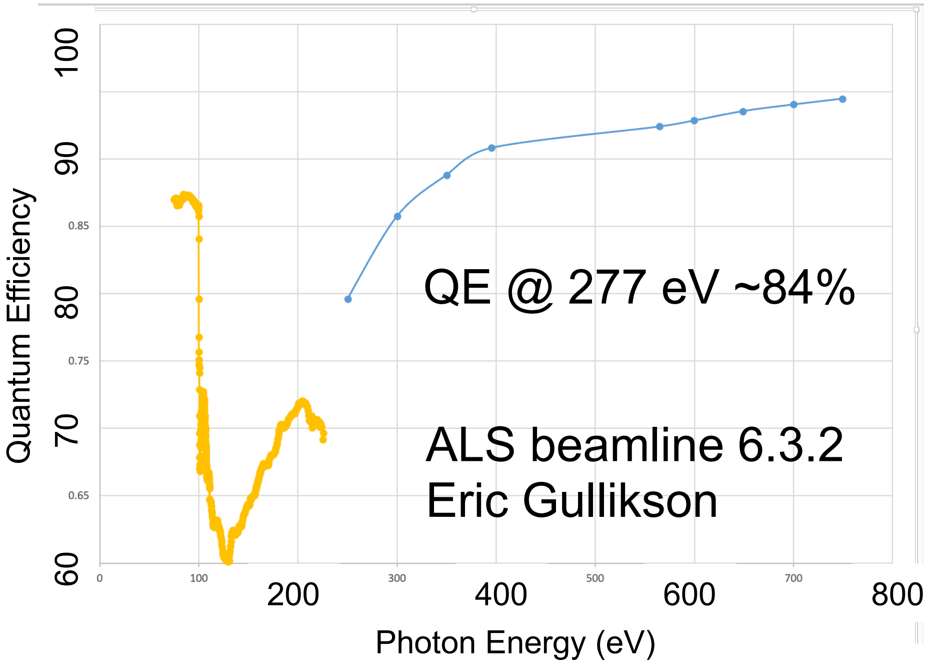




Window for illumination

Preliminary QE Measurement Results





QE @ 277 eV ~84%

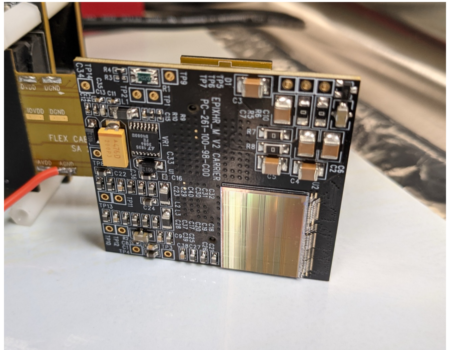
ALS beamline 6.3.2
Eric Gullikson

BF2 entrance window post-processed on foundry CIS sensor, 115μm thick.

As entrance window on SLAC planar sensor wafer, 300μm thick

Back-end V2

- Received 2nd version of back-end ASIC with better supply distribution and
- Engineer previously working on FPGA/testing/camera left SLAC → delays…
- **Improvements:**
  - Skew on data output lines reduced by 80%→ was causing sync issues at 5 kfps
  - Fixed: non-deterministic ping-pong on even/odd pixels, needed 2 dark images



ePix carrier board with ePixHR-M back-end

Add latest results…

Back-end V2

Add latest results…

ePixM Bump Bonding is Challenging and Essential

- **Missing power/control bumps are fatal**
- Must be back side illuminated
  - Requires thinning wafer to ~115 microns for full depletion
  - Shallow diffusion plus ultra-thin dielectric/metal films
  - Thin window is fragile
- Power/control bumps are near one edge of the chip
  - Where alignment and chip curvature are most sensitive
- Sparse arrangement of bumps across chip
  - Few bumps per cm2 means lower adhesive forces
  - Nonuniform distribution of bumps creates nonuniform bonding pressures

Many Unsuccessful Attempts at Bump Bonding

2020

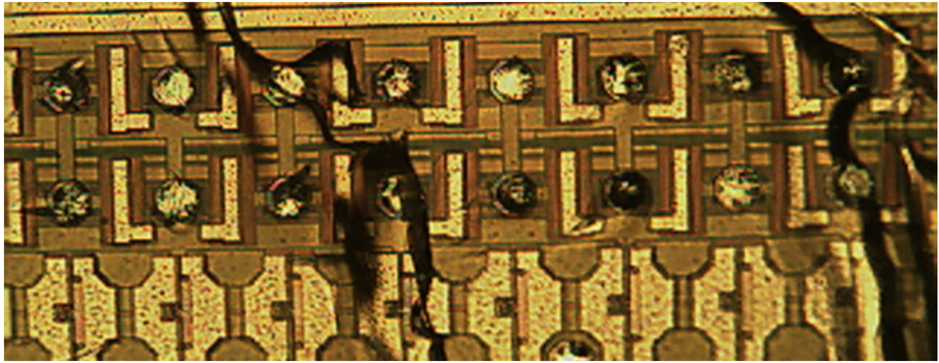
- Thin 200mm wafer
- Core out 150mm wafer center
  - Stanford can only handle 150mm
  - Outer 2-3cm of wafer coated with glass
- SLAC performed lithography for bump patterning and bump deposition
- SRI (local company) performed lithography on subset of wafers
- Trouble with thin, large wafers breaking
- SLAC flip-chip bonded multiple sets with process variations

More Unsuccessful Attempts at Bump Bonding

2021

- Contracted Micross to bond SLAC-bumped chip pairs (3 recipe attempts)
- Contracted Advacam to bond SLAC-bumped chip pairs (7 recipe attempts)
- Used underfill
- SLAC worked with flip-chip vendor to make a special chuck
- SLAC bump and bonded 700um thick, 150mm wafers
- Performed autopsies on failed modules

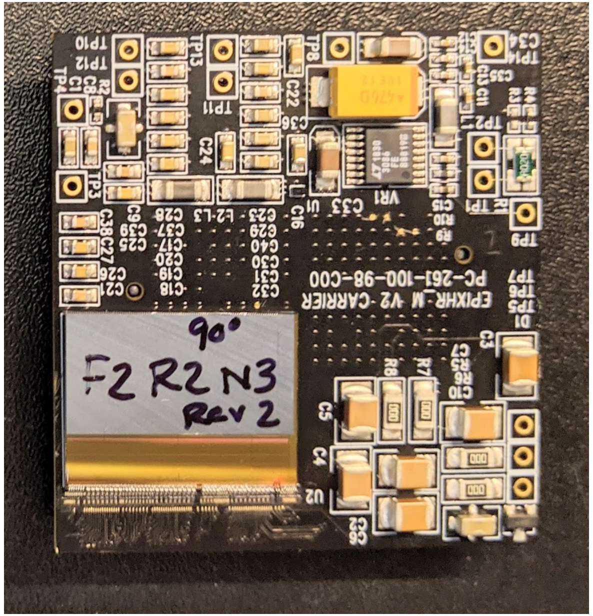
Difficult to interpret, but most of the bumps appear to have been aligned and bonded to their counterparts. White indicates a reflective, flat, smooth surface



Despite these Efforts, No Working Bonded Modules

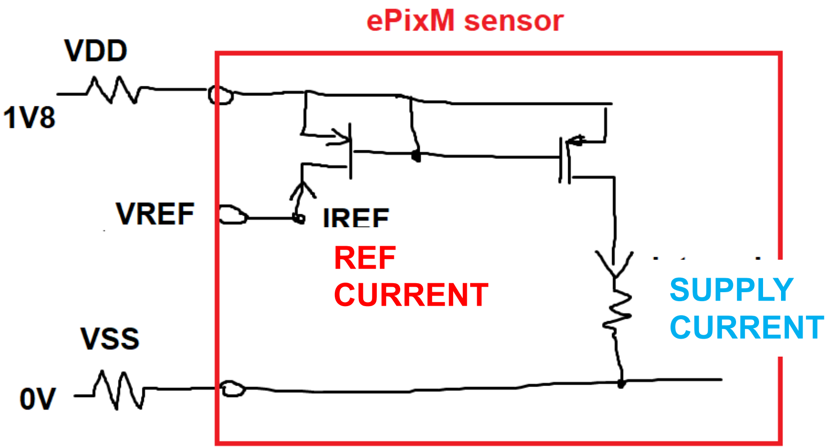
- When testing sensor+back-end bump-bonded:
  - Most modules show no current consumption on sensor supply
  - Few modules consuming 20% of nominal power and one drawing nominal power, but were not functional

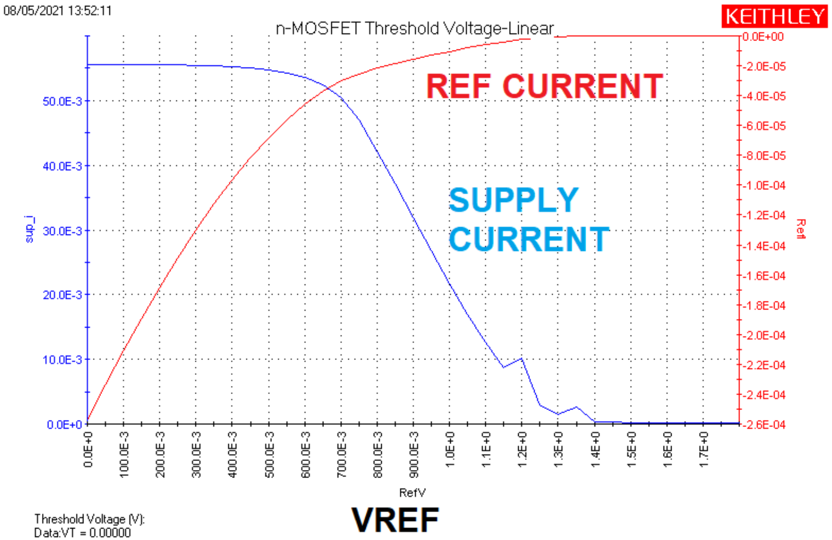
- Cause: missing electrical connection between biasing circuits on back-end ASIC and sensor
- Supply, references for bias circuits and control signals are distributed through bumps from the back-end to the MAPS



ePix carrier board with ePixM MAPS bonded on ePixHR-M back-end

Large-chip, sensor bias verified with probe test

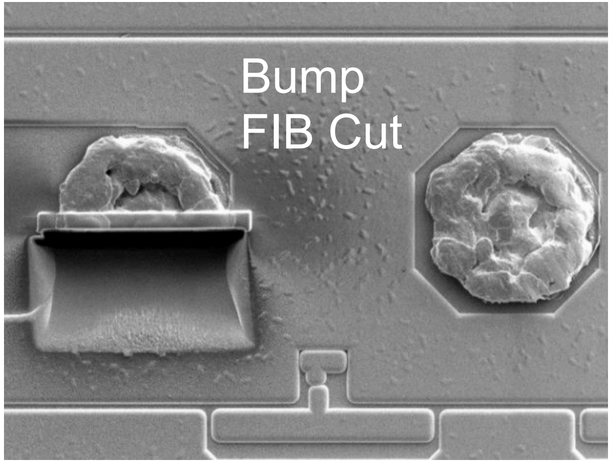


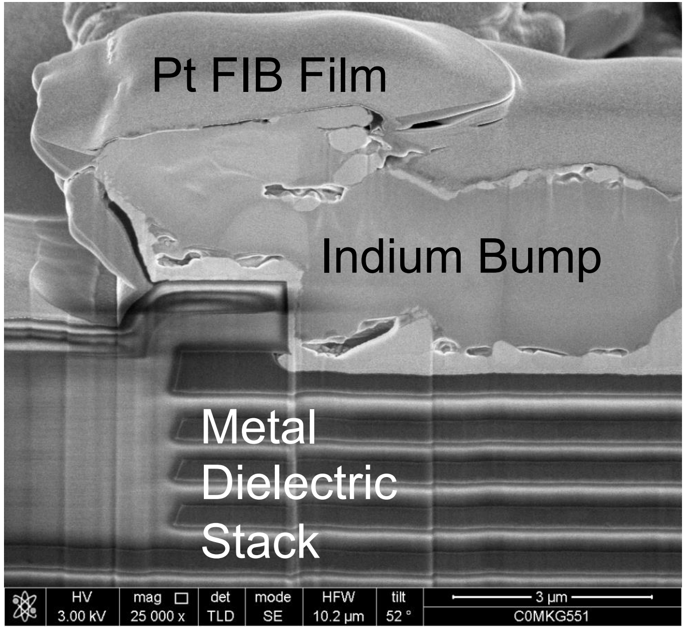


- Circuitry on large-scale MAPS is almost identical to smaller matrix
  → unlikely that there are bugs in the circuitry
- Test large MAPS independently to verify biasing / power consumption
- Connected VDD/VSS/Ibias through microprobes on probestation
- Measurements match simulations → sensor biasing looks functional

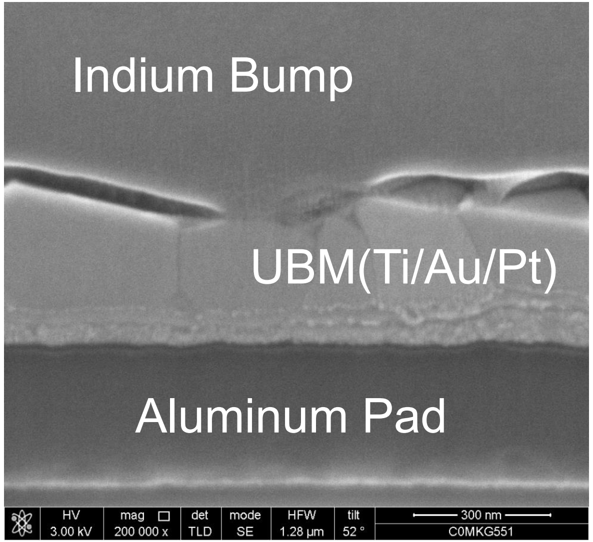
No Evidence of Residual Insulating Layer on Pads

- FIB cross sections
- Look for film between aluminum pad and indium/UBM
- No clear evidence for insulating film





Bump_006

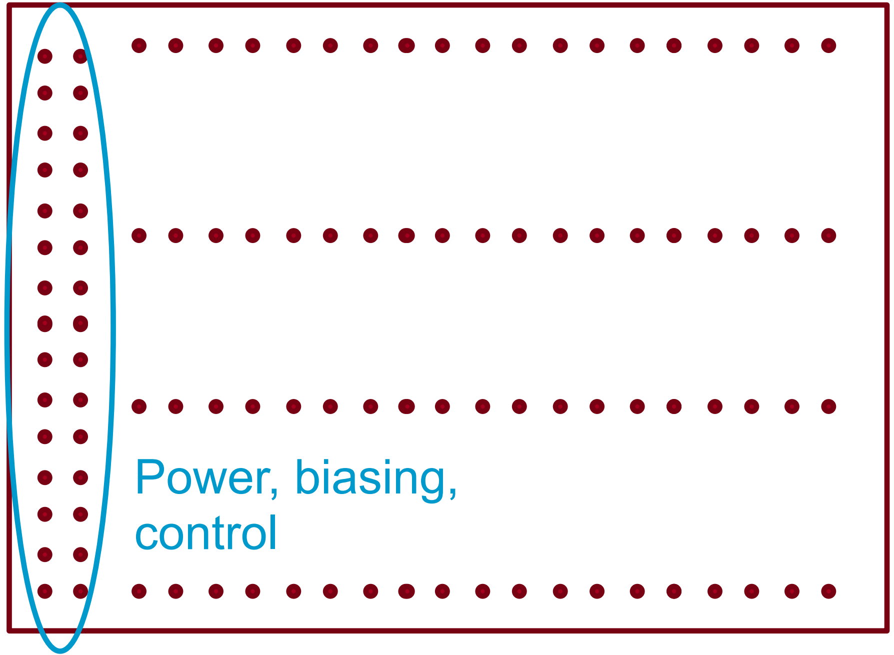


Bump_013

UBM
Stack

Is Unusual Sparse Bond Array a Problem?

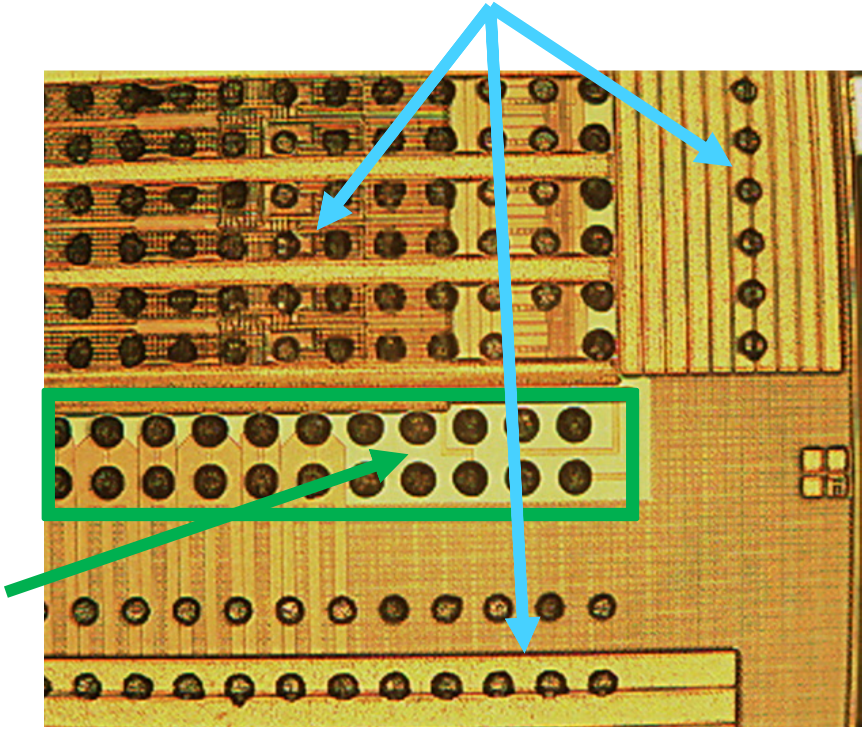
- Distribution of bumps on sensor and back-end ASIC is not uniform
- Large area, but relatively few bumps → low mechanical strength



Sketch of die floorplan with bump locations

Add Mechanical Bumps

- New mask for bump deposition with mechanical bumps
- Mechanical bumps are deposited on passivation, no electrical connection
- Better uniformity → higher mechanical strength and reliability
- More bumps around the corners → enclose critical ones
- SLAC processing thick sensors with mechanical bumps and sputter pre-etch in-house for quick turn



Preparation for Bump Bonding of Science Modules

- Prior to shipping to flip-chip vendor, SLAC must:
  - Half of batch left 200mm and half cored to 600mm
  - Thin 600mm and 200mm wafers down to about 130 microns
  - Polish back surface
  - Implant (current step)
  - Metal deposition
  - FGA anneal?
  - Microwave anneal
- All without breaking these thin wafers
- This program is occurring now to vet process using blank wafers

Commercial Flip-Chip Bonding by IZM

Batch IZM-0

- 700 micron thick sensor wafer – no entrance window – lowest risk
- Mechanical bumps included
- Launched over summer expect back by end of CY2021

Batch IZM-1

- First science modules
- SLAC will thin, polish, implant, metalize, anneal sensor wafers
- Send to IZM by end of CY2021 and receive Q1/Q2 CY2022

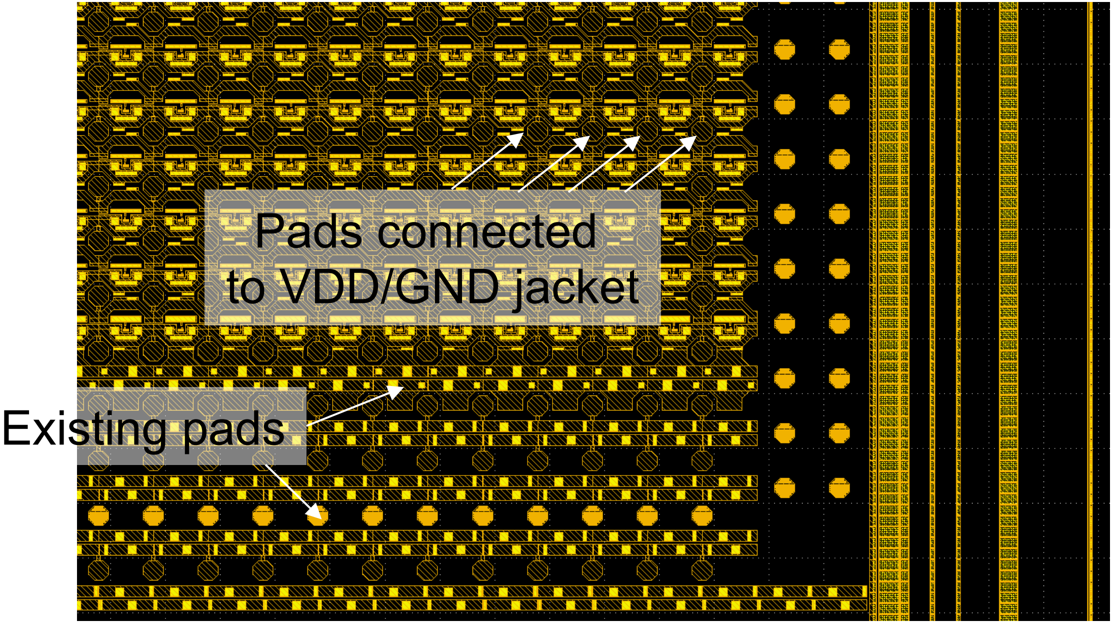
Batch IZM-2

- Start at least partway through IZM-1 processing to incorporate lessons learned and to reduce risk of single batch failure
- Receive summer CY2022

Flip-Chip Program Takeaways

- **Intense and broad effort to bump bond ePixM**
  - Involved multiple attempts and outside vendors
  - Unsuccessful so far
- **Aggressive plan to bond science modules**
- **Fairly confident that large sensor design works as expected**
  - Large sensor matrix is nearly identical to small sensors which are fully functional
  - Large sensor power consumption verified with probe test

Sensor with additional VDD/GND bumps



- August 2021 run: one version with additional bumps
- Re-Distribution Layer t.b.d. on back-end ASIC for electrical connection

Risk management

Risk	Likelihood/Impact	Mitigation	Risk status
Unexpected complexity in the design of the camera	**Low/Medium** Schedule delay and increased cost.	**Accept without mitigation**	Retired In R&D
Full size ASIC/sensor module at 5kHz has undiscovered issue	**Low/Low** 5kHz has been demonstrated performance analysis ongoing	**Accept without mitigation**	Active
Flip-Chip Bonding	**High/Medium** Schedule delay and increased cost.	**Use three vendors** **Multiple batches**	Active
Module yield insufficient	**Low/Low** Schedule delay and increased cost	**Module production is more than twice the minimum needed**	Active
FPGA procurement	**High/High** Schedule delay and increased cost	**We are trying to build a stock of FPGAs**	Active
Cooling of modules and related mechanical design aspects	**Medium/Medium** Schedule delay and increased cost.	**Include PDR review 5 months into design / prototype critical components**	Active
Assembly related mechanical design aspects	**Low/Low** Schedule delay and increased cost.	**Include PDR review 5 months into design / prototype critical components**	Active
Fabricated parts have defects	**Low/Low** Schedule delay and increased cost.	**Accept without mitigation**	Active
Metrology and geometry correction aspects	**Low/Medium** Schedule delay and increased cost.	**Analysis to be completed before the FDR**	Active

LDAC 2020 Recommendations

1. *A full system-level thermal analysis is recommended. The SLAC team may consider to build a mock-up of the detector to evaluate the mechanical design before detector modules are assembled.*

→ New camera baseline started with more conventional cooling system

2. *We have not seen wafer-scale QE uniformity data for microwave annealed entrance window. Measurements on uniformity are recommended.*

→ Have performed initial QE measurements on a few chips. Difficult to measure many chips due to assembly, beam time access, etc. and to do so with better than 5% uncertainty. Can't be done at wafer scale. Eventually a flat field with soft x-rays is required and will be performed.

3. *LCLS should evaluate the scientific impact from the ePixM's power dissipation and package size potentially being out of specification.*

→ New camera design addresses this concern