Technical Specification for ITk pixel modules

Summary

This document describes the specifications of the ATLAS ITk pixel module. The pixel module is the basic detection unit of the pixel sub-detector. It consists of a pixel assembly/pixel chip and the module PCB, which holds all the necessary circuity to connect the front-end chips to the services. The specification covers the module PCB as well as the module

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Distribution List

1 Introduction

The ATLAS Inner Tracker (ITk) is the all silicon tracker of the ATLAS experiment, which will be installed as a replacement for the ATLAS Inner Detector during the Phase-II HL-LHC upgrade. It will consist of an outer part made from silicon strip modules and an inner part made from silicon pixel modules.

The pixel sub-detector has the following characteristics:

- In the central region five barrel layers populated with single-, 2- (dual), and 4-chip (quad) modules mounted on support structures.
- In the forward and backward regions endcaps consisting of five ring layers populated with quad, single- and dual modules mounted on support structures.
- The inner two barrel and endcap layers form the inner replaceable pixel system, while the other three layers form the outer non-replaceable pixel system.

Two types of pixel technologies are under study:

- Hybrid pixel modules (baseline)
- Monolithic pixel modules (option for the outer barrel layer)

In the case of hybrid pixel modules, the CMOS frontend (FE) chip is connected to a silicon pixel sensor using fine pitch bump bonding. One or more FE chips maybe connected to a single silicon sensor. This assembly together with the module PCB forms the “hybrid pixel module”.

In the case of a monolithic pixel detector, the CMOS readout chip and the sensor are integrated into one silicon element, the monolithic pixel chip. This monolithic pixel chip together with the module PCB forms the “monolithic pixel module”.

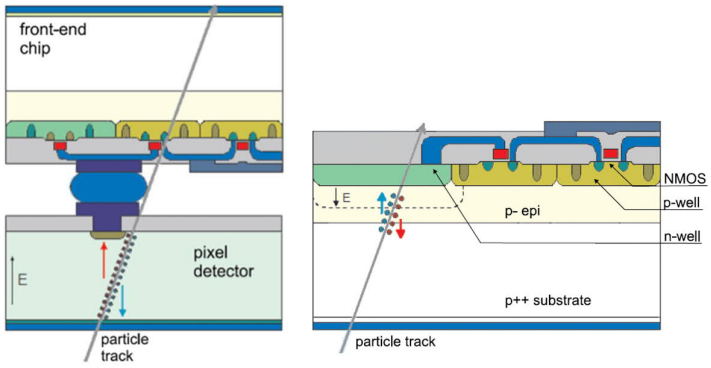

Fig. 1: Schematic view of a hybrid pixel detector (a) and a monolithic pixel detector (b).

2 Convention and Glossary

The acronyms used in this document are:

- ASIC: Application-Specific Integrated Circuit

- FE chip: Front-end pixel ASIC (in case of hybrid pixel assembly)
- Monolithic pixel chip: CMOS pixel chip that includes both the sensing element and the readout elements.
- EoCL: End of column logic area of the FE chip
- Bare hybrid pixel module/bare pixel module: a hybrid pixel module consisting of a pixel chip and a pixel sensor connected via fine pitch bump bonding
- Hybrid pixel module: a bare pixel module with the module PCB attached mechanically and electrically.
- Monolithic pixel module: a CMOS pixel chip(s) with the module PCB attached mechanically and electrically.
- Aggregator interface chip, AIC: ASIC that multiplexes several FE upstreams into an output data stream, and de-multiplexes a downstream into 4 FE input streams.
- Active Cable: Data cable constructed from Aggregator chip at the module end, low mass data cables and a connection to a receiver interface chip at the opto-board end.
- Opto-box: Patch panel housing electrical to optical signal functions
- EoSC: End of structure card
- PP0: Patch panel 0
- PP1: Patch panel 1.
- PCB: Printed circuit board
- QC: Quality control
- QA: Quality assurance

3 Related Documents

- ATLAS front-end pixel chip specification document (ATL-COM-ITK-2017-004)
- CMOS sensor specification (ATL-COM-ITK-2017-003)
- Planar Sensor specifications document (ATL-COM-UPGRADE-2017-002)
- 3D sensors specification document (ATL-COM-UPGRADE-2017-001)
- Bump bonding specification document (ATL-COM-UPGRADE-2017-003)
- Electrical service system specification document (?)
- Local support specification document (?)
- Active cable specifications document (still to come)

4 Description of Module

The ATLAS ITk pixel module is the unit made of a bare pixel module and a PCB glued together. The module connections for data, control, LV supplies, cooling etc. are independent of the technology choice (hybrid or CMOS pixel module) with the exception of the HV connection required to bias the silicon sensor in the hybrid pixel modules.

4.1 Module PCB

For both pixel technologies, the module PCB is fabricated either from a flexible polyimide or from thin rigid (e.g FR4) printed circuit board technology with multiple layers and vias as required to realize its functionality. The module PCB is electrically connected to the FE chips

via aluminium wire bonds using ultra-sonic wedge bonding. The module PCB circuit provides:

- Power domain for the FE chips, including the necessary filtering and reference voltages.
- Routing and filtering of the sensor HV bias.
- Connection, distribution and AC coupling of the downlink data signals from the Aggregator interface chip, AIC, to the FE chips. The AC coupling of the uplink data signals from the FE chip(s) to the AIC is done on the receiver side.
- Housing of the NTCs for the DCS and the interlock systems.
- Connection to the external electrical services.

The design goal is for a single PCB design for the quad hybrid pixel modules if the connection to the local supports allows. The module PCB is designed to be of maximum radiation length to minimize the module material in the experiment.

4.2 Hybrid pixel module

The hybrid pixel assembly is constructed from a silicon sensor and the ATLAS Pixel FE chip flip-chip bump-bonded together. Three different varieties of assembly exist, which are propagated to three varieties of modules, namely;

- a single-chip module consisting of a 3D-sensor and 1 FE chip
- a 2-chip (Dual) module consisting of a planar sensor and 2 FE chips
- a 4-chip (Quad) module consisting of a planar sensor and 4 FE chips arranged in a 2x2 array.

It is possible that some 2-chip (or 4-chip) modules fabricated from 3D sensors may be produced if the yield is sufficient and the layout requires them.

4.3 Monolithic pixel module

The monolithic pixel assembly is constructed from a silicon CMOS pixel. The monolithic assemblies can be combined with the module PCB to form different types of modules, e.g.:

- Single chip modules, consisting of only one monolithic pixel chip
- 2-chip (Dual) modules consisting of two monolithic pixel chips
- 4-chip (Quad) modules consisting of three monolithic pixel chips arranged in a 2x2 array.

5 Interfaces

The modules interface to the items listed in Table 1.

Table 1 Interfaces to the ITk pixel module

Name of component	Specification document
Aggregator interface chip.	Active cable specification document.
Stave electrical services type-0.	Electrical service system specification document.
Low voltage system.	Electrical service system specification document.
High voltage system.	Electrical service system

	specification document.
Detector control system.	Electrical service system specification document.
Detector interlock system.	Electrical service system specification document.
Low mass supporting structure.	Local support specification document.
Cooling system.	Local support specification document.

Internally to the module the module PCB additionally interfaces with the front-end chip and sensor or the monolithic pixel chip, respectively.

6 Physical Description

6.1 Components

The following components are combined to form a pixel module

1. Bare pixel module.
2. Populated module PCB.
3. PCB to bare module adhesive.
4. Wire bond encapsulant/potting material.
5. Parylene for HV discharge mitigation (one of two possible options for the hybrid pixel module. The second method is a BCB coating applied to the FE chips at the wafer-level as described in the hybridization specification document).

Additionally, an external pigtail to connect the module to the electrical service cables will be required.

6.2 Bare pixel module

The unpackaged bare pixel module consists of a sensor flip-chip bump bonded to a number of FE chips or a monolithic CMOS pixel chip. The module PCB is glued to the sensor side or to the CMOS pixel side, respectively, of the bare module. The pixel module differs depending upon its final location in the pixel system, with the baseline TDR layout given in Table 2, with open options given in parentheses.

Table 2 Pixel module details.

Module position in system	Sensor type	Module type		Active sensor thickness (μm)	FE chip thickness (μm)
		Barrel axial region/Rings	Barrel Inclined region		
B0, R0	3D	Single	Single	150 + 100 support	150
B1	Planar (3D)	Quad	Quad	100	150
R1	Planar (3D)	Quad		100	150
B2, R2	Planar	Quad	Dual (Quad)	150	150
B3, R3	Planar	Quad	Dual (Quad)	150	150
B4, R4	Planar	Quad	Dual (Quad)	150	150

B4 CMOS	CMOS	Quad	Dual (Quad)	< 200

The details of the sensors are given in the sensor specification documents. The separation of the FE chip and sensor after flip-chip bonding is defined in the bump bonding specification document to be between 5 and 35 micrometers.

The FE chip consists of pixels of size 50 μm x 50 μm arranged as 400 columns and 384 rows, resulting in an active pixel matrix of 20 mm x 19.2 mm. The additional logic area at the bottom of the chip and wire bond pads are in the EoCL area of the FE chip. The EoCL and the crack stop and dicing street around the perimeter of the chip define the chip's final size.

The chip width is between 20.046 mm and 20.126 mm. The minimum size is the outside of the chip seal ring to outside of seal ring based on the RD53A chip, while the larger dimension assumes a dicing street of 80 μm and a blade of zero width. The height of the chip is between 20.996 mm and 21.176 mm assuming exactly the same EoCL area as the RD53A chip and the same considerations as the chip width, with an additional 0.1 mm added to the EoCL area to account for possible design requirements.

The estimate of the final physical chip size is therefore 20.086 ± 0.04 mm x 21.086 ± 0.09 mm.

For multi-chip modules, the FE chip separation is limited by the position of the dicing edge relative to the edge pixel bump bond pad and the chip separation required by the flip-chip vendor, which must be around 100 μm. The separation should be minimized to reduce the pixel implant size in the edge region to improve module performance. A FE chip edge-pixel to edge-pixel spacing along the row of 250 μm is considered reasonable as defined in the sensor specification. This results in a physical chip-to-chip spacing between 124 μm and 204 μm. At the top of the chip the distance from the edge pixel to chip edge is larger, the FE chip edge-pixel to edge-pixel spacing along the column of 250 μm results in a physical chip-to-chip spacing of 134 μm.

The EoCL area of the FE chip extends beyond the sensor to allow interconnect to the module PCB. The sensor extends beyond the FE chip in the direction of the rows due to the sensor guard ring structure. The sensor size is defined in the sensor specification document and assumes 250 μm spacing between edge-pixels of neighbouring FE chips.

The CMOS quad module does not cover the space between physical cut edges with an active sensor, unlike the hybrid pixel module. This increases the requirement to dice the chip as close to the chip crack stop as possible and to place individual chips in the module as close together as possible. The CMOS chip will have an inactive chip edge of no more than 200 μm on buttable chip sides and a chip-to-chip spacing in the module of no more than 150 μm.

The module drawings are given at **AT2-IP-EP-0009** for hybrid modules.

6.3 Populated module PCB

The detailed design of the hybrid could differ depending upon module type (1-, 2-, 4-chip) and could differ depending on the intended module location (e.g. axial barrel, inclined barrel, inner endcap, outer endcap). However, the specification of the module PCB is universal.

The module PCB provides the electrically connectivity to the module. The pixel module will have the electrical connections to the external system shown in Figure 1. The CMOS module may not have an external HV connection as this may be generated internally from the LV line. Internal to the module, the module PCB connects the HV bias to the sensor's backside in case of the hybrid pixel modules and all the electrical connections to the FE chip, see FE chip and CMOS chip specifications for details.

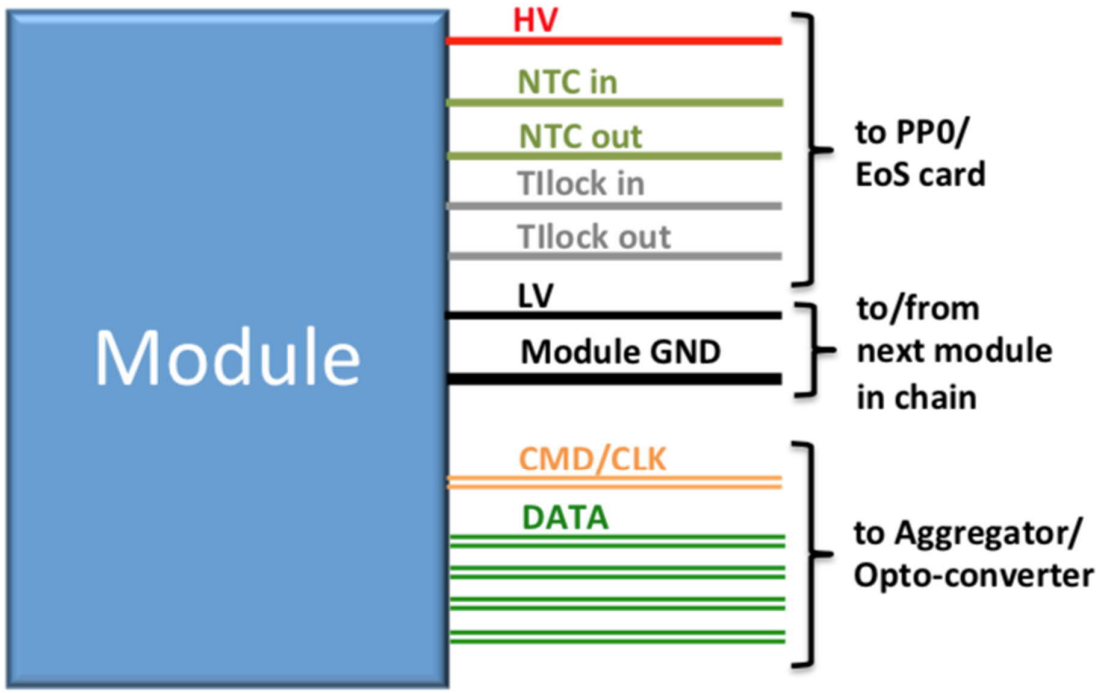

Figure 1 Electrical connection of a module.

The module PCB will be designed according to "IPC-2223A Class A Flex-to-Install" flexible circuit industry standards and specifications. The PCB made from several layers of polyimide dielectrics and/or thin rigid PCB material and copper layers. The mass of the copper layers is kept to the minimum required to perform their function so as to maximize the module radiation length.

The top solder mask, required for the soldering of components, is required to be flexible, the Green Flexible Soldermask EFP140 or equivalent is used. Where an adhesive layer is required Espanex (modified polyamide) adhesive will be used rather than an acrylic glue. The required radiation hardness will be demonstrated for both materials.

The backside of the PCB is covered with a cover layer (polyimide with 25um adhesive is preferred) to electrically isolate the circuit from the HV of the sensor for a sensor operational voltage $V_{SensorMaxOpp}$. The PCB will be tested to twice the maximum operational sensor bias ($V_{SensorMaxOpp}$) before attachment to the bare pixel module, see section 9.8.

The module PCB will support the necessary surface mount components to facilitate its electrical functionality. The surface mount resistors for the shunt circuit should be of

precision of 0.1% or better. The PCB will have pads for wire bonding along its edge to allow electrical interconnect to the FE chip. The position of the wire bond pads will be such to maximize the wire bond yield of the module. The solder and wire bond pads on the module PCB are plated using either Electro-less Nickel/Immersion Gold (ENIG) or Electro-less Nickel Electro-less palladium Immersion gold (ENEPIG). The Electro-less nickel thickness shall be 3 µm to 6 µm and the minimum immersion gold thickness shall be 0.05 µm detailed in IPC-4552 Specification for Electro-less Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards. The wire bond pads must be compatible with ultra-sonic Aluminium wedge wire bonding and sized for 25 µm diameter wire and will be no smaller than 100 µm x 200 µm. The final pad layout and assignment depends on the final FE chip design and will be given in a later document. Two additional wire bonds pads are present next to each FE chip wire bond pad array for sacrificial wire bond pull tests.

Fiducial marks are present on the module PCB to aid with the assembly process. At least two fiducial marks must be present in the vicinity of each FE chip wire bond pad array.

The PCB must have areas on its surface that are clear of surface mount components and wire bonds to allow module mounting onto the local supports, without degrading the performance of the module. The size and placement of the keep-clear areas will be defined in collaboration with the module mounting activity.

The PCB may be delivered surrounded by a frame for handling. The frame provides accurate fiducials and dowel holes for module construction and stiffness to hold the PCB flat. The frame is either the same build as the body of the PCB or has an addition FR4 laminated on the backside for additional mechanical support.

A single downlink data line is connected to the module and the signal is routed in parallel to each chip in the module. The clock and command signals are extracted from this data by the frontend chip. The uplink data streams from the frontend chip are routed from the chip to the AIC where they are multiplexed together into a number of high speed electrical data cables, which runs all the way to the Opto-box beyond PP1. The data signals to and from the module to the AIC are transmitted on differential pairs via either a (shielded) low mass twisted pair, Twinax cable or a flex tape which are connected to the module PCB via either a connector, with glue and wire bonds or solder connection. The shields are AC coupled to the module PCB's local ground reference. DC connection is prohibited as it will short-circuit the serial power chain. The signal lines are AC coupled to the data cables using discreet components mounted on the module PCB.

For multi-chip modules, the front-chip chips are connected in parallel for powering from a common low voltage input on the module PCB. The module PCB is connected to the type-0 cable to supply the electrical services (the LV, HV and NTC connections). The electrical connections of the module to the services must be done in such a way as not to constrain the module such that the difference in CTE of the service cable and the support structure causes stress on the module. Additionally, the connection must be compatible with the module to stave loading procedure. The electrical connection may be done via a connector, solder or wire bonds. Whichever method is chosen, the connection must fulfil the electrical specifications for the given interface.

The hybrid pixel module will be mounted onto the mechanical support structure via the backside of the front-end chips. This interface is part of the thermal path of the module to the cooling fluid. The attachment method is defined by the module to local supports mounting specification. The attachment method must hold the module in place for the full temperature range the system will experience throughout the lifetime of the experiment. It must do this without causing the silicon sensor to degrade due to excessive stress on the module due to CTE mismatch between the module and the local support structure. As stresses are proportional to the adhesive induced coupling, the glue interfaces should be compliant. The operational temperature range is defined in the local supports' specification as 60C to -55C.

7 Manufacturers

Only ITk Pixel institutes which have passed a qualification procedure will be able to perform module PCB and bare module reception tests, module build and module QC testing.

The module PCBs will be manufactured and populated with passive components in industry according to relevant IPC standards.

The bare pixel modules will be provided by the flip-chip suppliers to the module assembly institutes. The institutes will perform a number of reception tests on the pixel modules and module PCBs in addition to those performed by the vendor to guarantee quality, for example the PCB vendor may not be able to perform a QC HV isolation test to the required potential, detailed in section 9. The module PCB will be fabricated on panels containing a number of circuits and test coupons that are used for QC and QA test. These coupons come with test features that allow the assessment of the circuit performance and fabrication process, for example through-hole via reliability and high-speed signal transmission performance, see sections 9 and 11.

Initial inspection of the bare module will be performed at the ITk Pixel institutes followed by the module PCB to bare module attach process and wire-bonding. The module PCB maybe cleaned and dried before wire bonding to guarantee wirebond pull strength.

The FE chip is an electrostatic sensitive device and must be handled properly to avoid damage from electrostatic discharge (ESD). The international standard IEC 60747-1, chapter IX must be followed. The working environment, including tools, materials and containers for handling and transport of modules should provide for ESD protection (refer to IEC 61340-5-1 and IEC 61340-5-2). All operators dealing with the items must be grounded to same potential as the equipment with at least the use of grounding wrist straps. To avoid damage from particulates bare modules, module PCBs and assembled modules must always be handled in a clean room environment of at least class 10000 (lSO 7), or better, using properly designed tools and materials to prevent touching with bare hands and applying excessive pressure. Use of special tweezers or ESD dedicated vacuum pick up tools for picking up the parts are required. If modules are to be transported between cleanrooms, a suitable carrier should be used and the container should remain closed during transportation. The container should be externally cleaned on re-entering the cleanroom. At all times, bare modules, module PCBs and assembled modules should be stored in clean containers in a controlled inert (dry air or nitrogen) environment, with temperature: 18 C to 24C, RH between 7% and 30%, and particle count: ISO Class 7.

The institutes will perform a range of QC and QA tests on the assembled module before shipping to the module to local-support loading sites. Shipping containers will have to maintain module cleanliness, ESD protection as well as reduce and measure mechanical shock. The institutes that will perform the module construction and QC and QA tests are still to be defined.

8 Power

The power of the module is a combination of the sensor power, frontend chip power and power dissipated over the module PCB. The module LV is powered by a constant current source with modules arranged in a serial power chain. The FE-chips of a given module will be powered in parallel supplied by a single supply line. The power requirements for the module are dominated by those of the FE chips. The powering requirements are reproduced from the individual specification documents in Table 3.

Table 3 Module power

Name	**Max/Nom/Min V supplied**	**Max/Nom I for Voltage Source**	**Max/Min I for Current Source**	**Other Requirements**
Quad module LV	1.54V/1.4V/tbd	--	8A/5.6A (currently being reconsidered based on RD53A results)	floating PS
Planar sensor HV	800V/depends on irradiation level/-	6mA / < 105 μA/cm^2	--	floating PS
3D sensor HV	250V/ < 10 V (unirr.)	40 μA/cm^2 / < 2.5 μA/cm^2	--	floating PS
CMOS quad				
Module PCB traces LV			8A/5.6A (currently being reconsidered based on RD53A results)	Power dissipation kept to less than 10% of module power for type-0 and module PCB.

8.1 Input/Output

The input and output signals to the module are given in Table 4. The Electrical service system specification document specifies the modules' integration into the electrical system, a summary is provided here for completeness. The module will have LV power supplied via a serial power chain and as such will interface with the pixel serial power protection (PSPP) chip, mounted on the power bus before the connection to the module. The PSPP chip allows the LV connection to the module to be by-passed in case of module failure, including failure of the power bus to module connection. The sensor HV will be supplied in a parallel configuration via a single HV line to all modules in the LV serial power chain. The HV return function will be provided by the LV return cable. The module will have two NTCs; one for the DCS system to measure the temperature of the module, and the second for the interlock system, not all module interlock NTCs will be connected to the interlock system. All DCS NTCs will be connected to the DCS system.

Table 4 Module Input and Output signals

Name	**In, Out or I/O**	**Type**	**Description**	**Specification**	**Number of channels per module**
HV	In	Power	800V HV input, Power of 6.25W, current of 8mA	DC resistance of <100mOhm Tested to 1600V.	1 HV in.
LV In	In	Power	Serial power bus connection capable of supplying 2 V and 12 A.	DC resistance of <10mOhm, 12A total current carrying capability	1 LV in.
LV return (Module local GND)	Out	Power	Serial power bus connection capable of supplying 2 V and 12 A.	DC resistance of <10mOhm, 12A total current carrying capability	1 LV out.
NTC (NTC)	Out	Analogue	1 NTC connection to the DCS chip on the service cable		NTC in and out.
Interlock (Tilock)	Out	Analogue	1 NTC connection direct to interlock not via DCS system		NTC in and out.
Downlink data (CLK/CMD)	In	DC-balanced, JEDEC SLVS	160 Mb/s combined CLK and CMD (shielded) differential pair	100Ohm differential impedance. Less than 2 dB loss across the PCB at 0.75 GHz.	1 shielded differential pair to the module. Signal distributed to each chip in the module.
Uplink data (Data)	Out	Differential output: CML / SVLS	Up to 4 lanes of 1.28 Gb/s (shielded) differential pair per chip, see text.	100Ohm differential impedance. Less than 2 dB loss across the PCB at 0.75 GHz.	1/2/4 shielded differential pair(s) depending on position in the system, see text.

The downlink and uplink connections will be provided via shield data cables. The downlink is a single differential pair connection to the module with the signals distributed to each chip. The bandwidth for this link will be 160 Mb/s being sent out from the AIC via an e-link. Clock and data information is encoded in this signal and decoded by the FE-chip. The number of uplink connections from the module is dependent on the position of the module in

the system, which is summarized in Table 5 and Table 6 for a 1MHz trigger and the L1Track trigger with a 4MHz L0 readout rate, respectively. The modules in the inner layer do not increase the data rate for the L1Track trigger but utilize a fast-clear function (see FE chip specifications).

The data rates presented are based on RD53A data format and a 70% link occupancy. The number of FE chips per link and the data rate per link depend on the active cables and FE design, which are currently under discussion. For the 4MHz L0 readout rate, all chips have 1 or 2 data links per chip except for L0/R0 and L2/R2 which have 3-4 outputs/chip. However, R2 is likely to reduce with the new chip data format. The data tab only needs to route 1 or 2 outputs/chip, 8 differential pairs maximum for the majority of the modules. For R0/L0 and L2/R2 the data tab needs to route 4 or 3 outputs/chip.

Table 5 Module type and Uplink connections in the ITk pixel system for 1MHz L0 trigger

Layer	Baseline 1MHz L0			
Flat	1MHz Data rate/chip Gbps/chip	Number output lines/chip	Number of FE/link	Data rate per link, Gbps
0	3.56	4.00	1	3.56
1	0.54	1.00	4	2.16
2	0.38	1.00	4	1.52
3	0.28	1.00	4	1.12
4	0.22	1.00	4	0.88
Inclined				
0	3.94	5.00	0.8	3.94
1	0.89	1.00	4	3.56
2	0.50	1.00	4	2.00
3	0.32	1.00	4	1.28
4	0.22	1.00	4	0.88
Ring				
0	2.14	3.00	1	2.14
1	1.07	2.00	2	2.14
2	0.65	1.00	4	2.60
3	0.39	1.00	4	1.56
4	0.27	1.00	4	1.08

Table 6 Module type and Uplink connections in the ITk pixel system for 1MHz L0 trigger

Layer	Backup 4MHz L0				
Flat	Trigger rate MHz	Data rate/chip, Gbps/chip	Number o/p lines/chip	Number of FE/link	Data rate per link, Gbps
0	1	3.56	4.00	1	3.56

1	1	0.54	1.00	4	2.16
2	4	1.52	2.00	2	3.04
3	4	1.12	2.00	2	2.24
4	4	0.88	1.00	4	3.52
Inclined					
0	1	3.94	5.00	0.8	3.97
1	1	0.89	1.00	4	3.56
2	4	2.00	3.00	1	2.00
3	4	1.28	2.00	2	2.56
4	4	0.88	1.00	4	3.52
Ring					
0	1	2.14	3.00	1	2.14
1	1	1.07	2.00	2	2.14
2	4	2.6	3.00	1	2.60
3	4	1.56	2.00	2	3.12
4	4	1.08	2.00	2	2.16

9 Detailed functional description and specification

9.1 Signal transmission on module PCB

The module has a number of 1.28 Gbps differential pair high speed data outputs, see Table 5 and Table 6, which go directly from the FE chip to the AIC. The differential output impedance of the FE chip is 100 Ohm. The differential impedance of the transmission lines on the module PCB is 100 Ohm ± 10%, which must be verified on test coupons during manufacture, if not every module PCB. The attenuation of the chain from FE chip to AIC must be less than 5 dB with less than 2 dB on the module PCB measured at 0.75 GHz. The signal transmission on the module PCB and via the connector must have a cross-talk (S14) attenuation of more than 30 dB.

The input signal to the module is a 100 Ohm differential pair running at 160 Mbps. While the attenuation of the downlink is less critical than the uplink the same specification for the attenuation and cross-talk for the downline transmission and connector as for the uplink line applies.

The downlink lines are AC coupled on the module flex to allow for serial powering of the module. The uplink data lines are AC coupled at the receiver.

9.2 LV voltage drops

The power dissipation on the module PCB is defined in Table 3. The voltage drop on the PCB must be low enough to meet this. The LV lines on the flex must be positioned sufficiently far from the NTC as to not affect the temperature of the NTC by more than 0.1C during end of life operational conditions.

9.3 PCB to bare module attachment

The module PCB is attached to the sensor side of the assembly with an adhesive of thickness of 75 µm. The precision of the PCB alignment to the bare pixel assembly is ±50 µm in X and ±50 µm in Y and ±25 µm in Z. The X and Y alignment accuracy is to ease module wire bonding. The adhesive must be present under the module PCB wire bond pads to guarantee the ability to wirebond the PCB. The adhesive must not spread beyond the edge of the PCB such that it reaches the edge of the sensor or cover the wire bond pads of the FE chip. The adhesive must be present under the NTCs to guarantee a good thermal connection between the NTC and the sensor. The adhesive must not obscure the wirebond HV connection from the PCB to the backside of the sensor. The module will be thermally cycled from 60C to -55C (see test section below) and the adhesive must have a peel strength above 1.5 N after thermal cycling.

The forces in the module due to the module PCB and module PCB to bare module attachment method during thermal cycles must be such that no increase in disconnected bump bonds are observed and that the sensor IV does not change by more than 0.1% after 100 cycles from -55C to +60C, see section 11 for test protocol.

9.4 Wirebond

The FE to module PCB electrical connection is realised with ultra-sonic wedge wire bonding using 25 µm diameter Aluminium wire. The current carrying load of the wire bonds must not exceed 50 mA per bond, which is approximately 5 times lower than the fuse current. Where higher current is required multiple bonds must be used.

There are three possible failure modes for the wire bonds;

1. unintentionally placed weak bonds
2. damage from Lorentz force induced oscillations in the experiment
3. ionic corrosion due to chlorine contamination on the module PCB, aggravated in a high RH environment.

To assure against the first failure mode, the wire bond pull tests are performed as per METHOD 2011.7 of MIL-STD-883E. A pull strength greater than 5g for all bonds with an average of 8g and a standard deviation of < 15% is required. The pull strength must be met after thermal cycling the module according to IPC document -IPC-TM-650 -2.6.6, which is confirmed with QA testing on a test coupon and on sacrificial bonds on 1% of module PCBs produced. The module PCB will allow for an additional pair sacrificial wire bonds per chip for post aging testing of the module during module QC testing.

The second failure mode is negated by the use of a contact current source and the shunt circuit in the FE chip.

To protect the wire bonds from corrosion they must be coated or potted. The technique chosen must demonstrate protection from corrosion when a droplet of D.I. water is intentionally placed on the wire bond pads. The protection technique must not degrade the electrical or thermal performance of the pixel module and must be robust against CTE mismatch induced by a module thermal cycle over the operational temperature range at end of life radiation dose. This will be tested on a module PCB per batch.

9.5 Envelope

The module envelope is dominated by the HV capacitor used on the module which will be either a high reliability capacitor rated to $V_{SensorMaxOpp}$ or a commercial capacitor rated to 2 x $V_{SensorMaxOpp}$; for example, the Kermet High Voltage with Flexible Termination System (HV FT-CAP) which for a 1 nF device is available in a 1210 package of 1.2 mm height. The

HV capacitor will be potted with a glob top for HV protection, adding another 0.5 mm in height. The potential use of a ZIF type connector for interconnection of both power and data would require the same order of magnitude as the HV capacitor.

9.6 Bow

To guarantee that the module attachment to the local support is as required (thermally and mechanically) the bow of the module must be less than 25 μm at room temperature after assembly and thermal cycling tests.

9.7 Sensor IV

After flip-chip, the sensor leakage current must not increase by more than a factor of 2 from that measured at sensor reception. The absolute sensor leakage current, measured at 20C and RH<50%, must be, for planar sensors less than 1.5 $\mu A/cm^2$, (measured at V_depl + 50V), and for 3D sensors less than 5.0 $\mu A/cm^2$, (measured at V_depl + 20V). The breakdown voltage must also remain high and must not change by more than 10V and 5V for planar and 3D sensors respectively, compared to that measured during the reception tests. The absolute breakdown voltage must be, for planar sensors greater than V_depl + 80V, and for 3D sensors greater than V_depl + 40V.

9.8 HV Operation

The module PCB will be designed for HV conductor spacing as per IPC 2221A (General Standards on Printed Board design). For HV conductor separation determination, the HV traces will be considered as an external conductor coated with a permanent polymer as described in IPC2221A. The design value for the HV is the maximum operational sensor bias ($V_{SensorMaxOpp}$) defined in the sensor specification.

The HV trace connection to the sensor backside will be via multiple wire bonds through a hole cut in the module PCB. The HV trace will be filtered on the module PCB just before connection to the sensor with a filter consisting of a nano-Farad capacitor and a KOhm resistor. The HV filter surface mount capacitor will be either a “High Reliability Capacitor” having met the MIL-PRF-49467 specification rated to the maximum operational sensor bias or a standard component rated to twice the maximum operational sensor bias. The HV capacitor chosen will be sample tested with each lot qualified by testing 5% or 200 units (whichever is the lesser number) with no failures. Test conditions are $100^{O}C$ with a test voltage applied for 1 hour with a measured leakage current < 10 nA on all tested parts. The test voltage should be 1.5 x $V_{SensorMaxOpp}$ if “High Reliability Capacitors” are chosen and 2 x $V_{SensorMaxOpp}$ for all other HV capacitors.

All HV connections on the module PCB (including the HV filter capacitor) will be potted for HV isolation.

The module PCB will be tested to twice the maximum operational sensor bias ($V_{SensorMaxOpp}$) before attachment to the bare pixel assembly. The high voltage leakage current after a dwell time of 30 minutes at $V_{SensorMaxOpp}$, at a temperature of 20C, and 50% or higher relative humidity, should not exceed 50nA. The test requires the module PCB to be mounted on a metal vacuum jig in electrical contact with the back of the PCB and isolated from its surroundings. HV will be applied via the PCB connector/connections pads and the vacuum jig, to represent the sensor back plane of the final pixel module, and all other pins/pads in the PCB connector will be held at HV return.

The module must be protected against sensor high voltage discharge to 1.5 x $V_{SensorMaxOpp}$. High voltage discharge occurs when the sensor is at a voltage of more than 500 V, due to the high potential difference between the perimeter of the sensor and the FE chip in the area where they overlap. Two possible protection methods are allowed. The first is the use of a BCB coating on the sensor or FE chip. The second method is a conformal Parylene coating over the module. A Parylene coating of at least 3 μm is required. To guarantee adequate cooling of the module the backside of the module will have no coating that increases the thermal figure of merit by more than 0.5 $KW^{-1}cm^2$. This is equal to 4.2 μm of Parylene-C (thermal conductivity of 0.084 $Wm^{-1}K^{-1}$).

After the module is assembled, the module will be tested to the same maximum voltage used for the sensor QC steps. The sensor leakage current of the module is described in the section 9.7. A sub-set of the modules (0.2% of the modules made) will be irradiated to the maximum design fluence and tested to the maximum operational sensor voltage. The sensor breakdown voltage must exceed that stated in the section 9.7.

The module local ground must be isolated from the support structure so as not to short the serial power bus. The module HV must be isolated from the support structure so as not to compromise the sensor HV performance. This may be performed on the stave, via Parylene coating of the module or another coating method.

9.9 Digital operation

The digital functionality of all the FE chips (register tests, dead pixels from digital injection tests) should be no worse than those measured on wafer. The exception is that an increase in dead pixels by 5 pixels/chip is allowed.

9.10 Analogue operation

The noise performance and minimum threshold of the assembled module must be the same, to within 5%, of a bare module mounted onto a test PCB.

9.11 Bump bond yield

The number of disconnected bumps, as deduced from the difference in the pixel noise measured with threshold scans with the sensor bias on and off, after the full module QC testing cycle should match that recorded for the bare assembly test data within a maximum of 10 bumps per chip. The number of merged bumps detected from a threshold scan should match the X-ray data within 10 bumps per chip, as discussed in the hybridization specification document.

The final specification on the maximum number of bond failures for a given chip is 600 with the maximum size of continuous group of failed bonds equal to 50. This is a bump failure rate of $4x10^{-3}$ bumps per chip.

10 Radiation Tolerance

The modules must be able to electrically and mechanically function up to an ionising dose and a NIEL fluence as defined in the sensor specification documents. The passive components must be radiation hard, certified by the manufacturers or confirmed in extensive test by the ITk institutes. The adhesive used to attach the module PCB to the bare module, the wirebond protection material, HV capacitor glob-top and the method and materials used to guarantee HV operation of the sensor must be proven to be radiation hard by the Pixel ITk institutes.

All sensors, FE and CMOS chips will be radiation tolerant up to the expected dose.

11 Testing, Validation and Commissioning

The module PCB will be tested in industry for cleanliness (confirmed via QC tests according to IPC- CH-65A, and QA via IPC-TM-650 -2.6.14.1), electrical functionality (net list, opens and shorts), geometric tolerances, over and under etch of traces via cross-sectioning or visual inspection.

The production process and associate tests are given below. The tests include: reception test of the parts, tests on the devices as they are built and after a degree of stress and tests to destruction on a small sub-set of parts. The tests will be reviewed after pre-production and some maybe removed, in particular, the bare module reception sensor IV test which requires specialized equipment. Test data will be uploaded to the ITk production database.

The process performed at the ITk pixel institutes are:

1. Bare module acceptance tests
    a. Visual inspection
    b. Metrology, to check the critical dimensions of the bare module
    c. Sensor IV
    d. Weighting of bare module
2. Module PCB acceptance tests
    a. Visual inspection of all components, to include confirmation that the wire bond pads are clean and free from any deposit that can affect the wire bonding, check for any shorts on the PCB especially in the connector area and checks for solder mask pealing, ENIG/ENEPIG damage.
    b. Metrology, to check the critical dimensions of the PCB and flatness
    c. HV stand-off of module PCB, if not performed in industry
    d. Data transmission tests on PCB test tokens. Test tokens will be manufactured at the same time as the module PCB to allow a measure of signal integrity with a network analysis, or equivalent, to confirm transmission and cross-talk specifications.
    e. Weighing of the module PCB
    f. Wire bond pull tests on test tokens produced on the same panel as the module PCBs.
3. Module PCB to bare assembly adhesive attach
    a. Followed by visual inspection to confirm no gross defects.
    b. Metrology to confirm build process using a non-contact measurement system. This test will be reviewed after pre-production and may be replaced with a simple visual inspection for all modules and a detailed measurement at a 1% level.
    c. Weighing of the assembled module
4. Load onto module carrier
    The module will be placed on a module carrier for wire bond and further assembly and test.
5. Wire bonding
    a. Followed by visual inspection
    b. Wirebond pull tests. Sacrificial wire bond pads will be present on each module PCB.
    c. Sensor IV at 20C and RH <50%.
    d. Initial basic module functionality test to confirm basic electrical functionality.
6. Wire bond protection (which might take place in industry)

7. HV discharge protection with Parylene, if this is the chose method. Most likely this will take place in industry.
8. Initial Quality control tests on all modules
    a. Visual inspection
    b. Sensor IV at 20C and RH <50%.
    c. Initial basic module functionality test to confirm basic electrical functionality.
    d. Chip electrical tune and functionality test at 20C measured on the module NTC, including electrical tests of bump quality.
    e. Operational temperature chip electrical tune and functionality test. The operational temperature is about -25C measured on the module NTC, as defined in the local supports' specification.
9. Long term testing of modules
    a. Thermal cycles of 100 cycles between a temperature of 60C and -55C measured on the module NTC. The module does not need to be powered during the cycles.
10. Final module tests
    a. Final Sensor IV test measured at 20C and operational temperature
    b. Final chip tunes and tests at 20C
    c. Chip tune and test at 40C on the NTC. This test is required to allow warm system level tests during commissioning.
    d. Final chip tunes and tests at operational temperature measured on the module NTC.
    e. Source test for bump bond quality measured with at least 50 hits per pixel.
    f. Visual inspection and packaging before loading or shipping.
11. Quality control on sub-set of module PCBs.
    a. Thermal shock on PCB test token with daisy chain of vias. The coupon with have multiple vias and long traces and will be built in the same panel as the module PCB. This coupon is designed to understand the effect of thermal cycling on via geometry, via to trace build quality including inter trace resistance.
    b. Wire bond pads will be included to allow testing of the wire bond pull strength after rapid thermal cycles.
12. Quality assurance tests on a subset of modules.
    a. Thermal shock test
    b. HASS/HALT
    c. Radiation testing

Quality assurance tests such as thermal shock tests, HALT and HASS tests as well as radiation tests are performed only on a sample of items to control the quality between batches or different assembly sites. The number and size of samples will be adjusted in order to capture any changes in the production process while minimizing the work load. A sample rate of about 1 in 500 modules is expected, resulting in about 30 modules being tested to destruction.

The acceptance criteria for a module after thermal cycling are:

- Ratio of leakage current at operating voltage w.r.t sensor acceptance test: < 2
- Change of the breakdown voltage Vbk w.r.t. sensor acceptance test during each individual assembly process step: < 10V

- Leakage current for planar sensors < 1.5 μA/cm2 measurement at 20°C and at Vdepl + 50V (with a stability in time better than 20% when measured over 48h).
- Breakdown voltage for planer sensors Vbk > Vdepl + 80V.
- Leakage current for 3D sensors < 5μA/cm2, measurement at 20°C and at Vdepl + 20V.
- Breakdown voltage for 3D sensors Vbk > Vdepl + 20V.
- Number of failing ICs per module after assembly: 0
- Number of individual bump failures per single chip module: < 600
- Number of total individual bump failures per 2-chip module: < 1200
- Number of total individual bump failures per 4-chip module: < 2400
- Number of individual bump failures per IC which are grouped in a cluster: < 50