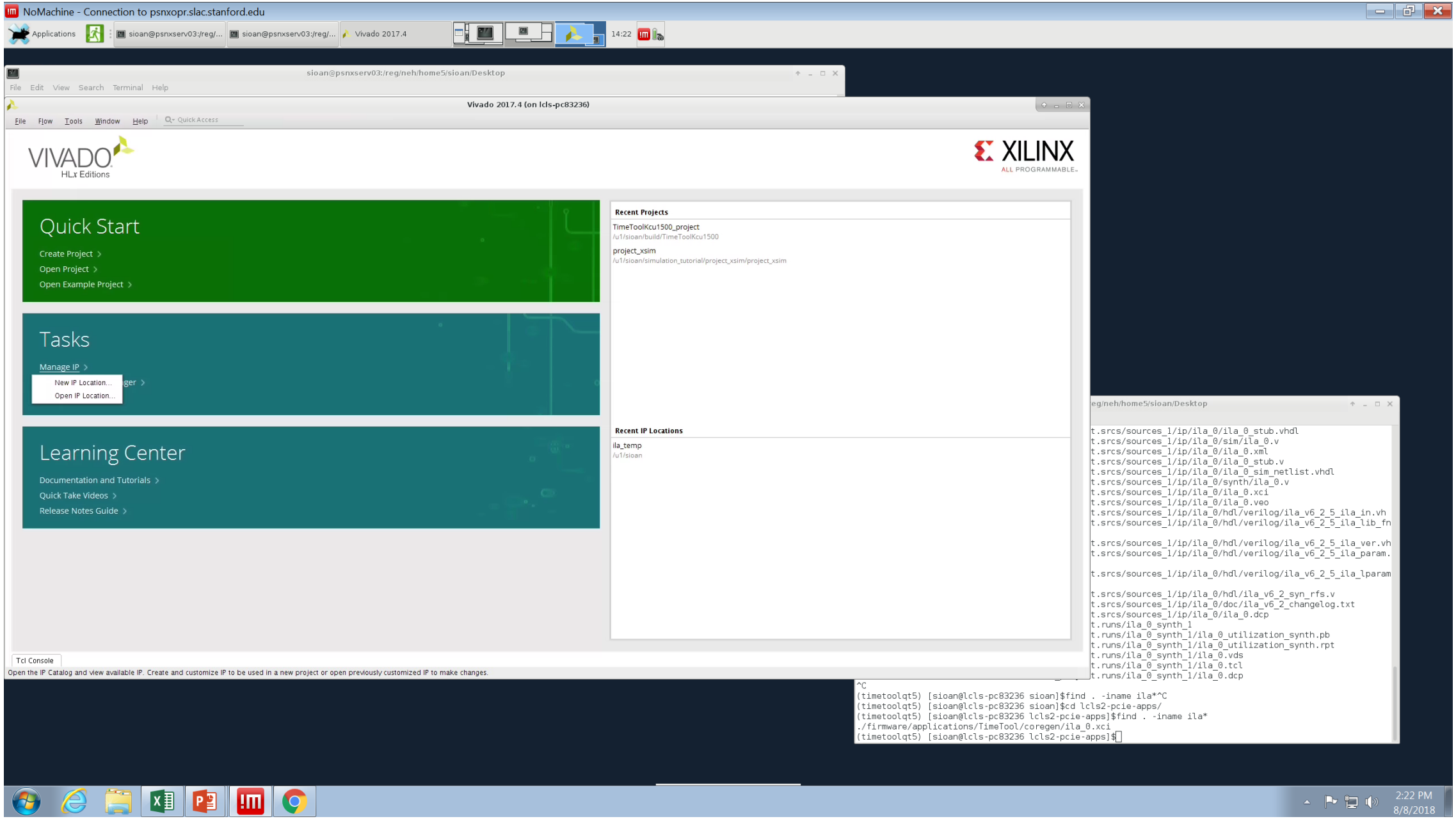
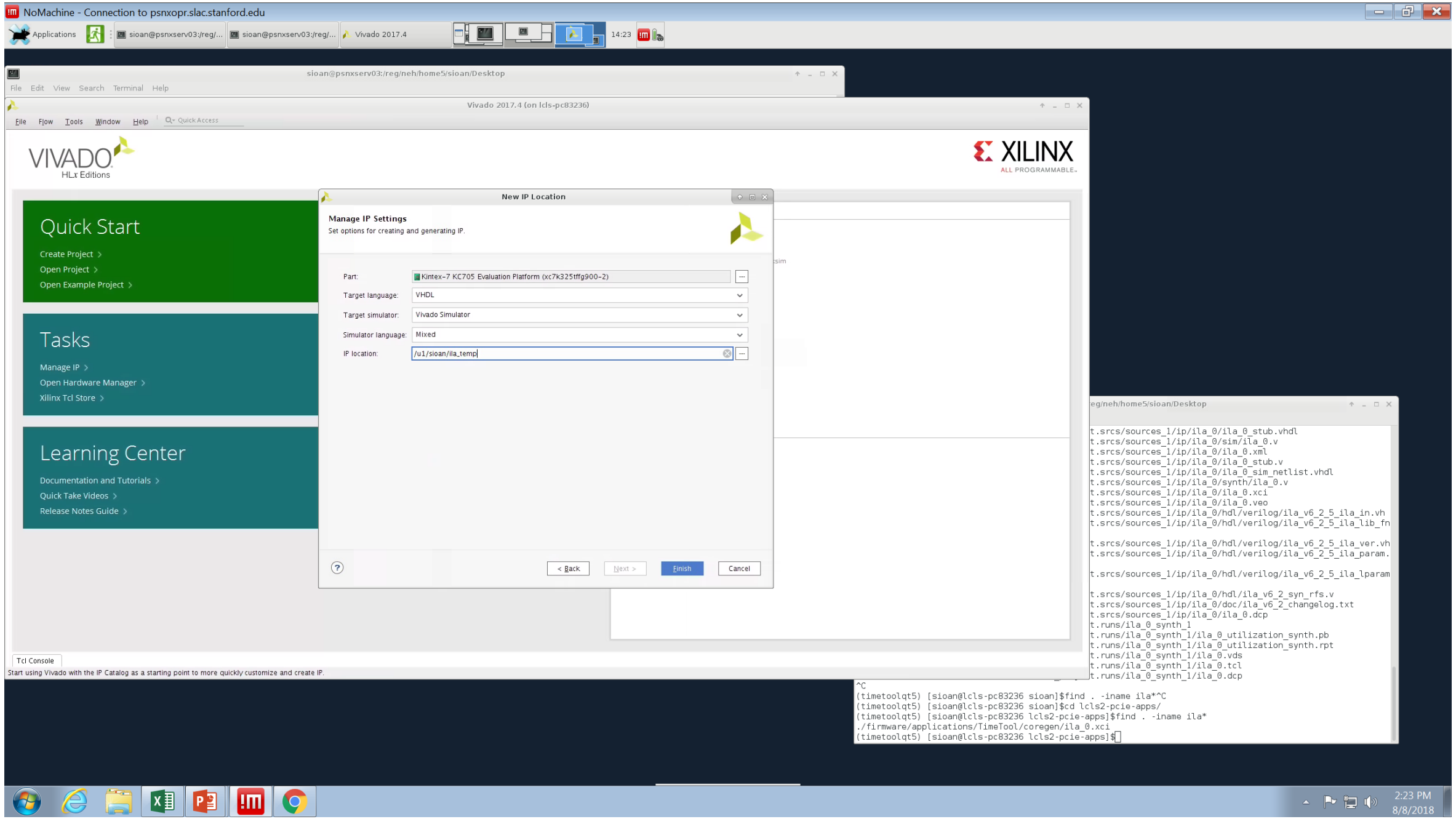
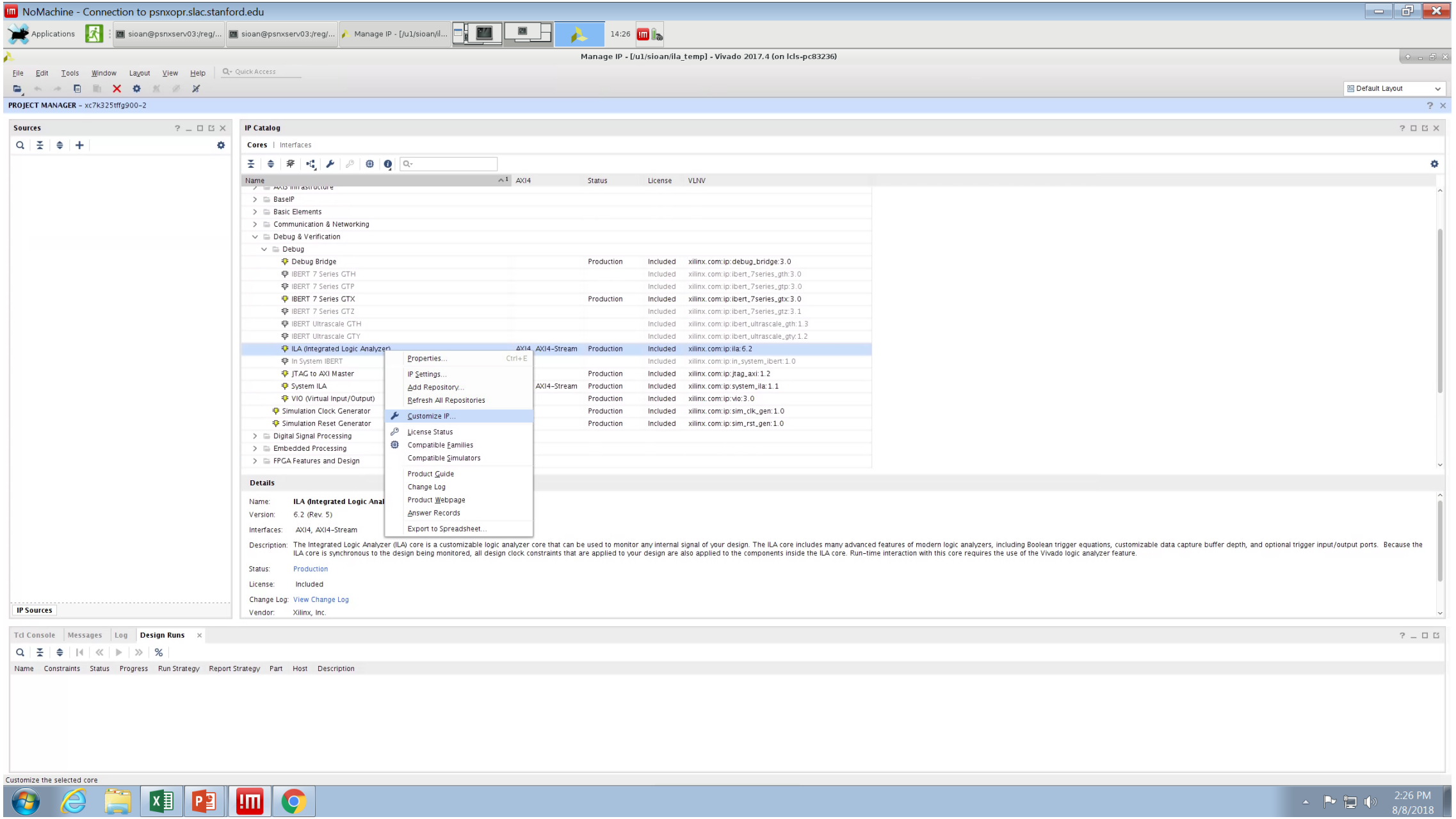
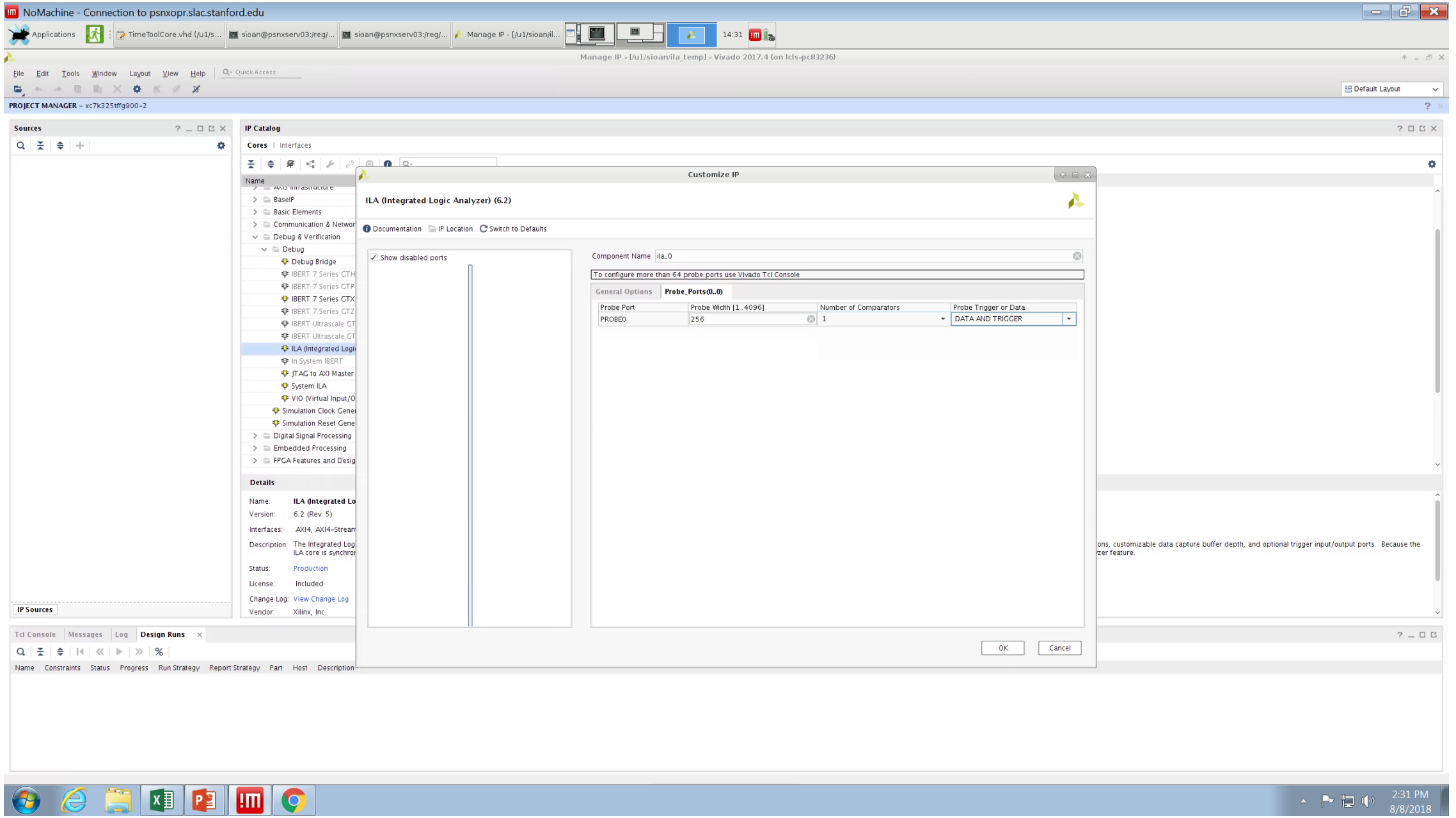
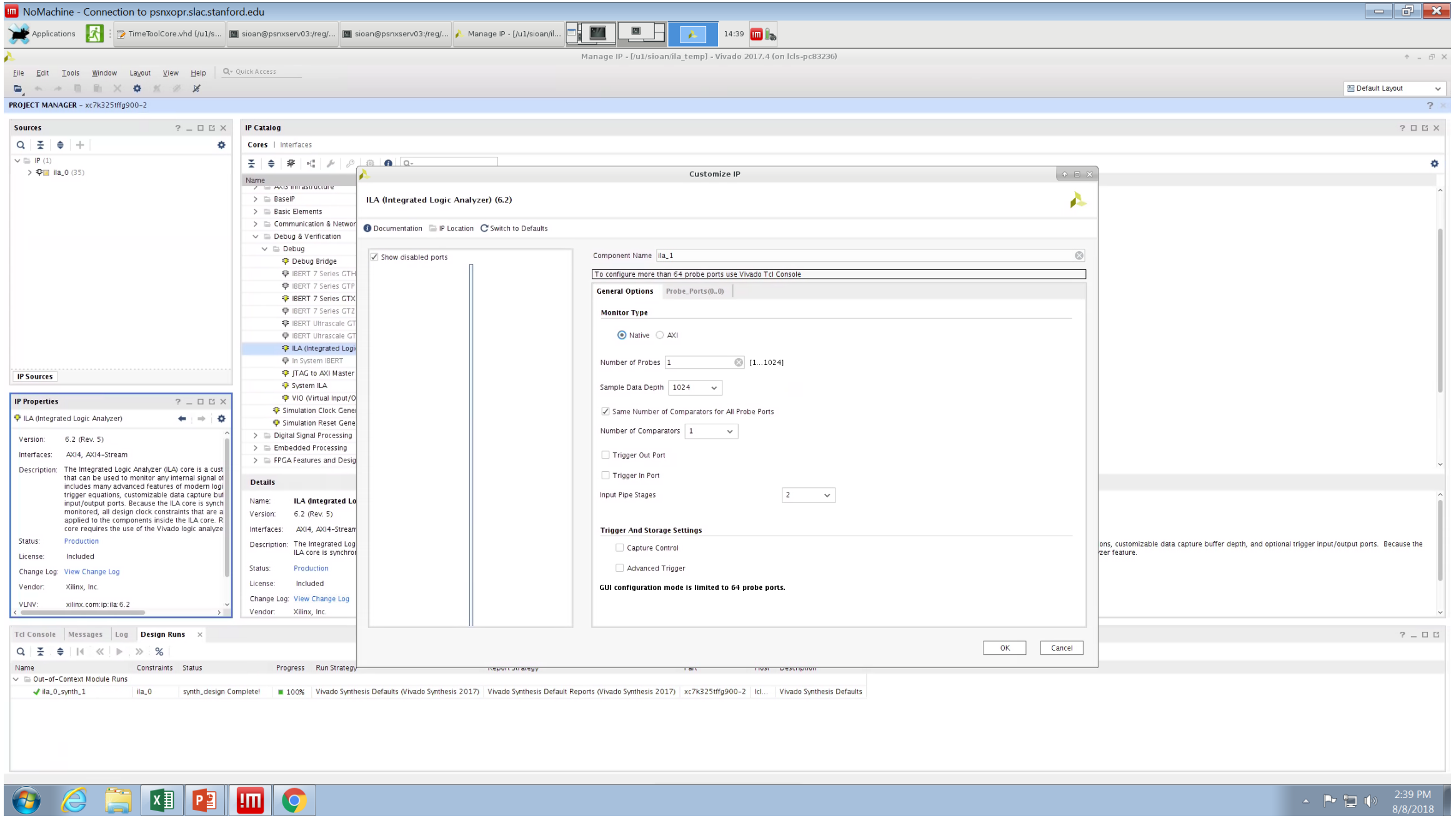
lla step through

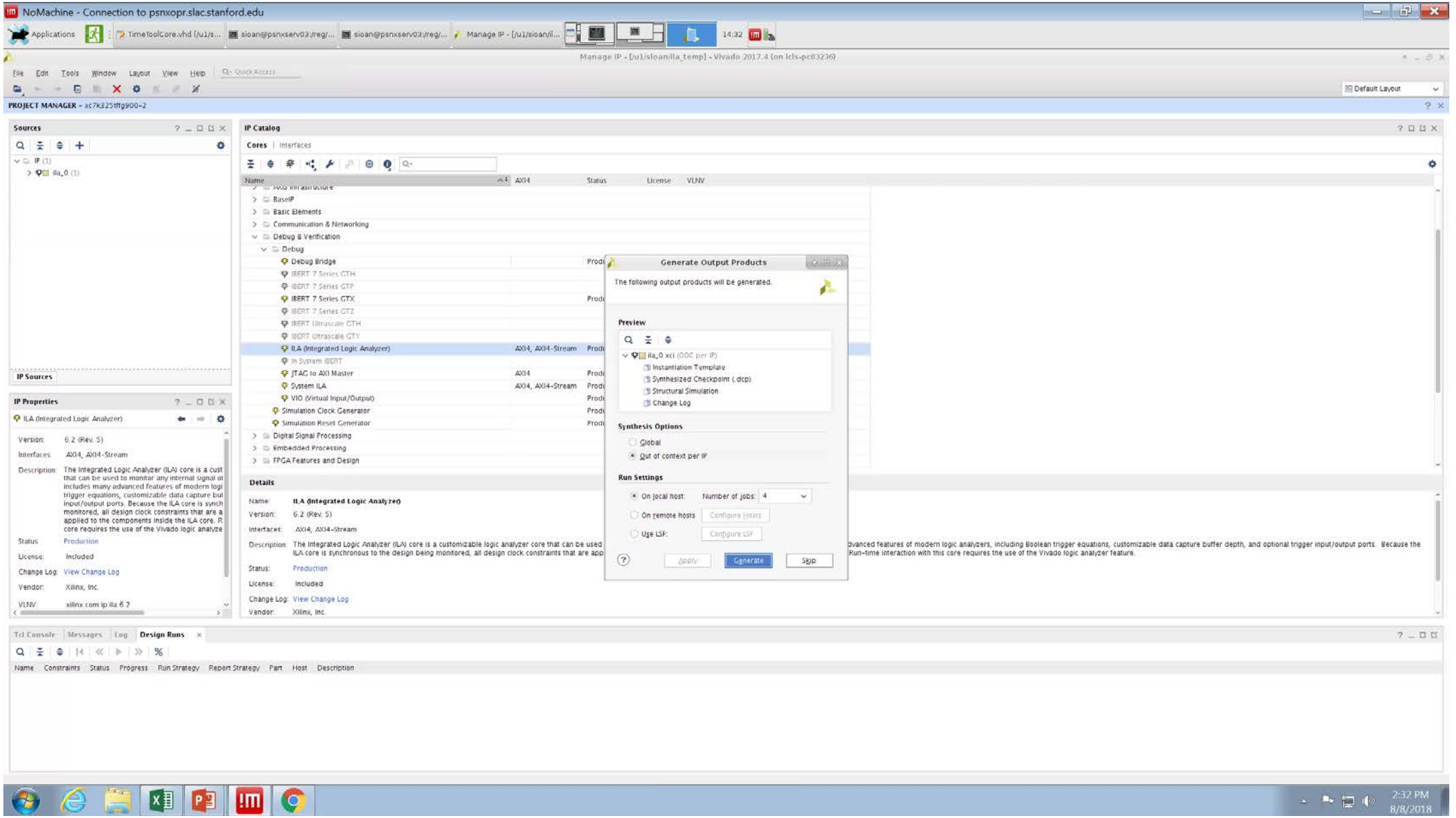

NoMachine - Connection to psnxopr.slac.stanford.edu
Applications
sioan@psnxserv03:/reg/...
sioan@psnxserv03:/reg/...
Vivado 2017.4
14:22
sioan@psnxserv03:/reg/neh/home5/sioan/Desktop
File Edit View Search Terminal Help
Vivado 2017.4 (on lcls-pc83236)
File Flow Tools Window Help
Quick Access
VIVADO
HLx Editions
XILINX
ALL PROGRAMMABLE.
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
New IP Location...
Open IP Location...
Learning Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
Recent Projects
TimeToolKcu1500_project
/u1/sioan/build/TimeToolKcu1500
project_xsim
/u1/sioan/simulation_tutorial/project_xsim/project_xsim
Recent IP Locations
ila_temp
/u1/sioan
Tcl Console
Open the IP Catalog and view available IP. Create and customize IP to be used in a new project or open previously customized IP to make changes.
eg/neh/home5/sioan/Desktop
t.srcs/sources_1/ip/ila_0/ila_0_stub.vhdl
t.srcs/sources_1/ip/ila_0/sim/ila_0.v
t.srcs/sources_1/ip/ila_0/ila_0.xml
t.srcs/sources_1/ip/ila_0/ila_0_stub.v
t.srcs/sources_1/ip/ila_0/ila_0_sim_netlist.vhdl
t.srcs/sources_1/ip/ila_0/synth/ila_0.v
t.srcs/sources_1/ip/ila_0/ila_0.xci
t.srcs/sources_1/ip/ila_0/ila_0.veo
t.srcs/sources_1/ip/ila_0/hdl/verilog/ila_v6_2_5_ila_in.vh
t.srcs/sources_1/ip/ila_0/hdl/verilog/ila_v6_2_5_ila_lib_fn
t.srcs/sources_1/ip/ila_0/hdl/verilog/ila_v6_2_5_ila_ver.vh
t.srcs/sources_1/ip/ila_0/hdl/verilog/ila_v6_2_5_ila_param.
t.srcs/sources_1/ip/ila_0/hdl/verilog/ila_v6_2_5_ila_lparam
t.srcs/sources_1/ip/ila_0/hdl/ila_v6_2_syn_rfs.v
t.srcs/sources_1/ip/ila_0/doc/ila_v6_2_changelog.txt
t.srcs/sources_1/ip/ila_0/ila_0.dcp
t.runs/ila_0_synth_1
t.runs/ila_0_synth_1/ila_0_utilization_synth.pb
t.runs/ila_0_synth_1/ila_0_utilization_synth.rpt
t.runs/ila_0_synth_1/ila_0.vds
t.runs/ila_0_synth_1/ila_0.tcl
t.runs/ila_0_synth_1/ila_0.dcp
^C
(timetoolqt5) [sioan@lcls-pc83236 sioan]$find . -iname ila*^C
(timetoolqt5) [sioan@lcls-pc83236 sioan]$cd lcls2-pcie-apps/
(timetoolqt5) [sioan@lcls-pc83236 lcls2-pcie-apps]$find . -iname ila*
./firmware/applications/TimeTool/coregen/ila_0.xci
(timetoolqt5) [sioan@lcls-pc83236 lcls2-pcie-apps]$
2:22 PM
8/8/2018


NoMachine - Connection to psnxopr.slac.stanford.edu
Applications
sioan@psnxserv03:/reg/...
sioan@psnxserv03:/reg/...
Vivado 2017.4
14:23
sioan@psnxserv03:/reg/neh/home5/sioan/Desktop
File Edit View Search Terminal Help
Vivado 2017.4 (on lcls-pc83236)
File Flow Tools Window Help Quick Access
VIVADO HLx Editions
XILINX ALL PROGRAMMABLE.
Quick Start
Create Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store
Learning Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
New IP Location
Manage IP Settings
Set options for creating and generating IP.
Part: Kintex-7 KC705 Evaluation Platform (xc7k325tffg900-2)
Target language: VHDL
Target simulator: Vivado Simulator
Simulator language: Mixed
IP location: /u1/sioan/ila_temp
< Back
Next >
Finish
Cancel
Tcl Console
Start using Vivado with the IP Catalog as a starting point to more quickly customize and create IP.
eg/neh/home5/sioan/Desktop
t.srcs/sources_1/ip/ila_0/ila_0_stub.vhdl
t.srcs/sources_1/ip/ila_0/sim/ila_0.v
t.srcs/sources_1/ip/ila_0/ila_0.xml
t.srcs/sources_1/ip/ila_0/ila_0_stub.v
t.srcs/sources_1/ip/ila_0/ila_0_sim_netlist.vhdl
t.srcs/sources_1/ip/ila_0/synth/ila_0.v
t.srcs/sources_1/ip/ila_0/ila_0.xci
t.srcs/sources_1/ip/ila_0/ila_0.veo
t.srcs/sources_1/ip/ila_0/hdl/verilog/ila_v6_2_5_ila_in.vh
t.srcs/sources_1/ip/ila_0/hdl/verilog/ila_v6_2_5_ila_lib_fn
t.srcs/sources_1/ip/ila_0/hdl/verilog/ila_v6_2_5_ila_ver.vh
t.srcs/sources_1/ip/ila_0/hdl/verilog/ila_v6_2_5_ila_param.
t.srcs/sources_1/ip/ila_0/hdl/verilog/ila_v6_2_5_ila_lparam
t.srcs/sources_1/ip/ila_0/hdl/ila_v6_2_syn_rfs.v
t.srcs/sources_1/ip/ila_0/doc/ila_v6_2_changelog.txt
t.srcs/sources_1/ip/ila_0/ila_0.dcp
t.runs/ila_0_synth_1
t.runs/ila_0_synth_1/ila_0_utilization_synth.pb
t.runs/ila_0_synth_1/ila_0_utilization_synth.rpt
t.runs/ila_0_synth_1/ila_0.vds
t.runs/ila_0_synth_1/ila_0.tcl
t.runs/ila_0_synth_1/ila_0.dcp
^C
(timetoolqt5) [sioan@lcls-pc83236 sioan]$find . -iname ila*^C
(timetoolqt5) [sioan@lcls-pc83236 sioan]$cd lcls2-pcie-apps/
(timetoolqt5) [sioan@lcls-pc83236 lcls2-pcie-apps]$find . -iname ila*
./firmware/applications/TimeTool/coregen/ila_0.xci
(timetoolqt5) [sioan@lcls-pc83236 lcls2-pcie-apps]$
2:23 PM
8/8/2018


NoMachine - Connection to psnxopr.slac.stanford.edu
Applications
sioan@psnxserv03:/reg/...
sioan@psnxserv03:/reg/...
Manage IP - [/u1/sioan/il...
14:26
Manage IP - [/u1/sioan/ila_temp] - Vivado 2017.4 (on lcls-pc83236)
File Edit Tools Window Layout View Help
Quick Access
Default Layout
PROJECT MANAGER - xc7k325tffg900-2
Sources
IP Sources
IP Catalog
Cores | Interfaces
Name
AXI4
Status
License
VLNV
BaseIP
Basic Elements
Communication & Networking
Debug & Verification
Debug
Debug Bridge
Production
Included
xilinx.com:ip:debug_bridge:3.0
IBERT 7 Series GTH
IBERT 7 Series GTP
IBERT 7 Series GTX
IBERT 7 Series GTZ
IBERT Ultrascale GTH
IBERT Ultrascale GTY
ILA (Integrated Logic Analyzer)
AXI4
AXI4-Stream
xilinx.com:ip:ila:6.2
In System IBERT
JTAG to AXI Master
xilinx.com:ip:jtag_axi:1.2
System ILA
xilinx.com:ip:system_ila:1.1
VIO (Virtual Input/Output)
xilinx.com:ip:vio:3.0
Simulation Clock Generator
xilinx.com:ip:sim_clk_gen:1.0
Simulation Reset Generator
xilinx.com:ip:sim_rst_gen:1.0
Digital Signal Processing
Embedded Processing
FPGA Features and Design
Properties... Ctrl+E
IP Settings...
Add Repository...
Refresh All Repositories
Customize IP...
License Status
Compatible Families
Compatible Simulators
Product Guide
Change Log
Product Webpage
Answer Records
Export to Spreadsheet...
Details
Name: ILA (Integrated Logic Anal
Version: 6.2 (Rev. 5)
Interfaces: AXI4, AXI4-Stream
Description: The Integrated Logic Analyzer (ILA) core is a customizable logic analyzer core that can be used to monitor any internal signal of your design. The ILA core includes many advanced features of modern logic analyzers, including Boolean trigger equations, customizable data capture buffer depth, and optional trigger input/output ports. Because the ILA core is synchronous to the design being monitored, all design clock constraints that are applied to your design are also applied to the components inside the ILA core. Run-time interaction with this core requires the use of the Vivado logic analyzer feature.
Status: Production
License: Included
Change Log: View Change Log
Vendor: Xilinx, Inc.
Tcl Console
Messages
Log
Design Runs
Name Constraints Status Progress Run Strategy Report Strategy Part Host Description
Customize the selected core
2:26 PM
8/8/2018


NoMachine - Connection to psnxopr.slac.stanford.edu
Manage IP - [/u1/sioan/ila_temp] - Vivado 2017.4 (on lcls-pc83236)
PROJECT MANAGER - xc7k325tffg900-2
Sources
IP Catalog
Cores | Interfaces
Customize IP
ILA (Integrated Logic Analyzer) (6.2)
Documentation
IP Location
Switch to Defaults
Show disabled ports
Component Name ila_0
To configure more than 64 probe ports use Vivado Tcl Console
General Options
Probe_Ports(0..0)
Probe Port
Probe Width [1..4096]
Number of Comparators
Probe Trigger or Data
PROBE0
256
1
DATA AND TRIGGER
OK
Cancel
Details
Name: ILA (Integrated Lo
Version: 6.2 (Rev. 5)
Interfaces: AXI4, AXI4-Stream
Description: The Integrated Log
ILA core is synchro
Status: Production
License: Included
Change Log: View Change Log
Vendor: Xilinx, Inc.
IP Sources
Tcl Console
Messages
Log
Design Runs
Name
Constraints
Status
Progress
Run Strategy
Report Strategy
Part
Host
Description
2:31 PM
8/8/2018


NoMachine - Connection to psnxopr.slac.stanford.edu
Applications
TimeToolCore.vhd (/u1/s...
sioan@psnxserv03:/reg/...
sioan@psnxserv03:/reg/...
Manage IP - [/u1/sioan/il...
14:39
Manage IP - [/u1/sioan/ila_temp] - Vivado 2017.4 (on lcls-pc83236)
File Edit Tools Window Layout View Help
Quick Access
Default Layout
PROJECT MANAGER - xc7k325tffg900-2
Sources
IP (1)
ila_0 (35)
IP Sources
IP Catalog
Cores | Interfaces
Name
BaseIP
Basic Elements
Communication & Networ
Debug & Verification
Debug
Debug Bridge
IBERT 7 Series GTH
IBERT 7 Series GTP
IBERT 7 Series GTX
IBERT 7 Series GTZ
IBERT Ultrascale GT
IBERT Ultrascale GT
ILA (Integrated Logi
In System IBERT
JTAG to AXI Master
System ILA
VIO (Virtual Input/O
Simulation Clock Gene
Simulation Reset Gene
Digital Signal Processing
Embedded Processing
FPGA Features and Desig
Details
Name: ILA (Integrated Lo
Version: 6.2 (Rev. 5)
Interfaces: AXI4, AXI4-Stream
Description: The Integrated Log
ILA core is synchron
Status: Production
License: Included
Change Log: View Change Log
Vendor: Xilinx, Inc.
Customize IP
ILA (Integrated Logic Analyzer) (6.2)
Documentation
IP Location
Switch to Defaults
Show disabled ports
Component Name ila_1
To configure more than 64 probe ports use Vivado Tcl Console
General Options
Probe_Ports(0..0)
Monitor Type
Native
AXI
Number of Probes 1 [1...1024]
Sample Data Depth 1024
Same Number of Comparators for All Probe Ports
Number of Comparators 1
Trigger Out Port
Trigger In Port
Input Pipe Stages 2
Trigger And Storage Settings
Capture Control
Advanced Trigger
GUI configuration mode is limited to 64 probe ports.
OK
Cancel
IP Properties
ILA (Integrated Logic Analyzer)
Version: 6.2 (Rev. 5)
Interfaces: AXI4, AXI4-Stream
Description: The Integrated Logic Analyzer (ILA) core is a cust
that can be used to monitor any internal signal of
includes many advanced features of modern logi
trigger equations, customizable data capture but
input/output ports. Because the ILA core is synch
monitored, all design clock constraints that are a
applied to the components inside the ILA core. R
core requires the use of the Vivado logic analyze
Status: Production
License: Included
Change Log: View Change Log
Vendor: Xilinx, Inc.
VLNV: xilinx.com:ip:ila:6.2
ons, customizable data capture buffer depth, and optional trigger input/output ports. Because the
zer feature.
Tcl Console
Messages
Log
Design Runs
Name
Constraints
Status
Progress
Run Strategy
Out-of-Context Module Runs
ila_0_synth_1
ila_0
synth_design Complete!
100%
Vivado Synthesis Defaults (Vivado Synthesis 2017)
Vivado Synthesis Default Reports (Vivado Synthesis 2017)
xc7k325tffg900-2
Vivado Synthesis Defaults
2:39 PM
8/8/2018


NoMachine - Connection to psnxopr.slac.stanford.edu
Manage IP - [/u1/sloan/ila_temp] - Vivado 2017.4 (on lcls-pc83236)
PROJECT MANAGER - xc7k325tffg900-2
Sources
IP Catalog
Cores | Interfaces
IP Properties
Generate Output Products
The following output products will be generated.
Preview
Synthesis Options
Run Settings
Generate
Skip
Tcl Console
Messages
Log
Design Runs