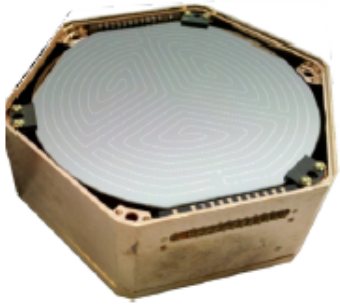


SuperCDMS SNOLAB

CD 2/3 Status Review

Readout Electronics – WBS 1.5

Bruce Hines

January 24 – 26, 2018

Presentation Outline

- Introduction
  - Key deliverables
  - Technical requirements
- Flow-down from science goals
- WBS definition and organization
- Technical designs
- Design maturity
- Schedule
- Costs
- Responses to past review recommendations
- Risks and mitigations

Readout Electronics – Introduction

Key Deliverables

- Readout cabling
  (wiring from detector tower to vacuum interface)
- Detector Control and Readout Card (DCRC)
  (room-temperature electronics)
- Signal Distribution Unit (SDU)
  (clock fan-out to synchronize signals)
- Vacuum Interface Board (VIB)
  (connection point for room-temperature electonics)
- Heat sinks for cables

Requirements

- Phonon-channel noise of SQUID plus Readout Electronics:
  < 4.5 pA/rtHz in white noise region
  < 10 pA/rtHz at 100 Hz
  (detector noise should dominate)
- Charge amp output noise including HEMT < 300 nV/rtHz at low frequencies
- Bandwidth of phonon and charge channels both 100 kHz
- Adequate radiopurity
- Signal amplification and readout with sufficient fidelity
- Suitable interface with DAQ

Science Goals Flow-down to Technical Requirements

Science Goals

SG-1 Search for dark matter particles with masses below 10 GeV/c^2 using complementary target nuclei (germanium and silicon) and complementary techniques (iZIP and HV) that will provide an understanding of residual backgrounds.

SG-2 Design for the possibility of future upgrades that would further increase the low-mass sensitivity of the experiment to the level where solar neutrinos are detected.

Technical Requirements

	Required	Goal
HV detectors		
Phonon energy resolution (σ) for Ge (Si)	50 (35) eV_t	10 (7) eV_t
Minimum bias voltage	50 V	100 V
iZIP detectors		
Phonon energy resolution (σ) for Ge (Si)	100 (50) eV_t	50 (25) eV_t
Charge energy resolution (σ) for Ge (Si)	300 (330) eV_{ee}	160 (180) eV_{ee}
Bandwidth for DAQ/trigger system	50 MB/s	100 MB/s

Readout Electronics

Noise level for phonon channels (SQUID plus readout electronics)
- white noise region: < 4.5 pA/$Hz^{½}$
- at 100 Hz: < 10 pA/$Hz^{½}$

Noise level for charge channels (iZIP detectors)
- 300 nV/$Hz^{½}$ at charge amp output at low frequencies (HEMT plus electronics)

DCRC analog bandwidth
- phonon channels: enough for possible 100 kHz from L/R of input circuit
- charge channels: 100 kHz

phonon pulse sampling rate: 625 ksps
charge pulse sampling rate: 2.5 Msps

Readout Electronics – Organization

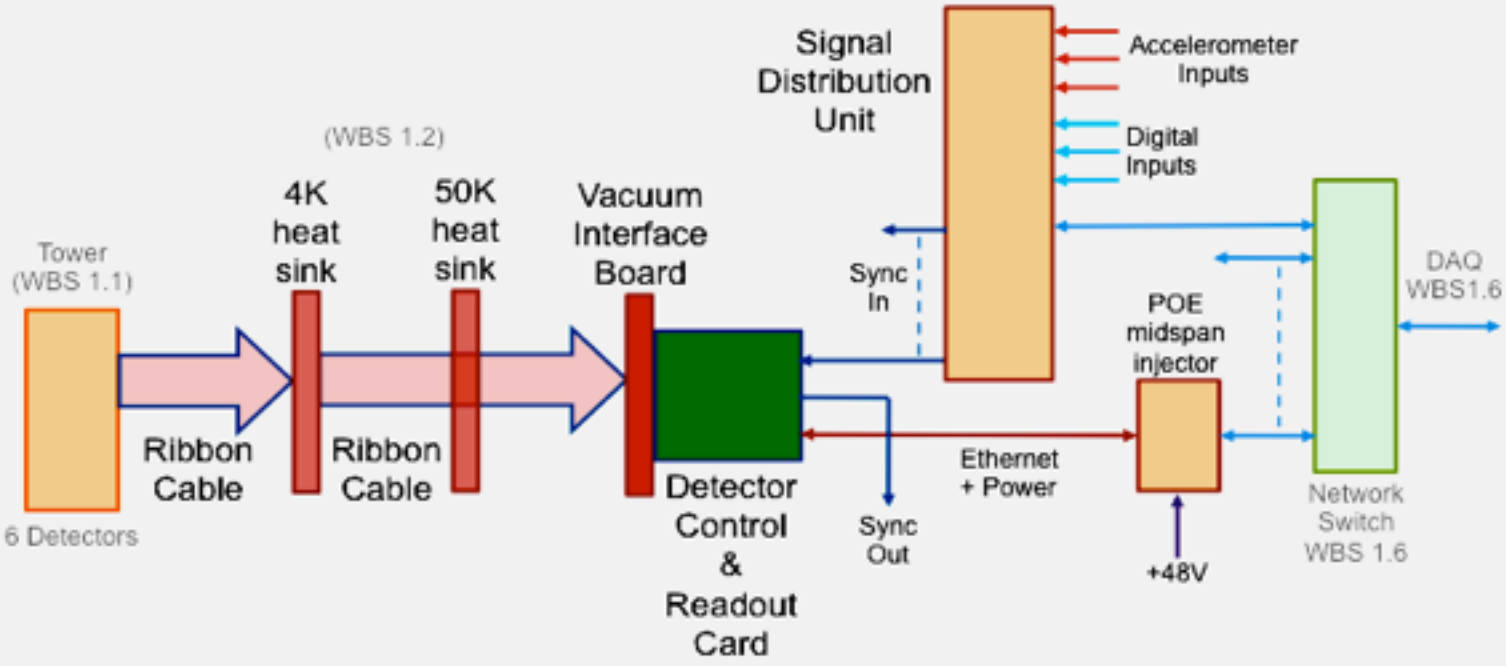
WBS

- 1.5.1: readout cabling
- 1.5.2.1 – 1.5.2.4: Detector Control and Readout Card (DCRC)
- 1.5.2.5: Signal Distribution Unit (SDU)
- 1.5.3.1 – 1.5.3.2: Vacuum Interface Board (VIB)
- 1.5.3.3 – 1.5.3.4: – heat sinks
- 1.5.4 – management

Organization

- Readout cabling: SLAC (Pelle Hansson)
- DCRC, SDU, VIB: FNAL, electronics (Sten Hansen)
- Heat sinks: FNAL, cryogenics (Matt Hollister)
- Management: CU Denver (Bruce Hines)

Readout Electronics Overview

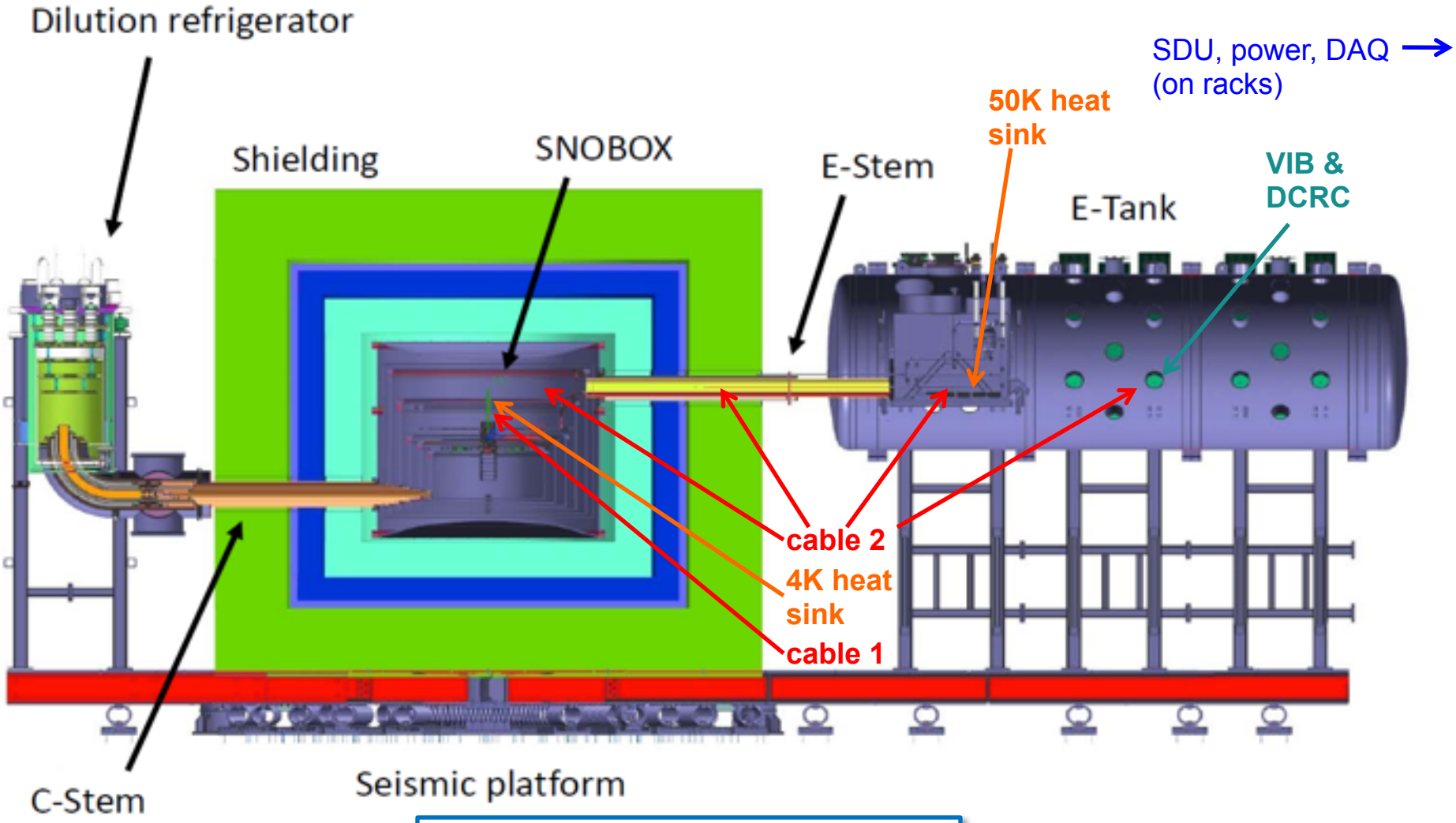


iZIP detector: 12 phonon channels, 4 charge channels, 6 LEDs, 1 Thermometer, 1 DCRC

HV detector: 12 phonon channels, no charge channels, 6 LEDs, 1 Thermometer, 2 DCRCs

Readout Electronics interfaces with other sub-systems (1.1, 1.2, 1.6)

Readout Electronics Overview



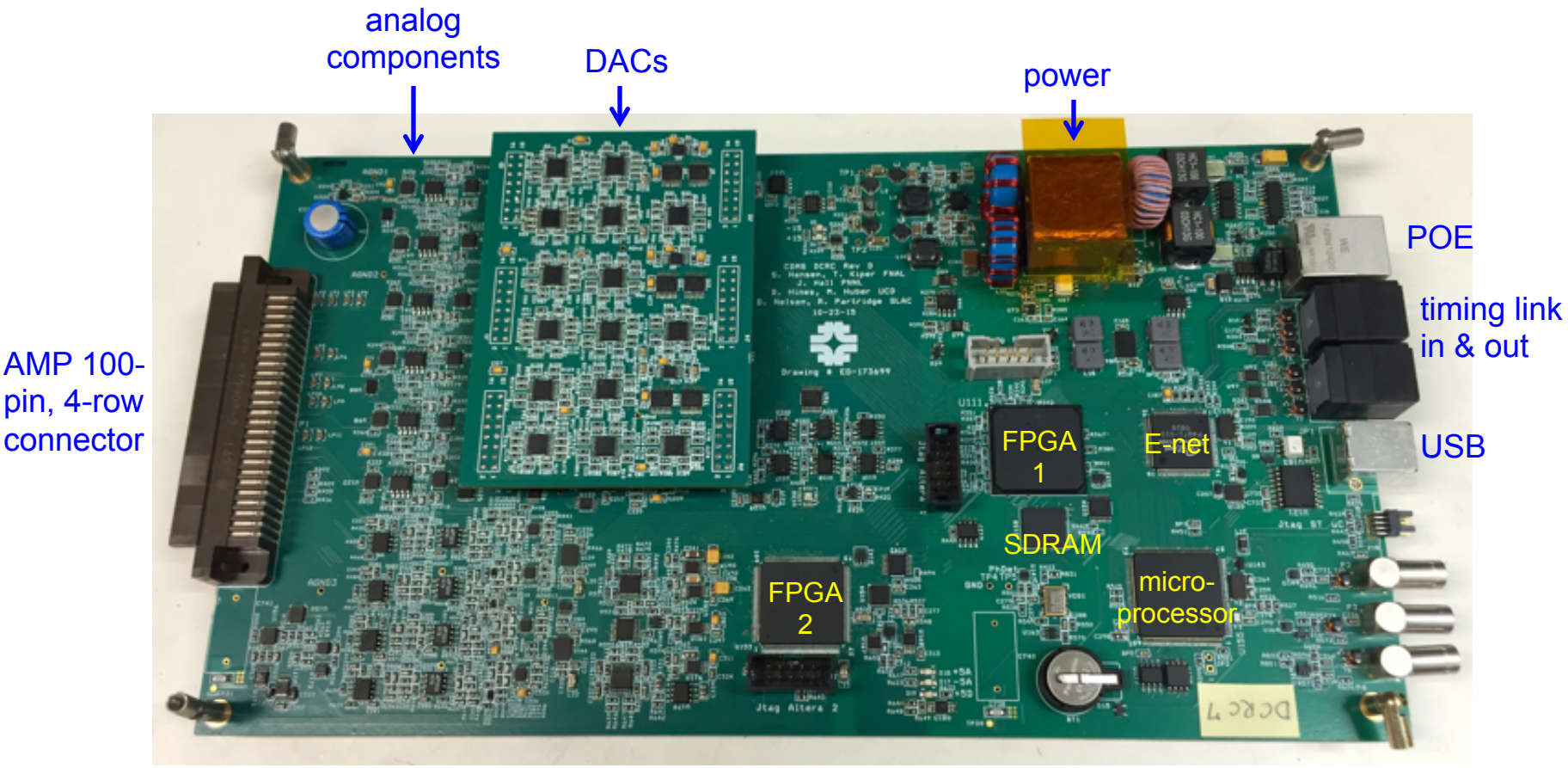
Physical locations of elements

Readout Cable

- 100 wires (32 gauge)
- 50 twisted pairs, woven into 1-inch wide cable
  - SNOLAB cable 1: all pairs are copper
  - SNOLAB cable 2: 48 P-bronze to balance thermal & electrical conduction, 2 Cu for analog ground
- Photo of cable for test facility
  - Soldered to connectors
  - Connector to top of tower on left
  - Connector to vacuum interface on right
  - Epoxy strain relief (blue)
- Fuzz Button array on bottom side of connector on the left (not visible)
- Same readout cables used for both iZIP and HV detectors

Readout cable design/fab progressing well

Detector Control and Readout Card



Prototype room-temperature electronics fabricated, thoroughly tested

DCRC functions

- Bias and tune detectors, SQUIDs, HEMTs
- Readout and amplify signals (ionization and phonon pulses)
- Feedback circuitry for phonon and ionization channels
- Test signals for phonon channels
- Analog-to-digital conversion
- Level 1 trigger
- Control of LEDs for detector neutralization (both iZIP and HV)
- Drive and readout thermometers
- Interface to SDU (pulse synchronization) and to DAQ (controls, buffering, data transfer)
- SQUID warmup to remove trapped flux

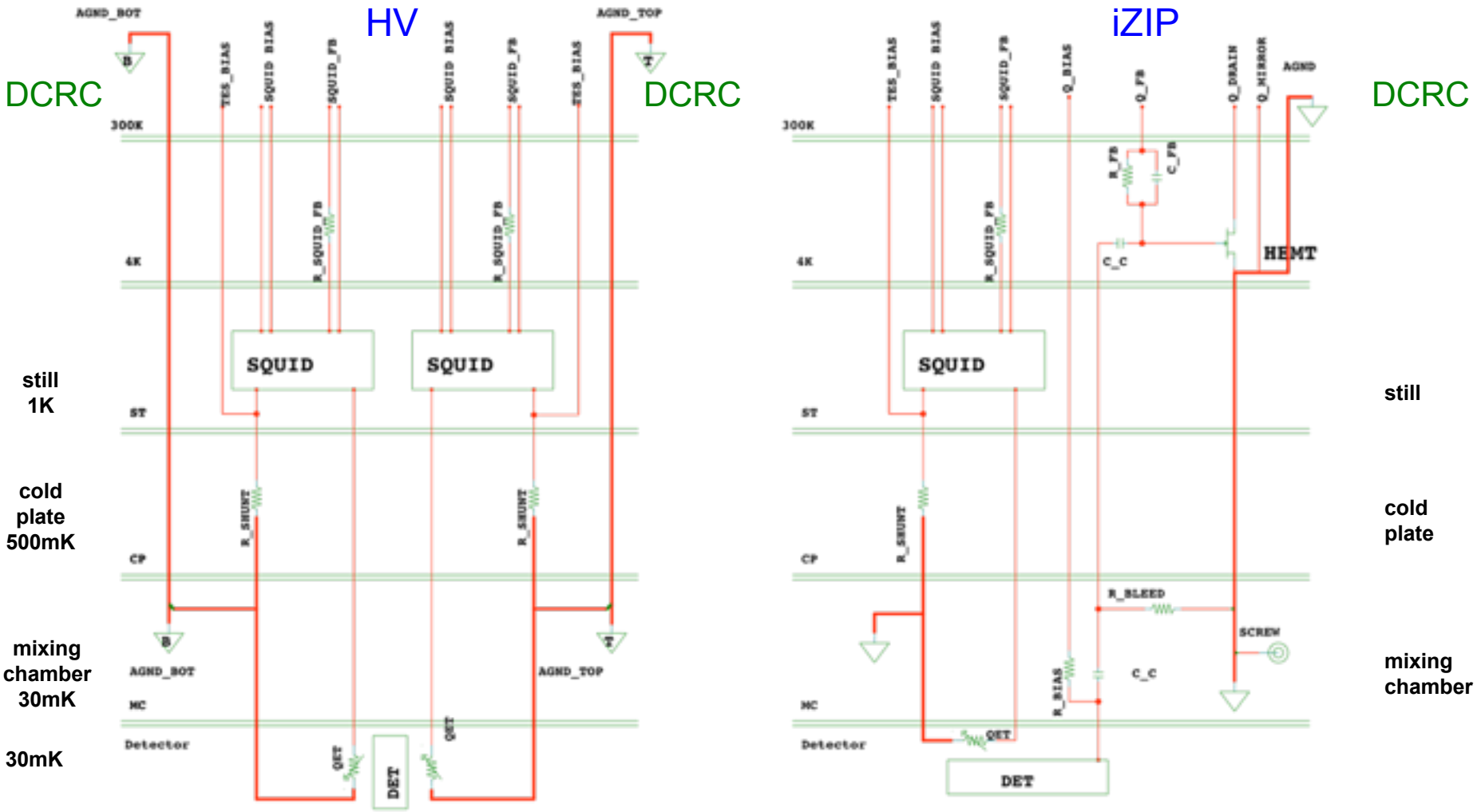
Functionality has been defined and verified with testing

DCRC use

- Plugs directly into vacuum interface on E-tank via 100-pin connector
- 6 DCRCs per iZIP detector tower
- 12 DCRCs per HV detector tower
- 36 DCRCs for initial SNOLAB payload
- Data transfer capability – 8 Msps for each DCRC
- For HV detector, traces from two DCRCs merge on VIB to single readout cable
- Power-over-ethernet (POE+ protocol) via mid-span injectors
- For HV detector, DCRC floats at voltage of corresponding side of detector (DCRC ground plane connects to TESes via analog ground)

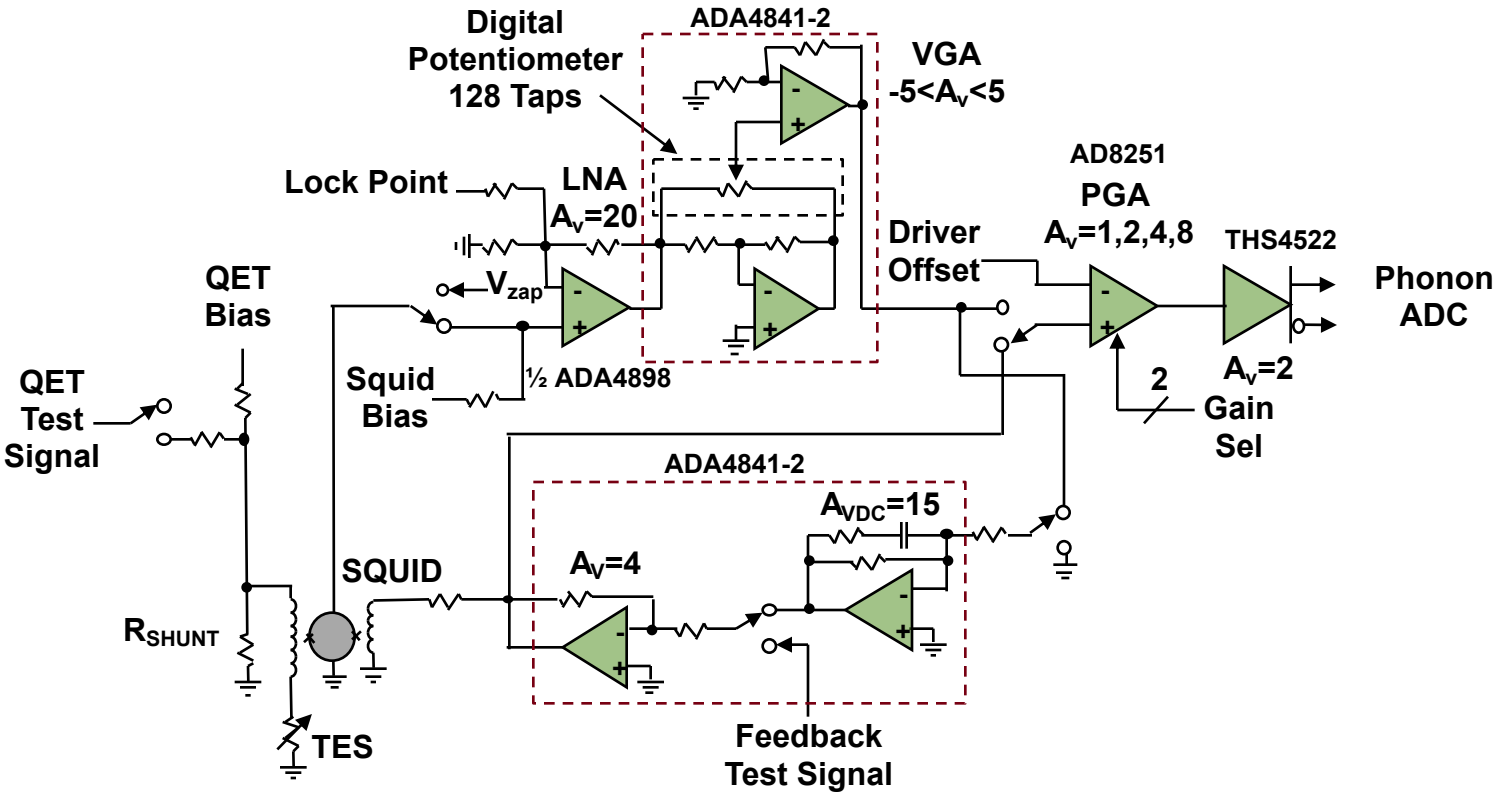
Overall setup has been worked out, testing in progress

DCRC – relation to tower electronics



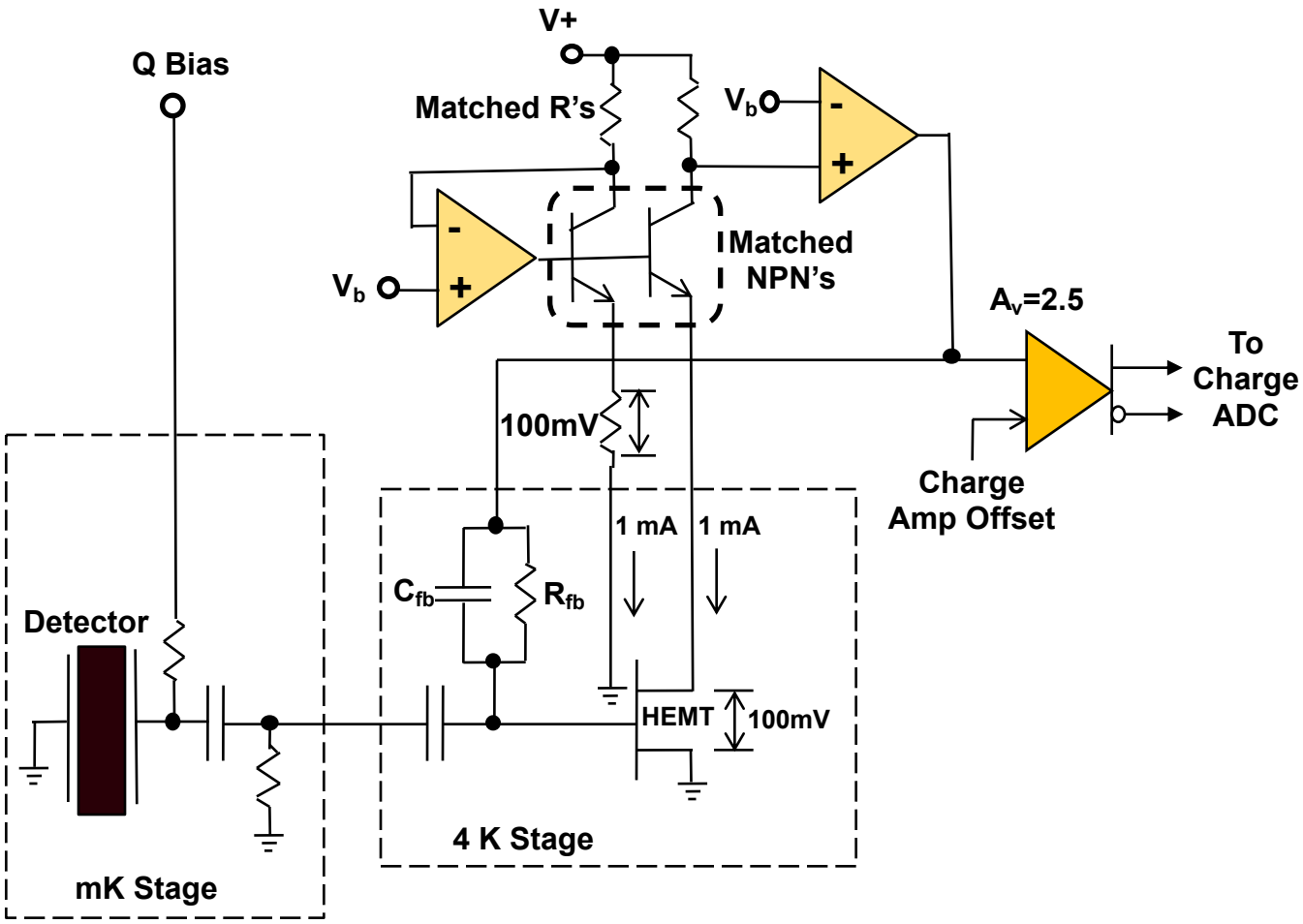
Readout electronics and tower electronics are coordinated

Preproduction DCRC, Block Diagram of Phonon Channel



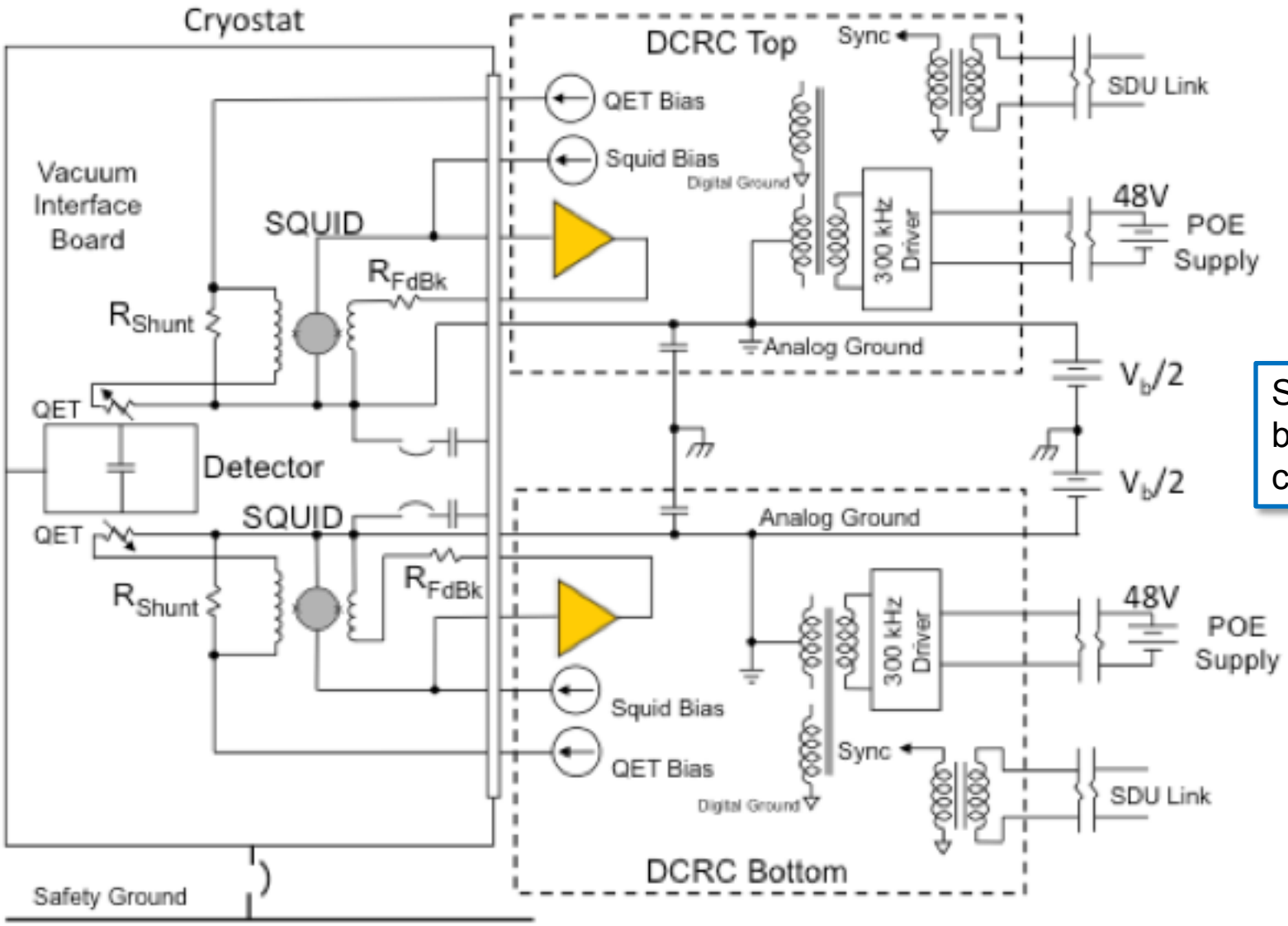
Phonon signal amplifier design is mature, functionality tested, meets specs

DCRC – single charge channel block diagram



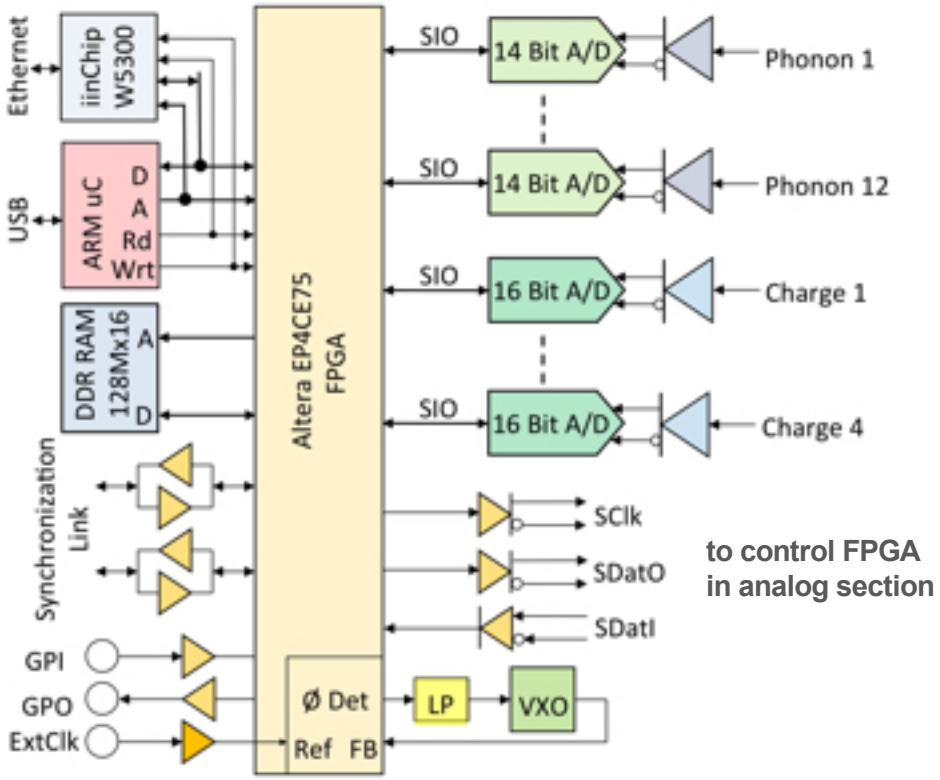
Ionization signal amplifier design is mature, verified by tests

High-voltage Bias Detail



Same DCRC for both HV & iZIP, connections set

Block Diagram of Digital Section



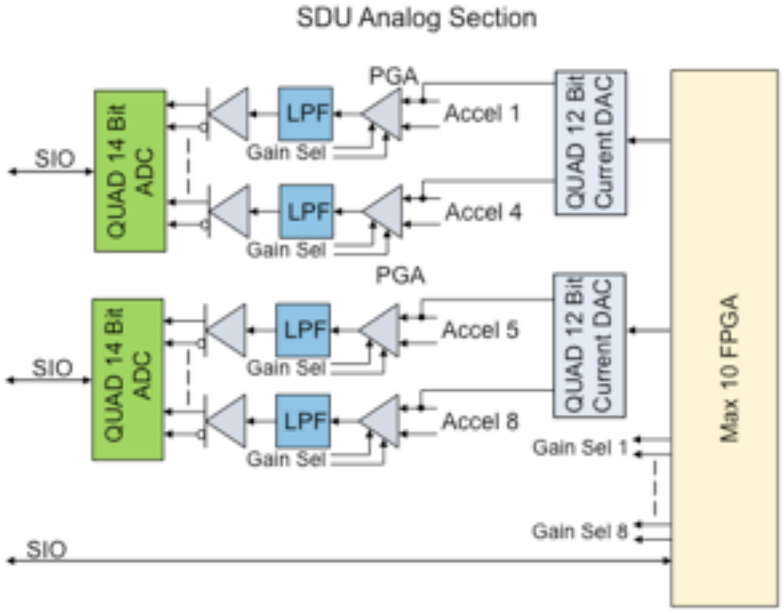
Room-temperature electronics design is mature, verified by tests

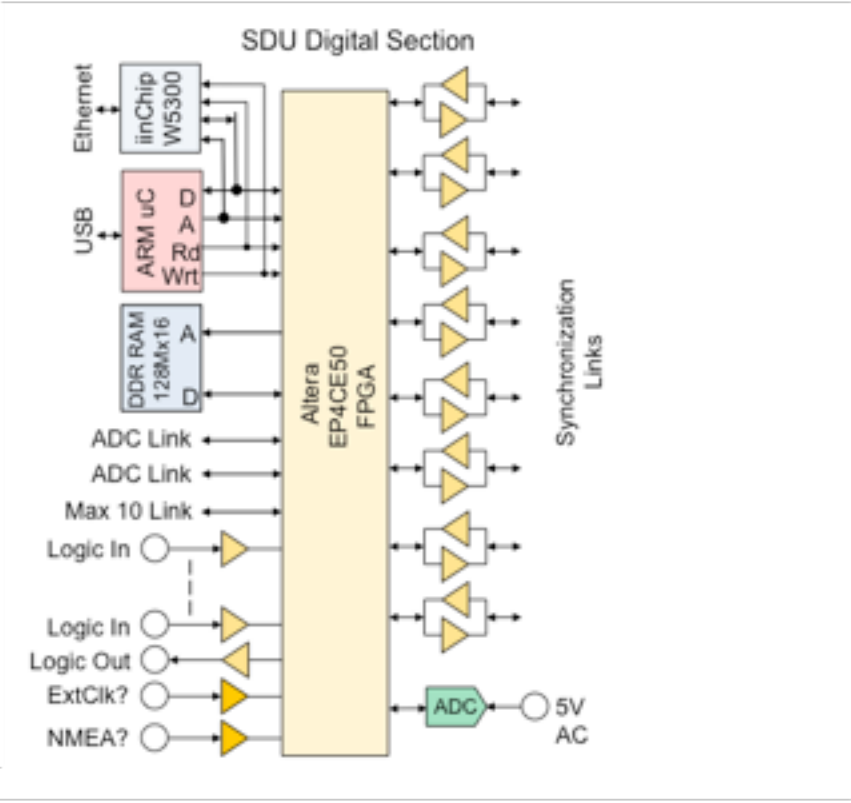
Signal Distribution Unit

- Synchronizes all DCRCs so pulses from all detectors are aligned in time
  - Transmits an 20MHz FM sychronization signal to all DCRCs
  - Uses a voltage-controlled crystal oscillator and a phase-lock loop
  - Makes the SDU and DCRC clocks coherent
  - groups of six DCRCs, daisy-chained together, connect to SDU via RJ-45 connectors
  - A command from DAQ to SDU synchronizes DCRCs
  - Timing is based on the DAQ computer's clock (synchronized to SNOLAB's Network Time Protocol system)
  - SDU capable of using GPS signal for timing (possible future upgrade)
  - Propagation times of signals have been taken into account
  - Any timing mismatch between DCRCs is a negligible fraction of fastest sampling rate
- Includes logic signals for acoustic sensors, phase monitors, and auxiliary monitoring time stamps (if needed)
- Condition, digitize, and buffer accelerometer signals (if needed)
- Can broadcast synchronous messages to all DCRCs (e.g. an L1-trigger-inhibit signal)

SDU schematic/layout done

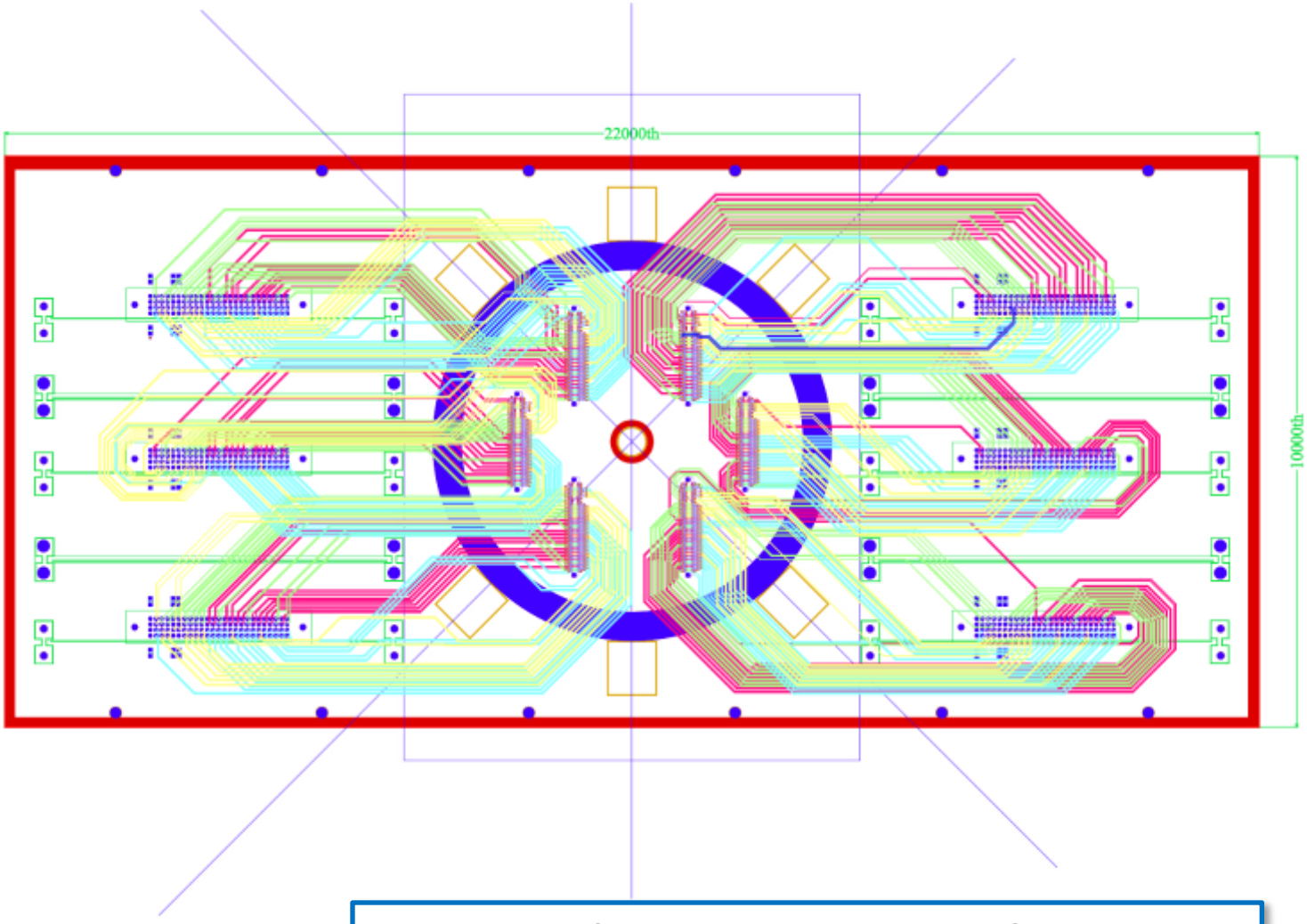
Signal Distribution Unit





SDU schematic/layout done

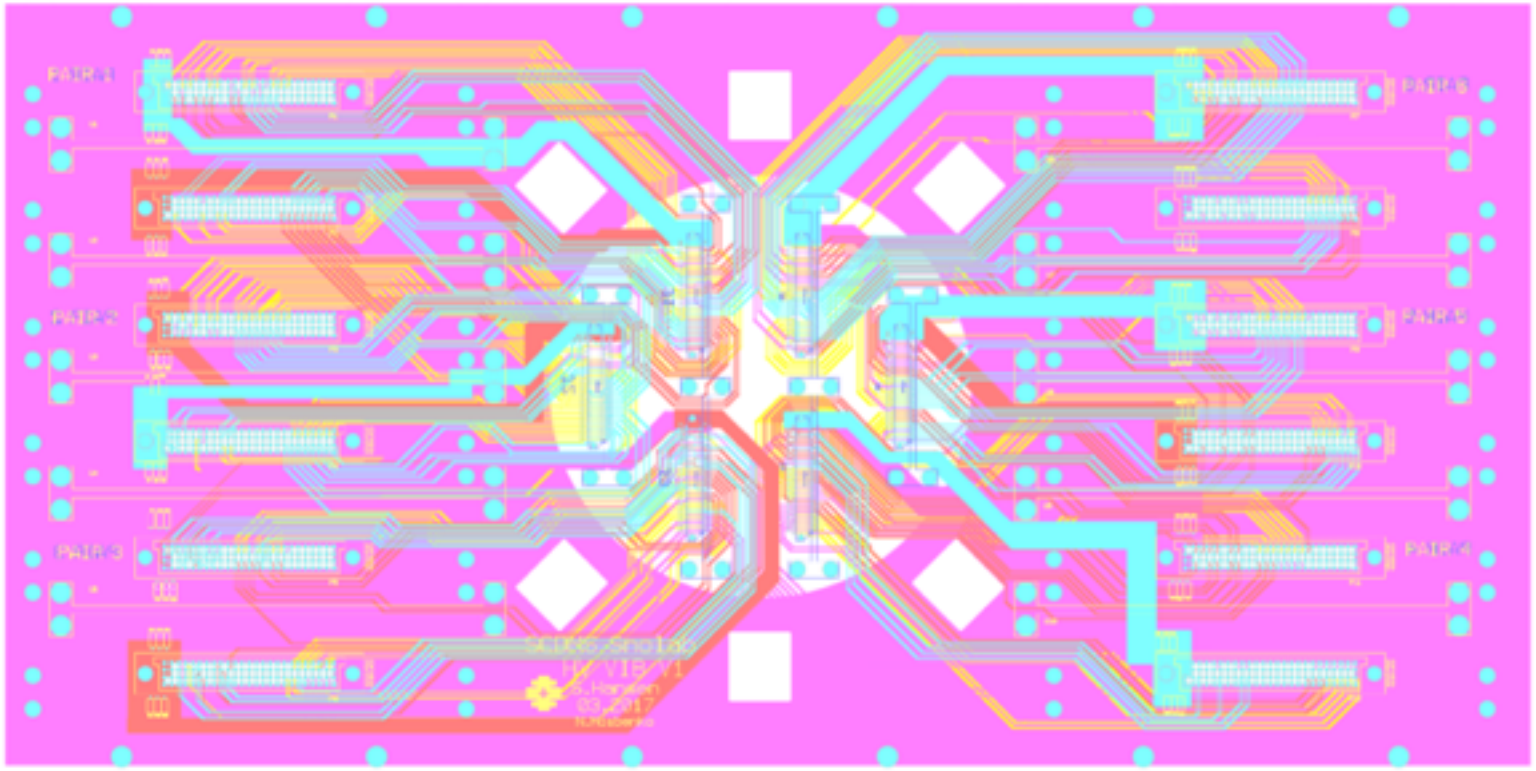
Vacuum Interface Board – Layout for iZIP



- All layers superimposed
- 22 x 10 inches
- Six DCRCs connect on air side
- Six cables connect on vacuum side
- 600 traces
- Large blue ring for vacuum seal
- Revised version has filters on all lines entering cryostat

VIB design for iZIP is mature, verified by tests

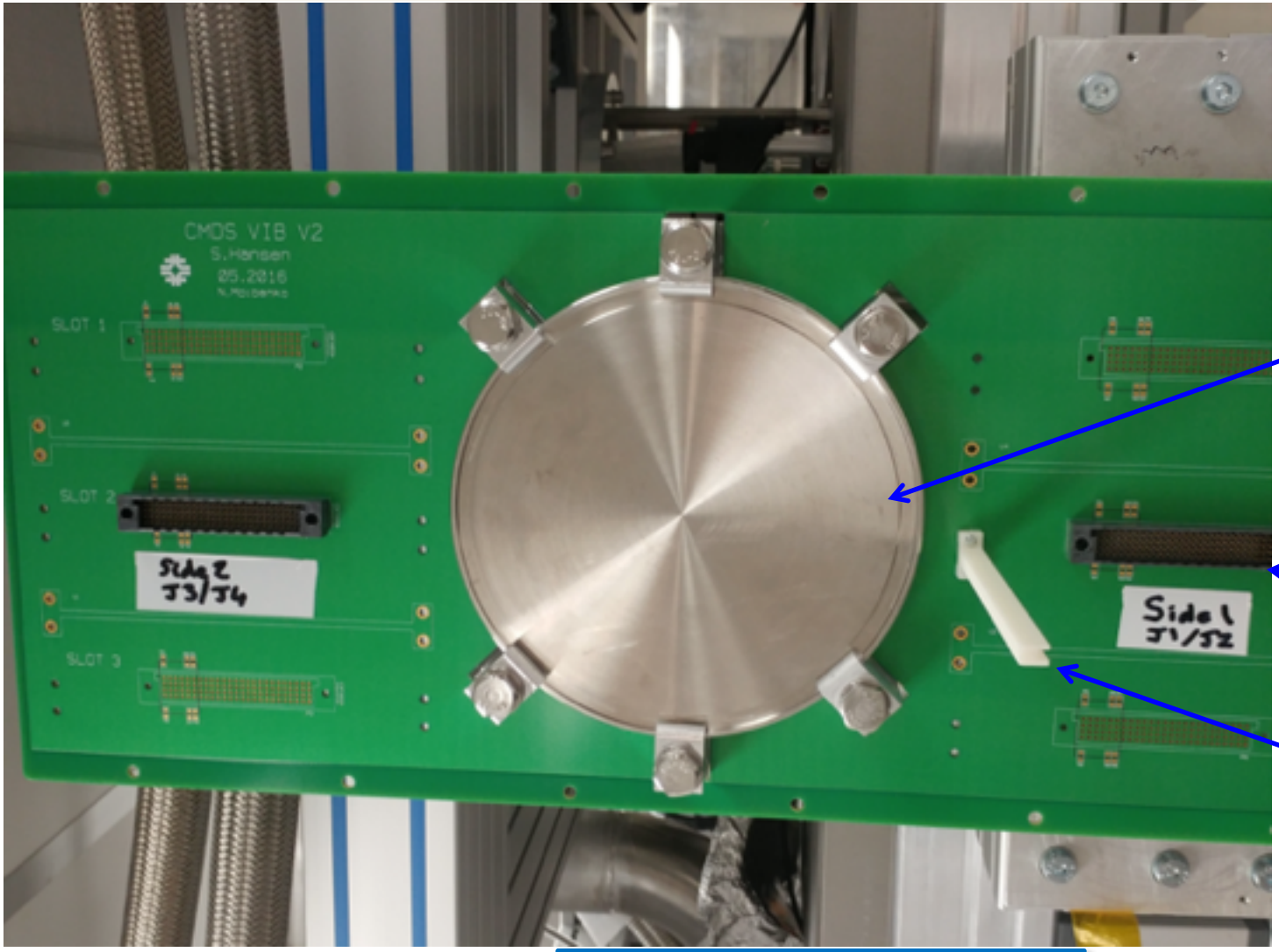
Vacuum Interface Board – Layout for HV



- All layers superimposed
- 22 x 11 inches
- 12 DCRCs connect on air side
- Six cables connect on vacuum side
- 600 traces
- Filters on all lines entering cryostat

HV VIB design is mature, verified by tests

VIB for iZIP – Tested at SLAC



Air side

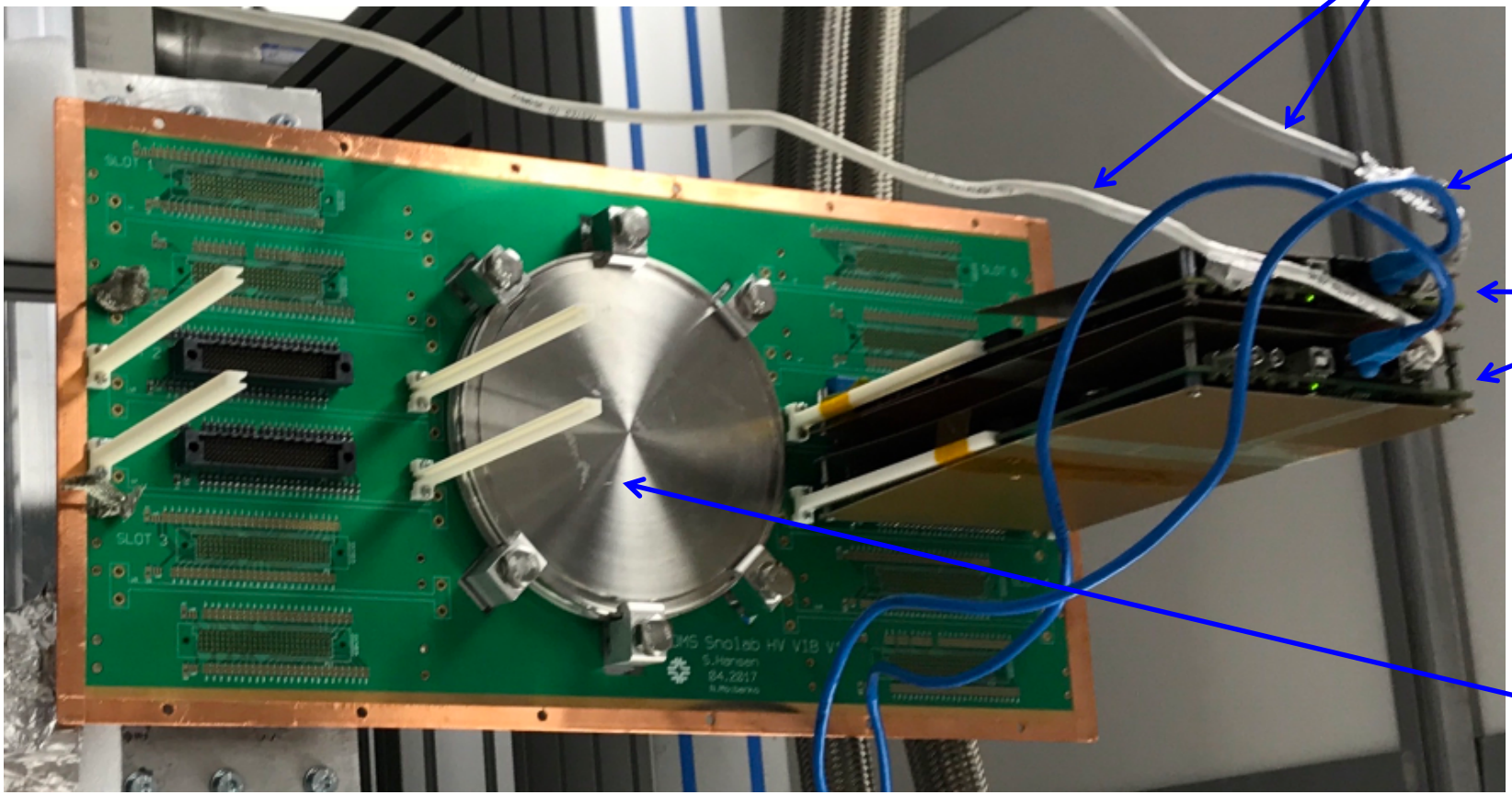
Vacuum flange

Connector to DCRC

DCRC support

iZIP VIB fabricated, tested

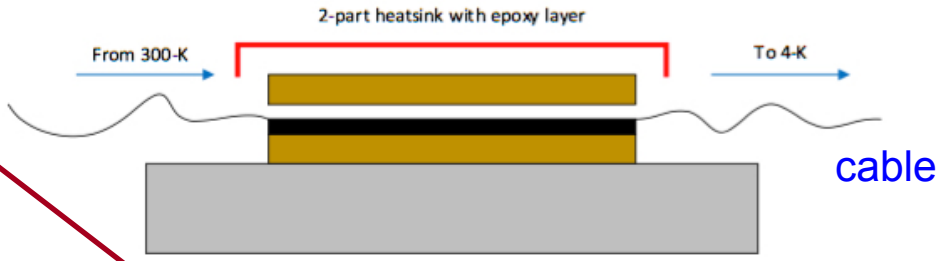
High-voltage VIB – in use at SLAC



HV VIB fabricated, tested

Heat Sinks

4K

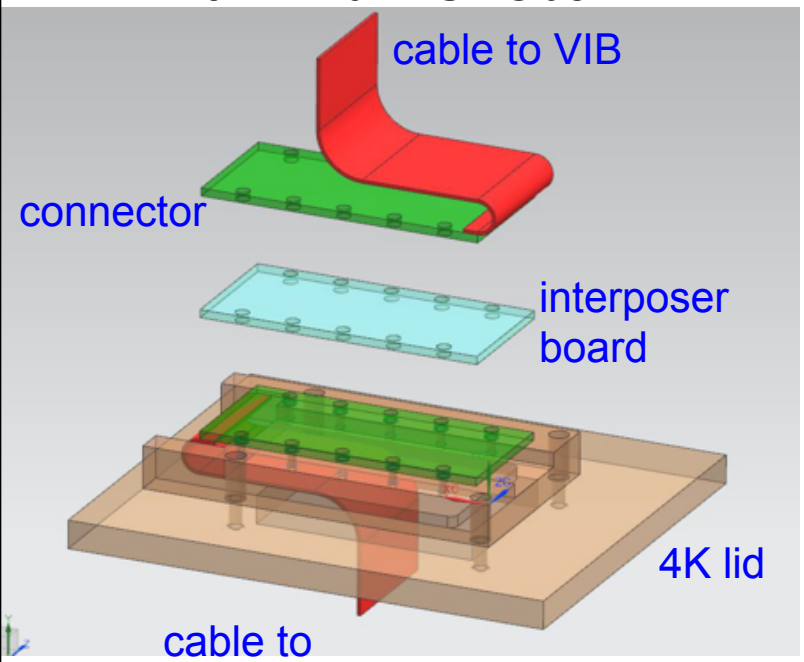


50K Layer of E-Tank

- ΔT = 0.2 K
- 4” long

50K

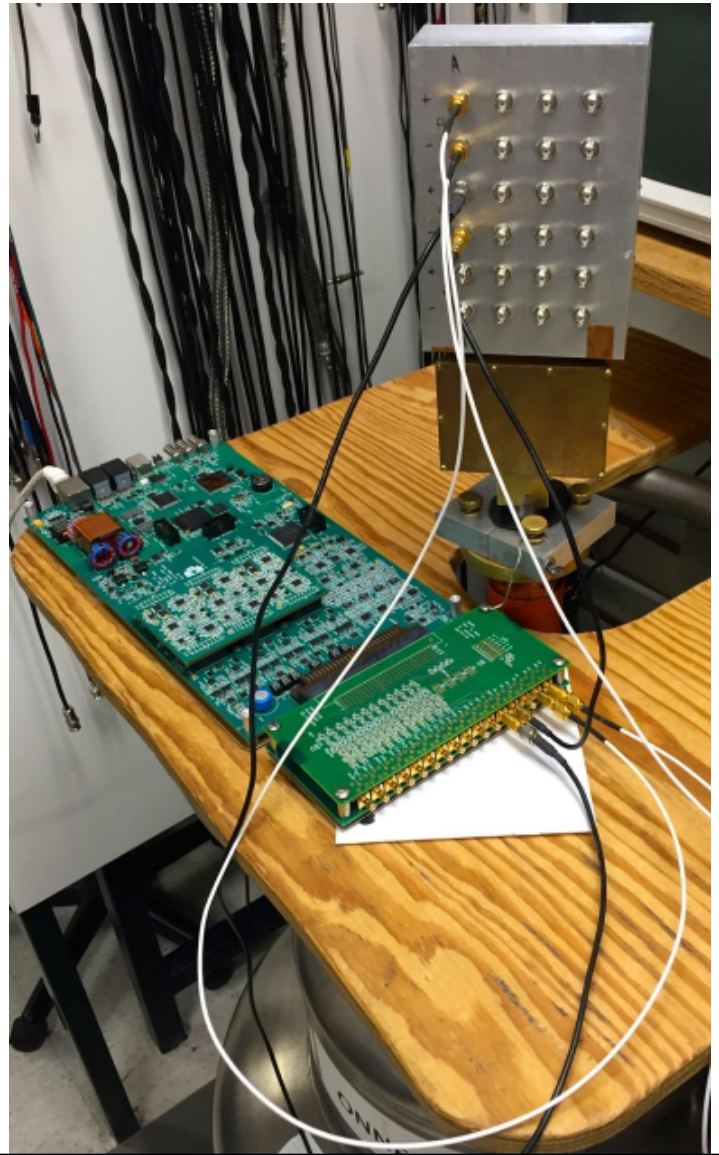
At LH Lid in SNObox



- ΔT = 10 mK
- Fuzz Button connectors
- Connectors 2.4” x 1.1”
- Upper connector must be narrow so many of them can pass through E-stem

Design of heat sinks mature

Testing



Test setup at CU Denver

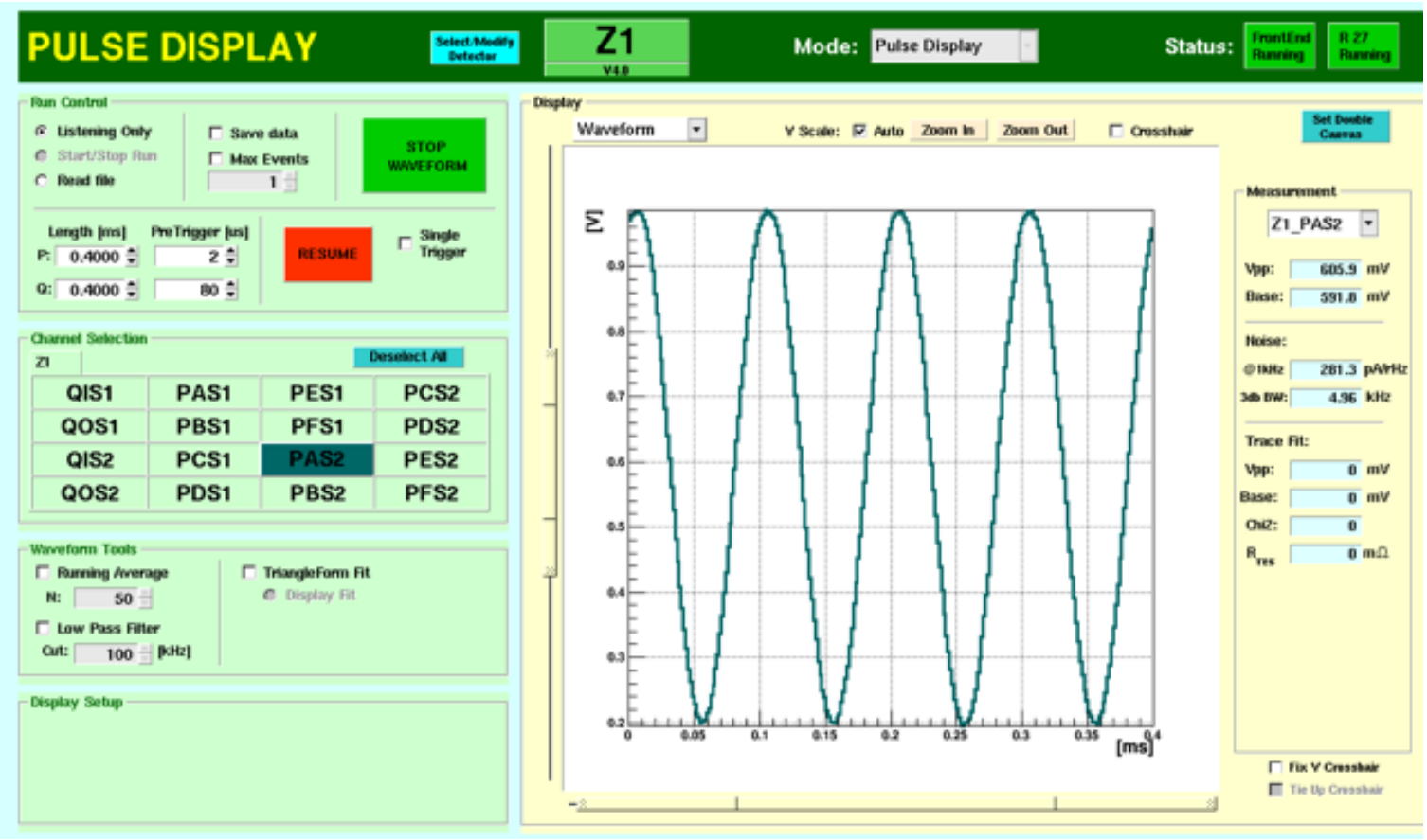
- DCRC
- Dunk probe with cold SQUID
- Power-over-ethernet cable (white, far left)
- Signals travel via separate breakout board plugged into DCRC

Extensive testing of prototype DCRC with detectors has also taken place at SLAC (also with prototype readout cable, detectors, and tower electronics) and at Berkeley

Testing plan well underway

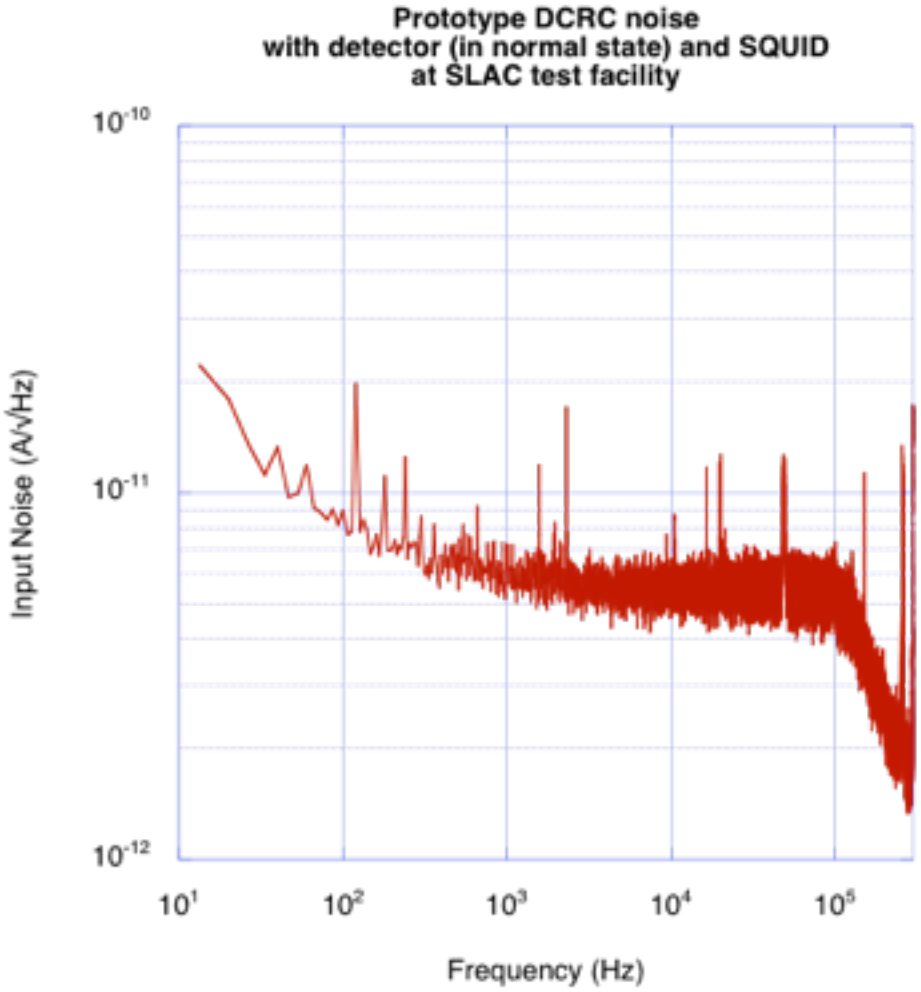
Example of Test Results – DCRC with cold SQUID

- SQUID output via DAQ graphical user interface
- Amplified sinusoidal 10kHz input (closed loop)



Basic functionality demonstrated

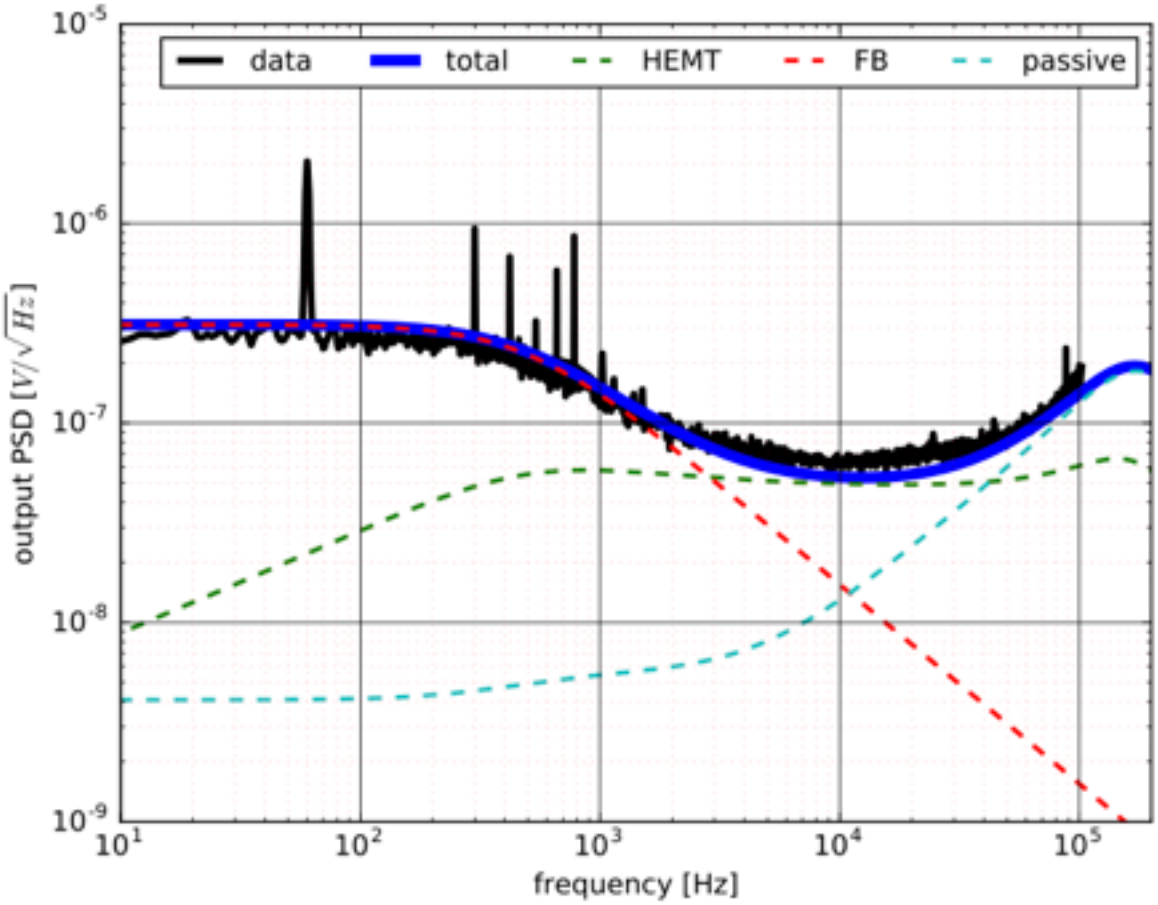
DCRC Test Results – another example (SLAC)



- Major accomplishment!
- Phonon channel noise, with SQUID, prototype cold hardware, and detector
- When detector is normal, noise from readout electronics dominates
- Meets requirements
- SQUID noise is sub-dominant

Staged testing of noise progressing, successful

Test Results of Ionization Ampifier Design (SLAC)



Charge amplifier noise at output

- Same circuit as DCRC (different board)
- Model (blue) matches measured values (black) at frequencies of primary interest (< 1 kHz)
- Modeling indicates this noise level will allow the desired charge sensitivity
- Needs to be measured with DCRC and SNOLAB cold hardware/electronics

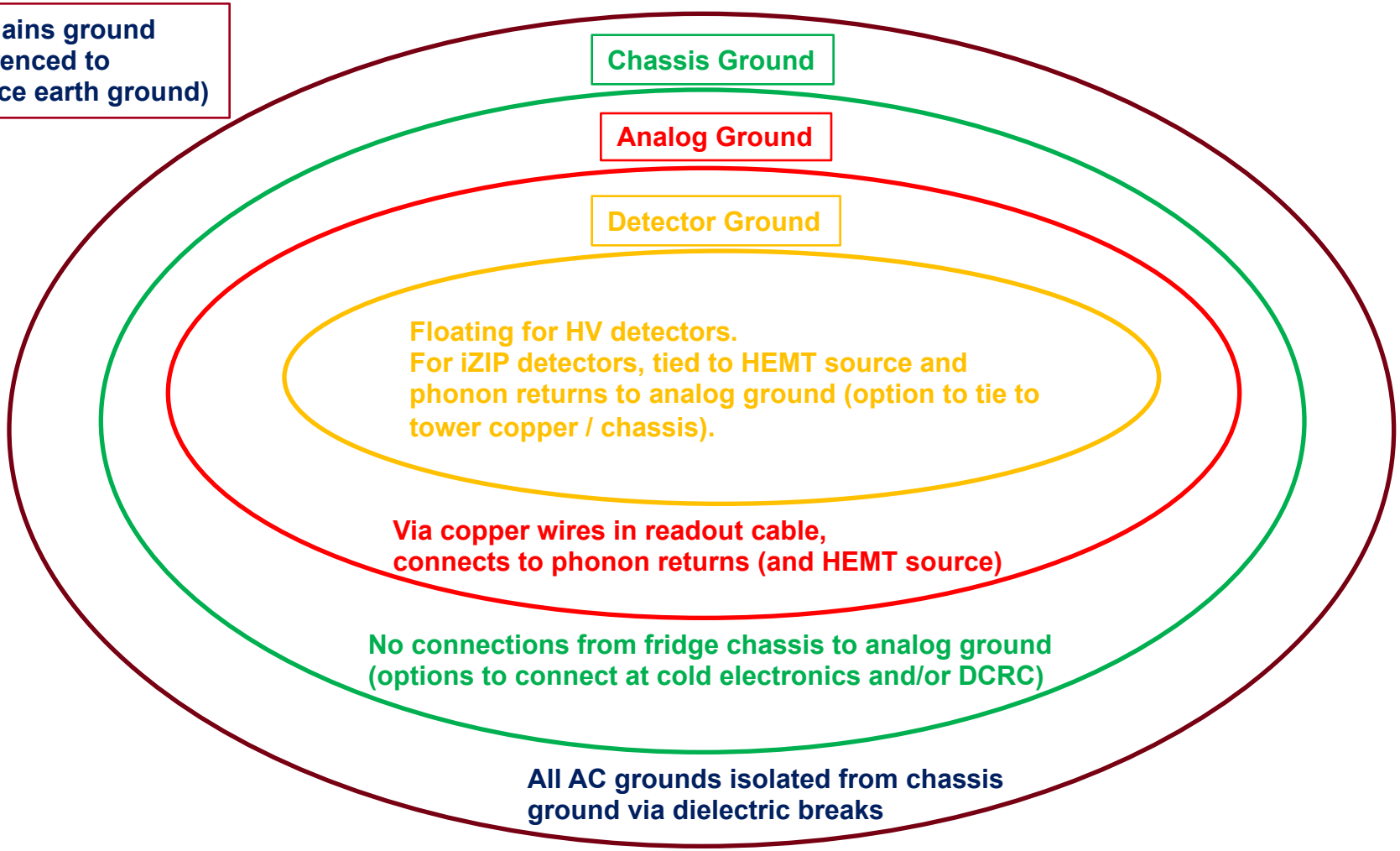
Charge channel circuit design meets noise spec

Verification of design

- Basic funtionality of DCRC and interface to DAQ have been demonstrated
- Phonon channel noise brought down to requirement level operating single DCRC
  - Added filtering in key spots on DCRC
- Successfully ran four synchronized DCRCs, observed pulses
- HV and iZIP VIBs produced and used at SLAC
- DCRCs operated in high-voltage mode
- Successfully ran DCRCs with detector, readout cable, VIB, and prototype cold electronics/wiring, achieved required phonon sensitivity
- First readout cables for test facilities produced and tested

Plan and schedule are resulting in functioning sub-system

Grounding layers



Task force will minimize noise/interference based on testing plan

Grounding considerations

AC ground
- Referenced to “earth” on surface via copper cable
- Tied to cryocoolers, pumps, DAQ racks (POE, HV power, computers), fridge compressors, gas handling, PLC, instrumentation, other infrastructure
- AC power via UPS (verify negligible switching noise, sufficient conditioning of power)
- May need isolation transformers on some equipment

Chassis ground (cryostat)
- Connection to AC ground required, will be filtered
- Forms a shield around detectors and electronics (fridge, SNOBOX cans, e-stem, e-tank)
- Connects to tower copper
- Dialectric breaks between chassis ground and all instrumentation
- Monitor for accidental DC short between AC and chassis grounds

Analog ground
- On DCRC, connects via copper wires in readout cable to phonon-channel returns at detector (and to HEMT source for iZIP detectors)
- Isolated from external power supply and ethernet connection (need to minimize AC coupling)
- Options of no or AC or DC connection to chassis

Detector ground
- For iZIP detectors, options to tie to tower copper at detector or to chassis at DCRC/VIB
- HV detectors always isolated from chassis

Testing at SLAC/CUTE will help solidify grounding scheme, we have flexibility in interconnections between layers

Design maturity

• DCRC: testing plan on track to have final design for production boards by mid-2018

• SDU: design and layout of prototype done; production unit needed Nov 2018; design is straightforward

• VIB: both versions (HV and iZIP) produced and tested; minor modifications are straightforward

• Heat sinks: designs finalized

• Cables: various versions of cables for test facilities and SNOLAB; first ones have been assembled; designs for later versions are similar

Design maturity is sufficient for CD2/3 and beyond

Interfaces with other sub-systems

The Readout Electronics subsystem interfaces with:

- Detector Towers (WBS 1.1)
- Cryogenics (WBS 1.2)
- Data Acquisition and Triggering (WBS 1.6)
- Background Control (WBS 1.7)

Cross-system issues are discussed in regular meetings

Interface control documents have been prepared and posted for each of these interfaces

Interfaces are being addressed for smooth integration

Readout Electronics management

- Monitor schedule progress with monthly reports on accomplishments and updates on progress on tasks

- L2 manager regularly attends:
  - bi-weekly readout electronics meetings
  - weekly meetings for L2 managers
  - bi-weekly DAQ meetings
  - weekly tower technical meetings
  - weekly integration meetings for cross-system issues

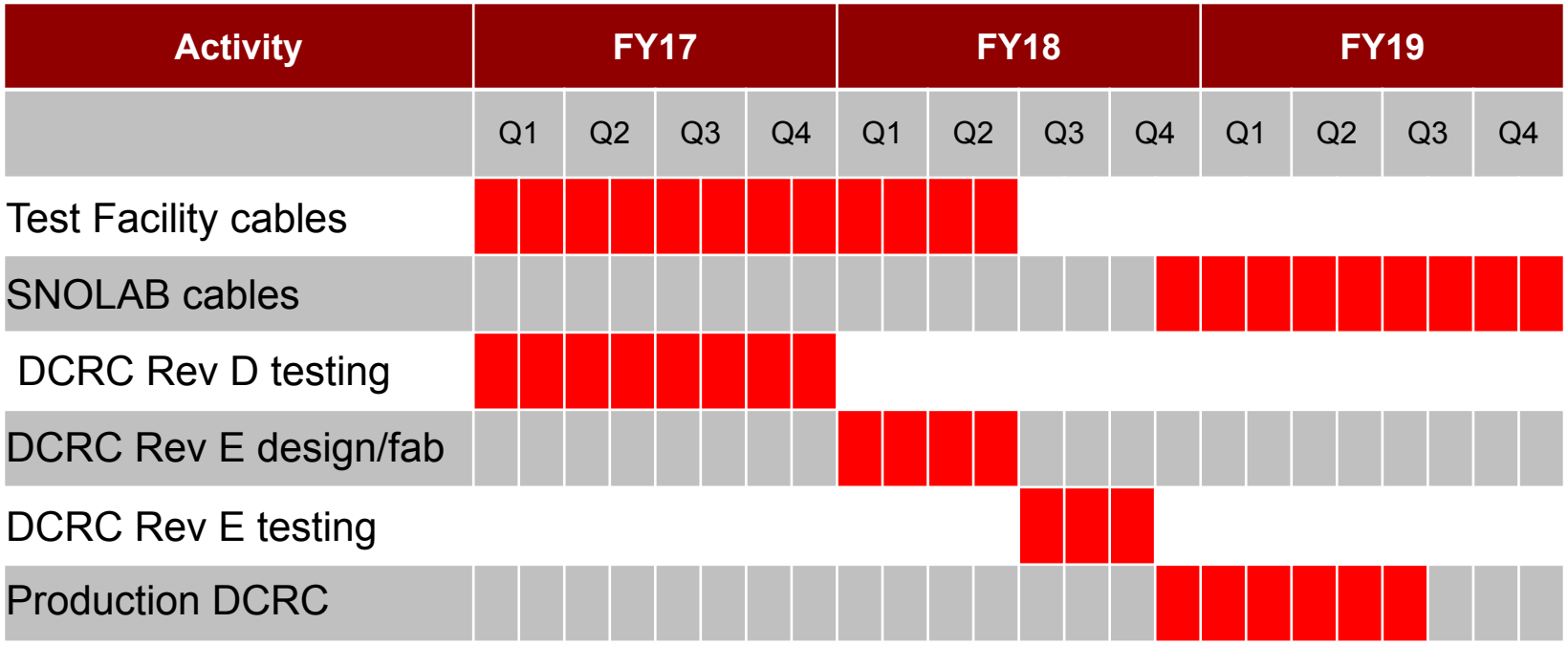
- Close liaison with Project managers

- Coordination with interfacing sub-systems

- Keep track of actual costs vs what has been budgeted

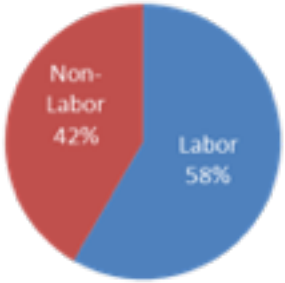
Tools in place to manage schedule and budget

Readout Electronics Schedule

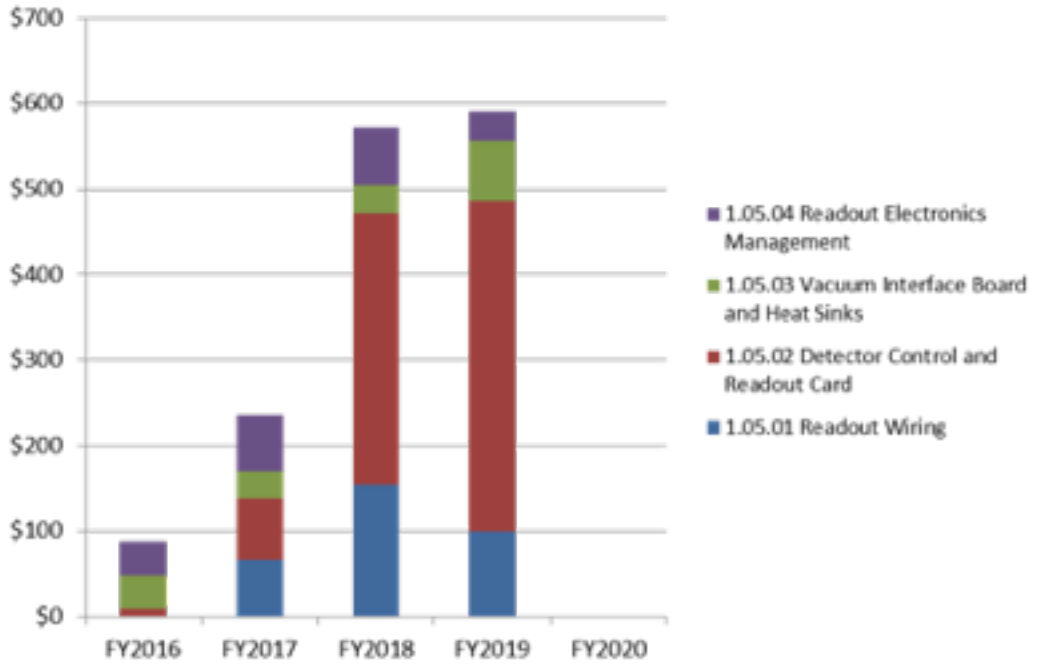


On schedule to meet needs of other sub-systems

Readout electronics cost summary – 1.05



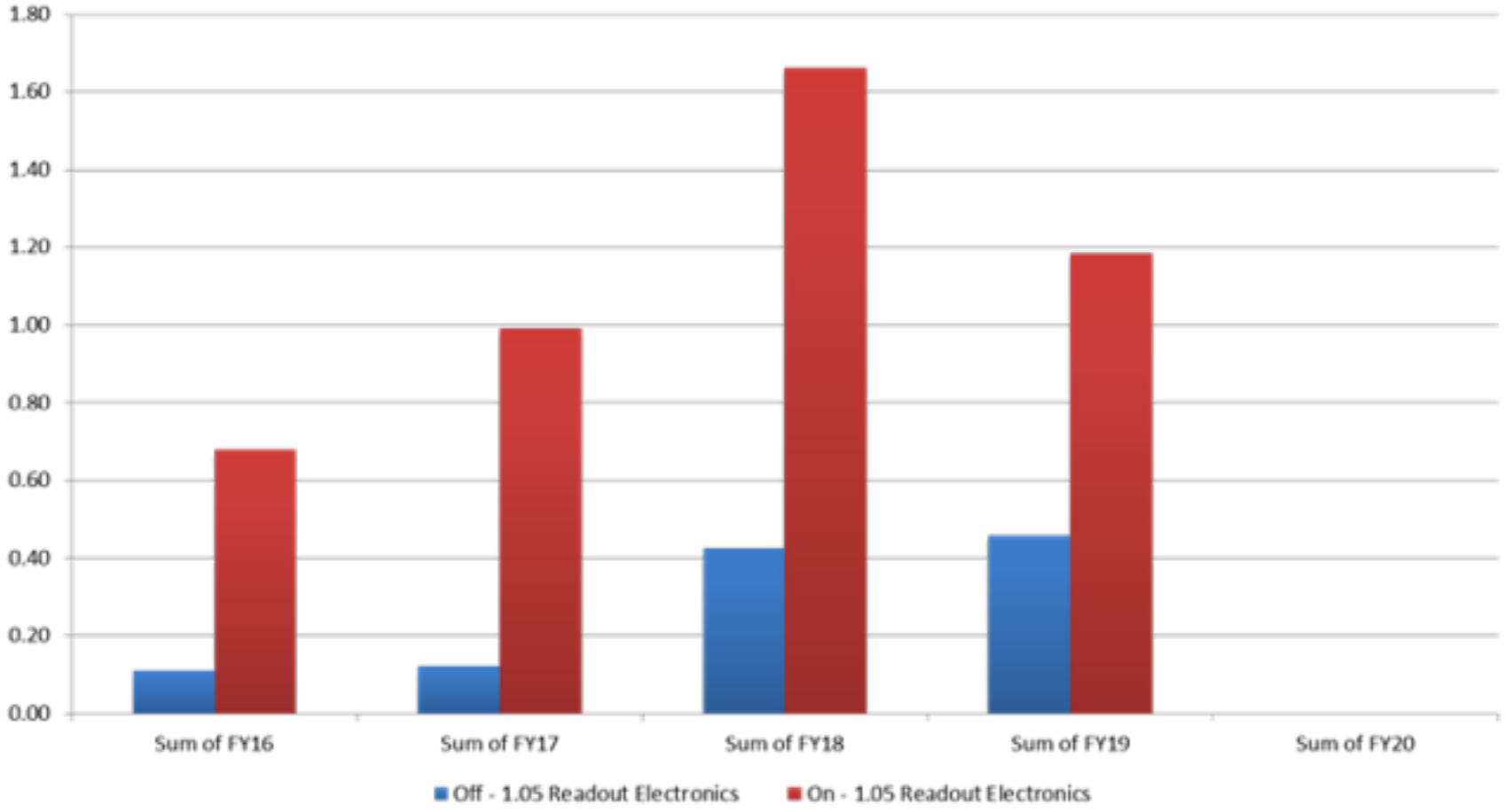
1.05 Readout Electronics	
Resource Type	($K)
Labor	$869
Non-Labor	$619
Total BAC	$1,488



WBS	FY2016	FY2017	FY2018	FY2019	FY2020	Total
1.05.01 Readout Wiring	$0	$67	$155	$99	$0	$321
1.05.02 Detector Control and Readout Card	$9	$72	$316	$387	$0	$785
1.05.03 Vacuum Interface Board and Heat Sinks	$39	$31	$34	$71	$0	$175
1.05.04 Readout Electronics Management	$39	$66	$67	$34	$0	$207
Grand Total	$88	$236	$573	$592	$0	$1,488

Costs are understood and under control

Readout electronics staffing – 1.05 FTE



Manpower is adequate

Responses to Past Review Recommendations

Recommendation from July 2017 status review relating to WBS 1.5:

- **Conduct an end-to-end surface test of a SuperCDMS-SNOLAB HV detector with prototype cables, frontend readout and DAQ. Show that the detector resolution can meet design requirement before CD-2/3.**
- Response:
  - Test conducted at SLAC in Dec 2017
  - Used prototype VFC and HFC, HV detector, readout wiring, VIB, and two DCRCs operated by the DAQ
  - Achieved resolution of ~ 30 eV, better than the required level

Previous review recommendations have been addressed

Risks and Mitigation

Two risks, both rated as low, included in risk registry

One risk worth noting:

If DCRC noise is too high, then detector performance and signal fidelity would be compromised.

Mitigation:

- As per P6 schedule, continue iterative testing plan
- Use prototype and pre-production DCRCs
- With SNOLAB detectors and cold hardware
- Identify dominant noise sources
- Implement revisions to DCRC
- Re-test to find next major sources of noise
- Continue in this fashion
- Arrive at the final design of the production DCRC
- There is enough testing in the plan to mitigate the risk

Improvements from testing so far has reduced this risk from moderate to low

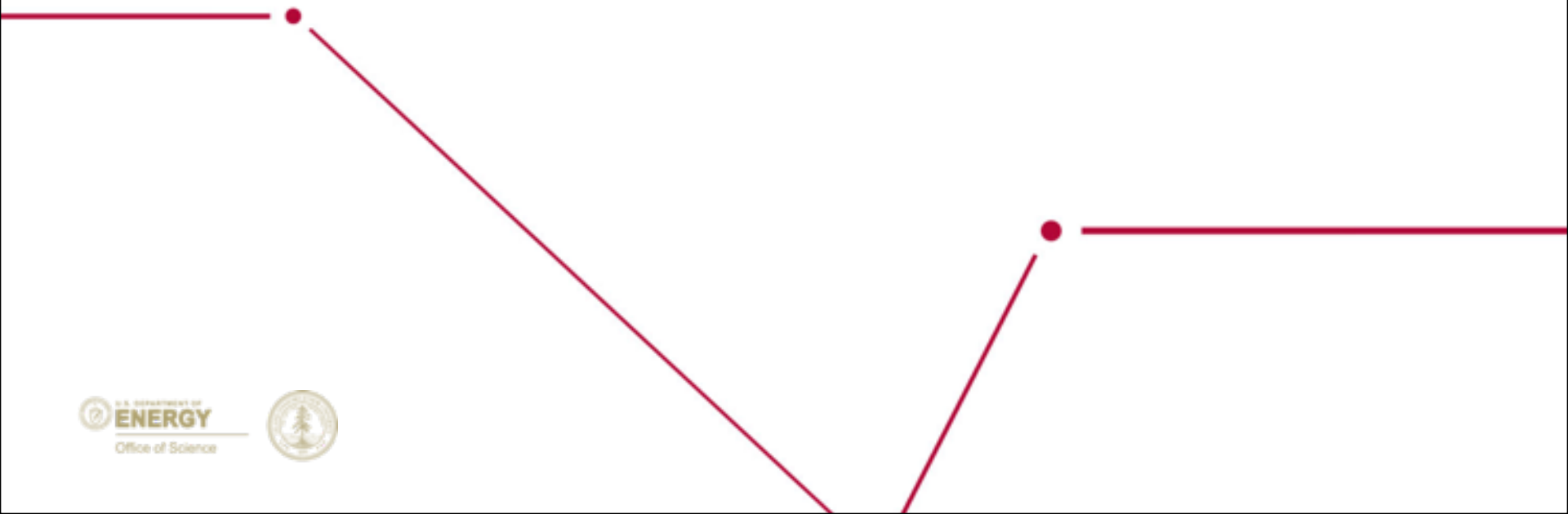
Sound plan for risk mitigation

Summary

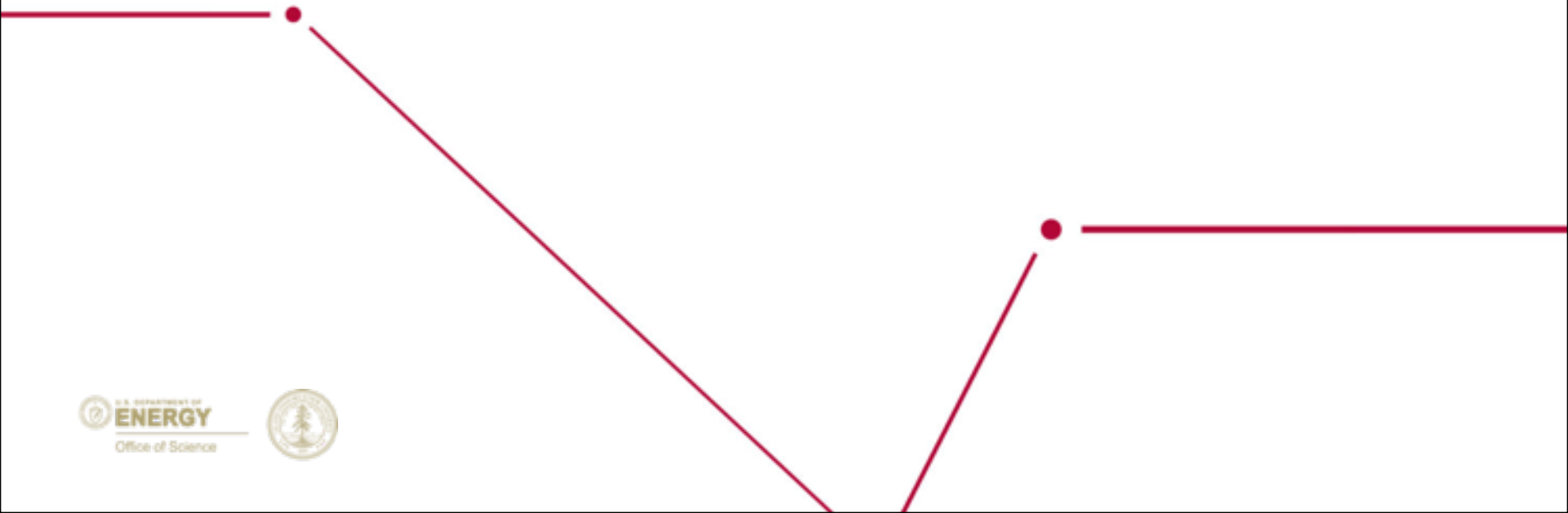
For the Readout Electronics sub-system:

- Specifications have been derived and flow down from science goals
- Organization and manpower are adequate
- Technical designs are sufficiently mature
- Testing plan is in place, progressing, to further improve performance
- Recommendations from previous independent reviews have been addressed
- Risks have been identified, with a sound mitigation plan
- Costs and schedule are understood and are being managed

Questions?



Backup Slides

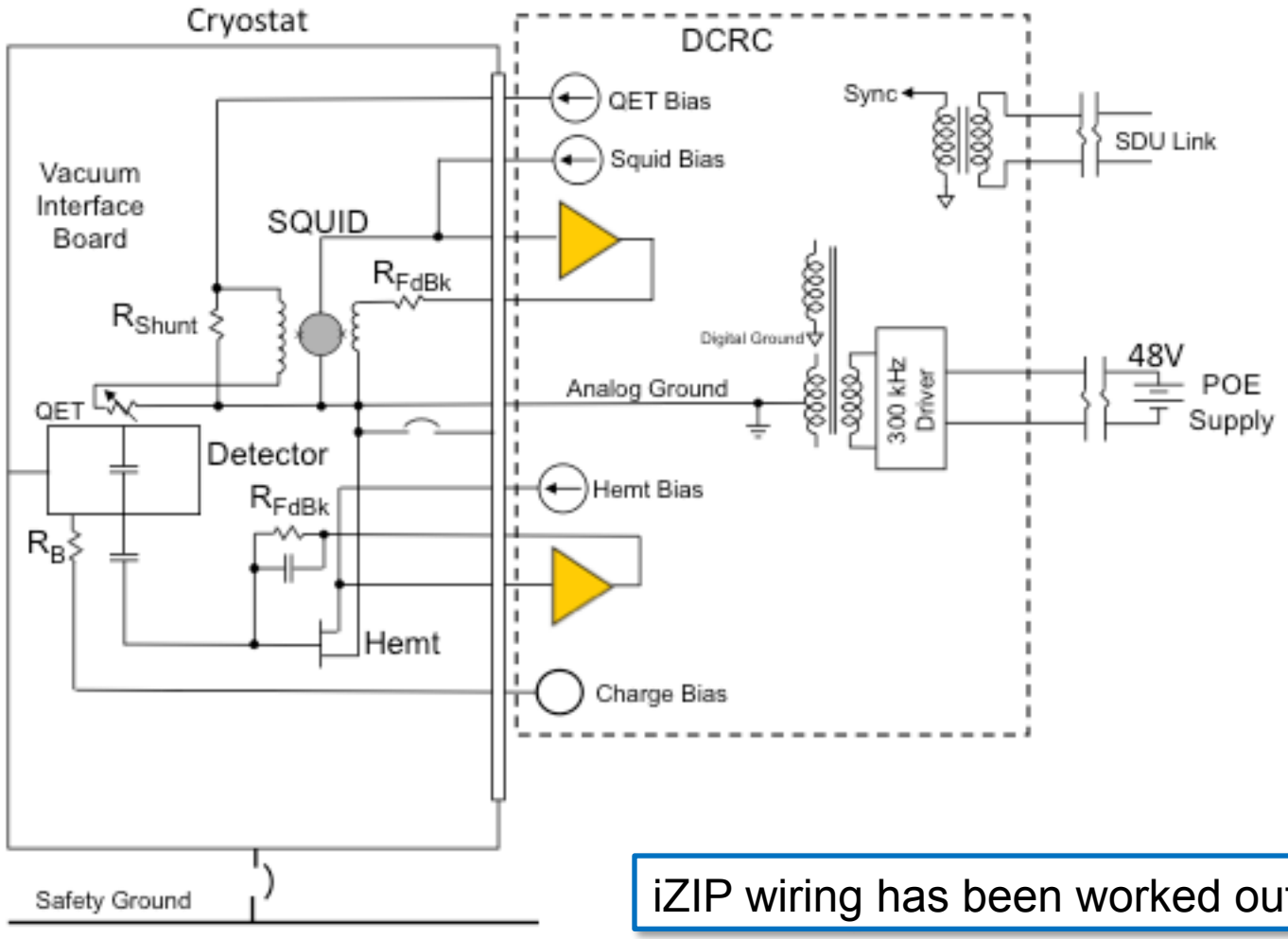


Close-out plan

- Testing of HEMTs and ionization readout at SLAC with DCRC and SNOLAB cold hardware, wiring, and detector
- Implement improvements to DCRC in design of preproduction board (Rev E)
  - Digital-to-analog converters (on a daughter board) will be current-based and have lower noise (daughter board schematic and layout already done)
  - Different (linear) voltage regulators on DCRC will also have lower noise
  - Adjust values of capacitors/resistors to improve filtering
- Testing of all aspects of operation of DCRC Rev E at SLAC using DAQ
- Revise DCRC based on test results, as needed, as per P6 schedule
- Test of full complement of production DCRCs, POE, HV power and SDU with DAQ at TRIUMF
- Creation of a procedure for the replacement of the DCRC board due to failures
- Remote firmware and software download over ethernet

Testing plan in place and doable

Grounding – iZIP (with options)



iZIP wiring has been worked out

AC ground

What's tied to it?

- Everything in utility drift B3 (cryocoolers, pumps,…)
- DAQ racks, including "power over Ethernet" and HV power supplies
- Fridge compressors and gas handling rack
- PLC and all fridge instrumentation
- Cleanroom, crane, computers and all other infrastructure in drifts C3 and B2

Issues

- There is no good 'earth' reference in the underground laboratory at SNOLAB. The AC grounds are referenced to 'earth' via a copper cable to the surface.
- Mining equipment produces a significant "feature" on AC mains, currently at about 3.75 kHZ
- Lab lighting, radios, Ethernet, and other devices also radiate "features" that may appear on AC mains. This may come from our own equipment (e.g. in the DAQ racks)
- SuperCDMS AC power will come from the large UPS, which may condition it, but could also add switching noise
- We might need isolation transformers for some key equipment like the DCRC POE and HV

Chassis ground

What's tied to it?

- SNOLAB requires a ground connection but it would have to be filtered
  - Saturable inductor to deal with possibility of DCRC HV fault
  - This could perhaps be built into the HV supply return
- The chassis ground is a shield around the detectors and electronics.
- The detector tower copper is connected via the SNOBOX cans and fridge

Issues

- The fridge and cryogenics design has dielectric breaks for all instrumentation from chassis ground, although these do not prevent capacitive coupling
- May want to have a monitor that detects any DC connections from chassis ground to AC ground and sends an alarm. Looking for GigaOhm isolation so perhaps a nanoammeter and battery?

Analog ground

What's tied to it?

- Analog portion of DCRCs and phonon return lines for iZIP detectors

Issues

- Analog ground is DC-isolated from the power supply grounds on the DCRCs
- Electronics design unit at FNAL is trying to make sure there isn't too much power supply noise coupling to analog ground
- Option for AC connection to chassis ground

Detector ground

What's tied to it?

- Tower copper and the analog ground of the HEMT amplifier for the iZIP detectors

Issues

- Tower copper is tied to chassis ground via the SNOBOX and fridge
- The iZIP detector towers will have the option of connecting analog and detector ground at the cold electronics end. This would then be a star ground.
- The DCRCs will have the option of tying analog ground to chassis ground. This would then be a star ground.
  - We probably would not want to do both of these options

Detector grounding plans

HV Detectors

- By design, HV readout is fully isolated from tower mechanics and the SNOBOX
- Use low noise power supply to power DCRC analog ground to desired bias voltage relative to the vacuum vessel
- Use high impedance TES bias supplies to keep constant bias current in the event there is a difference between detector and DCRC ground potentials
- Probably should do a test of the candidate power supply to make sure that power supply noise isn't an issue

iZIP Detectors

- Likely the only way to prevent noise injection on the HEMT input is to utilize a robust local ground at the detector
- Tie analog ground of HEMT amplifier to the tower mechanics
  - Make sure all tower stages are at the same potential
  - Tie phonon returns to the analog ground of the HEMT amplifier

All of these measures have been implemented in tower electronics

- We have a dedicated grounding screw that if installed shorts the analog ground to the detector housing for iZIP detectors only
- The vertical flex has a NbTi trace connecting all tower stages to housing
- A NbTi trace on the vertical flex connects TES returns to the HEMT source

Detector grounding plans

Biggest concern is that the analog ground wires running between the detector and the DCRC could serve as a ground return path for non-detector signals

- Resistance in ground wires would create varying potential difference between DCRC ground and detector ground resulting in noise pickup

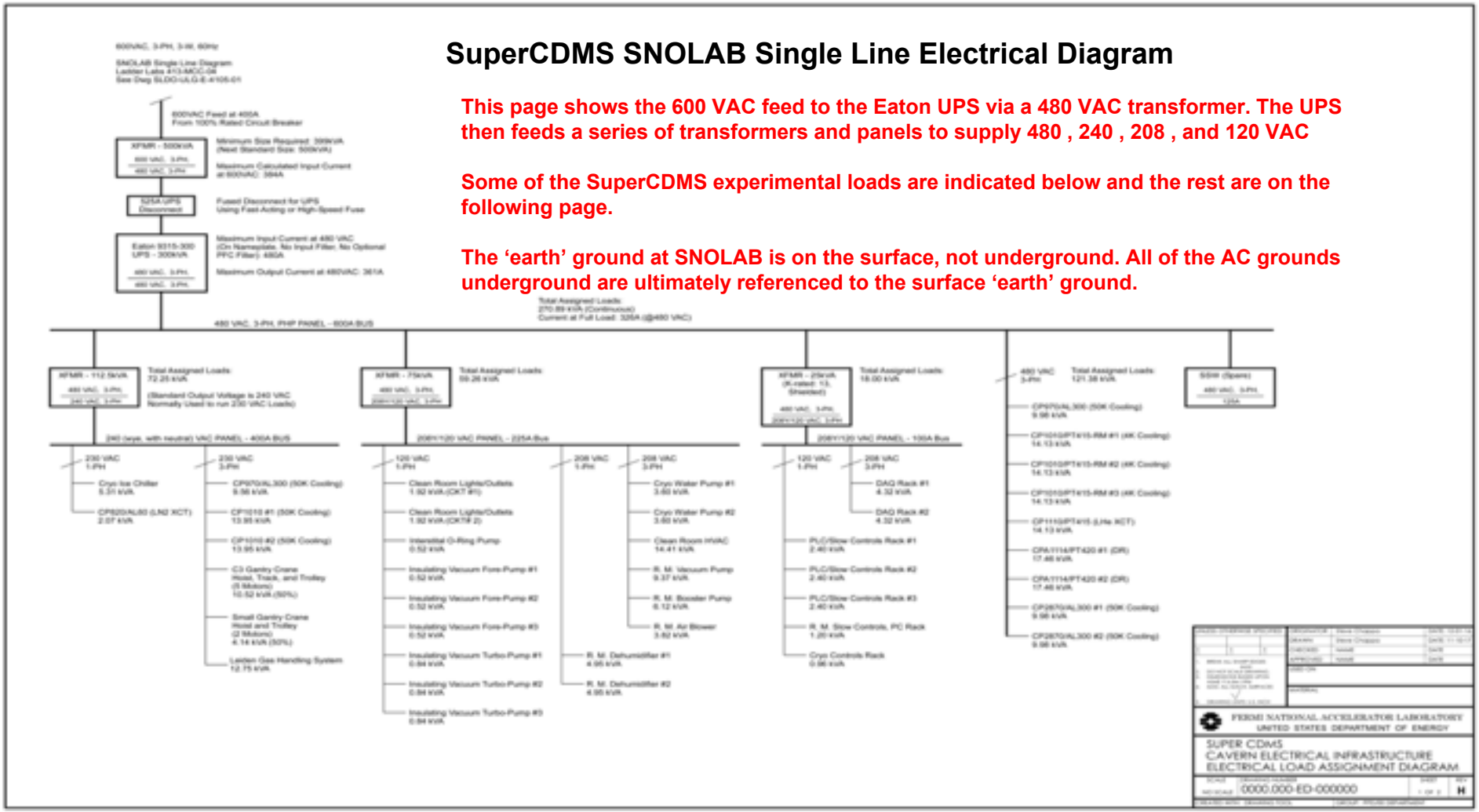
Easiest way to avoid shared currents is to isolate DCRC

- Avoid low impedance connection of analog ground of iZIP DCRC to cryostat or other external ground
- Leave possibility for jumpers to tie DCRC to cryostat

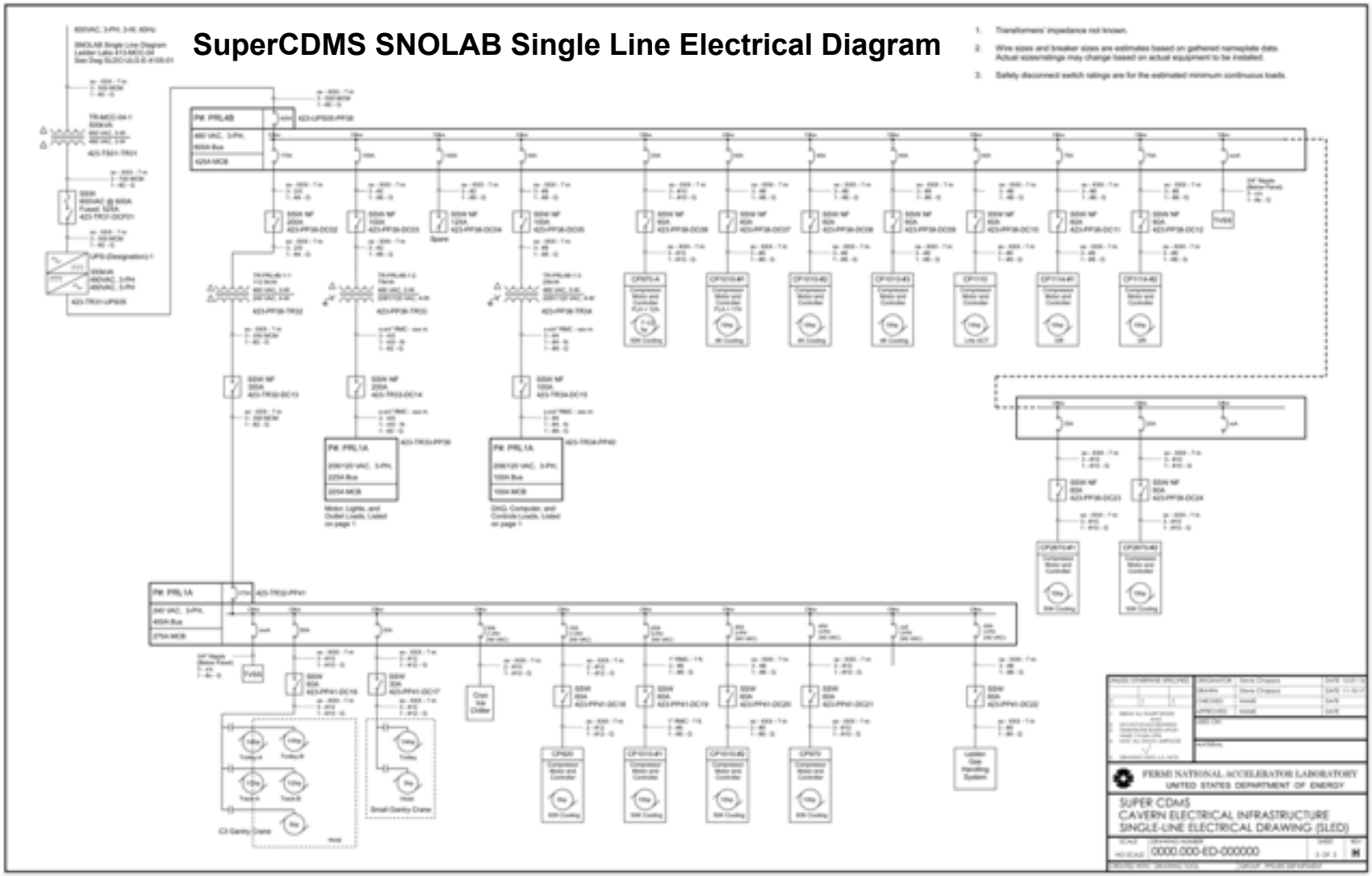
We should also strive to ensure that the cryostat is not used as a ground return path (direct or capacitive) for infrastructure

- Isolate cryostat from floor, lab AC, instrumentation
- Have a way to easily test isolation

SNOLAB electrical loads



SNOLAB electrical loads



Planned internal reviews

- Preproduction DCRC fabrication readiness review
- Production DCRC fabrication readiness review
- Production signal distribution unit fabrication readiness review
- SNOLAB 4K – 300K readout cable fabrication review
- SNOLAB Tower – 4K readout cable fabrication review
- Production vacuum interface boards fabrication reviews

Internal review plan is in place

DCRC technical details

Phonon channels:
- 14-bit digitizers, 10 Msps
- sampling rate = 625 ksps (after down-conversion by 16)

Charge channels:
- 16-bit digitizers, 5 Msps
- sampling rate = 2.5 Msps (after down-conversion by 2)

Data buffer:
- 128M x 16 LPDDRAM
- 200 MHz
- (fast enough to simultaneously supply data to the Ethernet link and accept data streaming from the ADCs)
- 6.71-second buffer for digitized signals

ARM microcontroller, 160 MHz

100 Mbit TCP/IP, up to 8 MB/s for each DCRC

DCRC power:
- multi-port mid-span injectors
- POE+ standard (30 W)
- low-noise, 24 ports, 48 V, 600 W supply

Further technical details

HV detector bias:

- units from iSEG (Model EHS 8401x106)
- 8 channels each
- 100-V maximum range
- 50-pA current monitor resolution
- positive or negative polarity

SDU:

- distributes FM fequency reference to all DCRCs
- broadcasts synchronous messages to all DCRCs
- makes clocks on SDU and DCRCs coherent
- dgital section utilizes architcture much like that of DCRC

Milestones

WBS 1.05

- L4_MS_1.05: Ready for Status Review – done, review held July 2017
- L4_MS_1.05: Ready for CD-2/3 – done, review in progress
- L4_MS_1.05: Ready for CD-4 – 31 July 2019
- L4_MS_1.05: Production DCRC modified after test at TRIUMF – June 2019