

1 module has 8 ASICs in 4x2 arrangement:



← 2 more rows of pixels here

↕ 36 pixel gap to lower module

↗ 2 more columns of pixels in each gap

1 module
Readout: 1024x512
Physical: $(1024+6) \times (512+2) = 1030 \times 514$

2 modules
Readout: 1024x512 twice
Physical: $(1024+6) \times ((512+2) \times 2 + 36) = 1030 \times 1064$