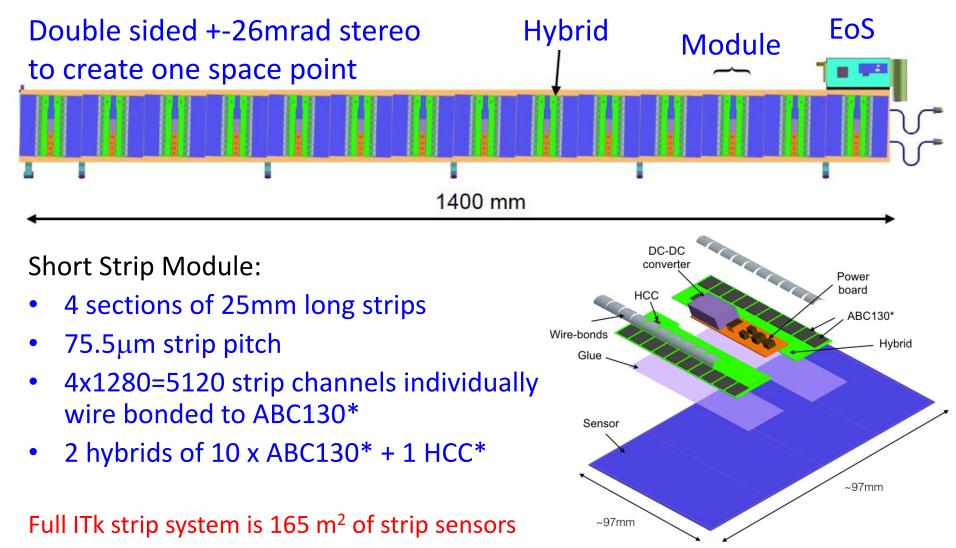
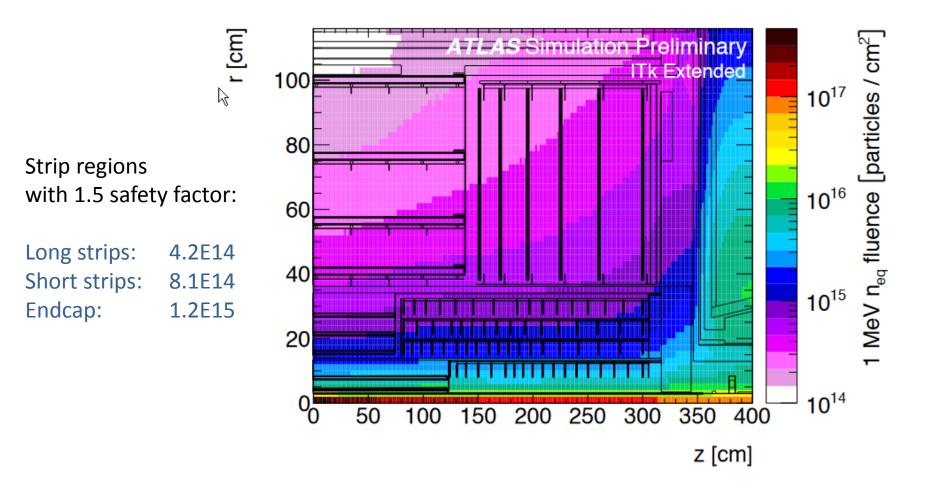


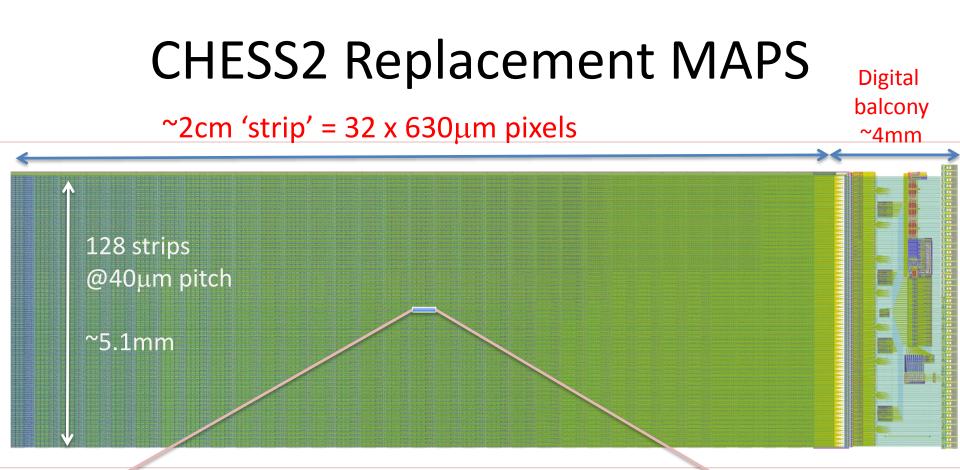
ITk Strip Stave Baseline

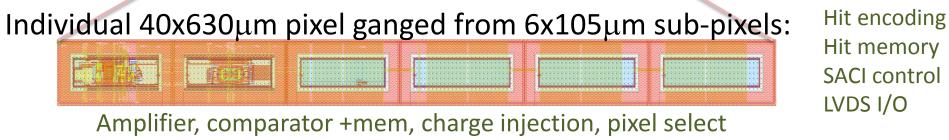


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ITk Radiation Dose

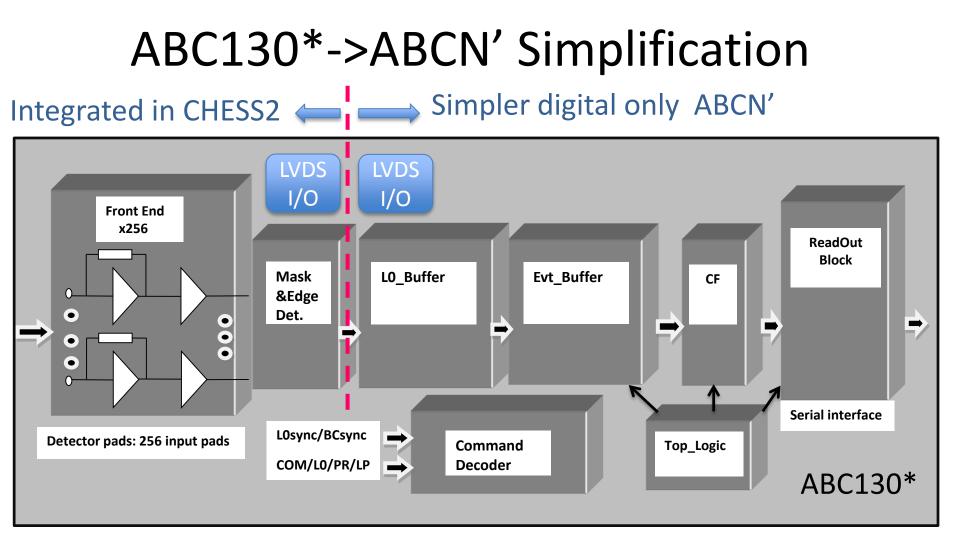






More CHESS2 design details in <u>Piero Caragiulo's talk at SLAC/Stanford upgrade meeting</u>

1/20/2017

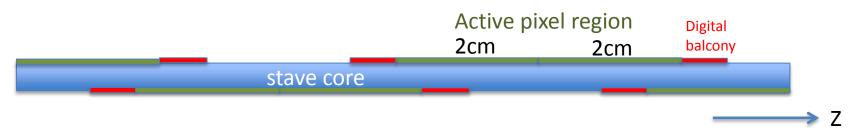


- Eliminating 256 analog strip wire bonds / ABC*
- Adding 2x28 LVDS digital lines at CHESS2->ABCN' interface
- Reuse HCC* and rest of strip readout chain and stave infrastructure

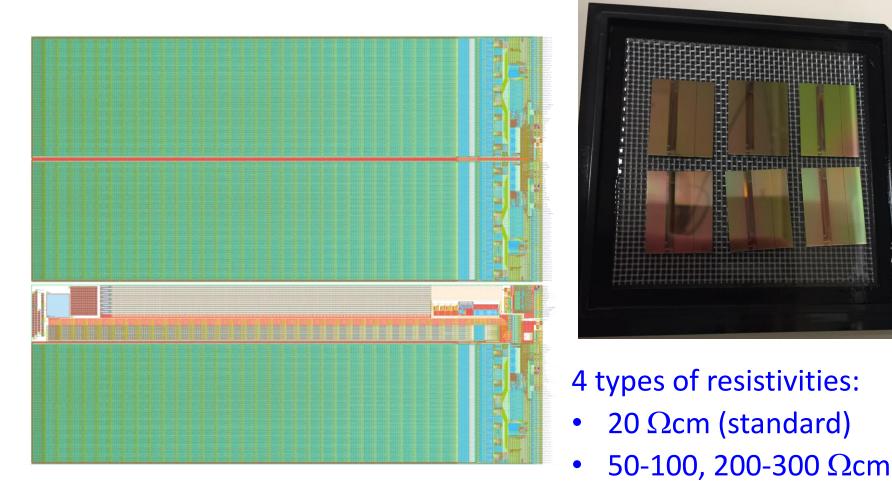
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CHESS2 based 'module'

- 2x20 CHESS2 chips form a $10cm(\phi)x4cm(z)$ module
- Each module has 2x2560 strips covered by 10 (?) ABCN'+1 HCC
- One side (2D pixel) establishes 3D space point by itself
- Still double sided stave to stagger modules up and down to give space to digital balcony, but much more relaxed spacing
- spatial resolution:
 - R ϕ : one 40 μ m pitch space point trading for two strip hits of 75.5 μ m pitch (/V2 ~ 53 μ m) is still slightly better
 - Z: 630 μ m pixel much better than 52mrad stereo over 2.5cm.
- Pattern recognition: 40x630µm pixel much more superior



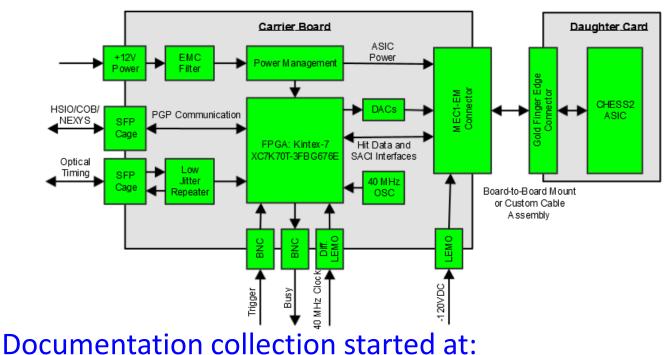
CHESS2 Chips



• 600-2000 Ωcm

CHESS 2 Test Readout

- Analog test boards on test structures: Oxford
 - Some loaded analog daughter cards already went for irradiation at CERN PS (proton) and Ljubljana (neutron)
- Full digital array readout: SLAC



https://twiki.cern.ch/twiki/bin/view/Atlas/CHESSStripTestChip

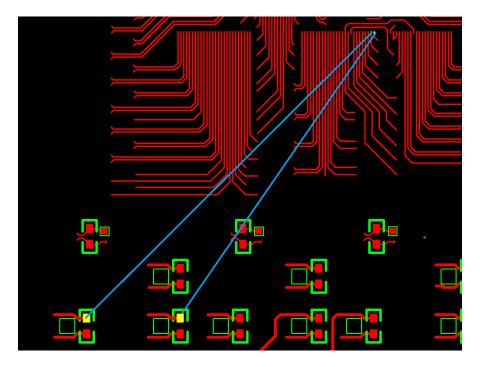
Digital Test Daughter Boards



- First panel of 10 PCBs at SLAC
- Allow no-soldering option for wire bonds only – no hold up for release after irradiation
- Somewhat trickier layout (10 layers) and more expensive than original expectation due to many fine pitched wire bond pads.

Design details for daughter + carrier are documented at: https://confluence.slac.stanford.edu/display/AIRTRACK/ATLAS%3A+CHESS2

Digital Test Daughter Board



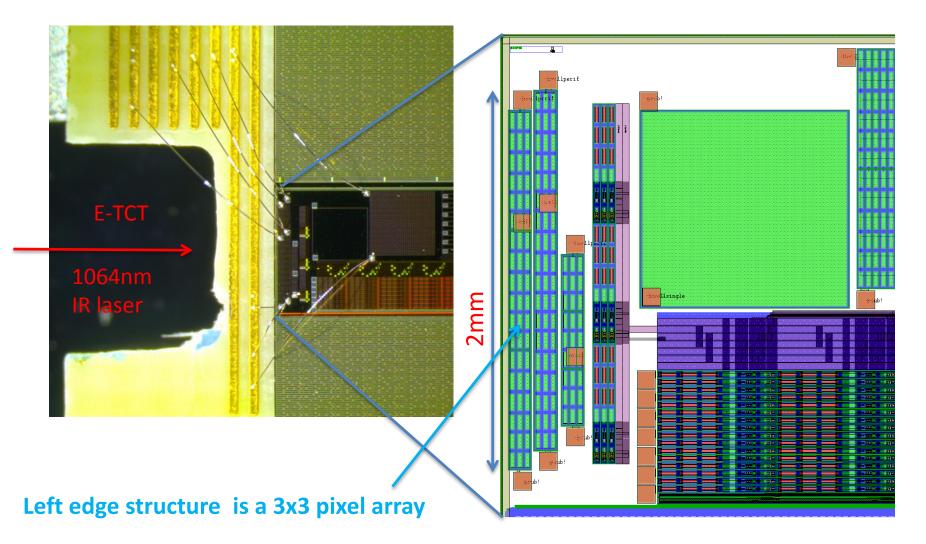
- First panel of 10 at SLAC
- One bug spotted: BL/BLR mislabelled on SamTec connector as BR/BRL caused no connect at layout.
- Two regular wire soldering patch on daughter card
- Carrier board still OK
- 3 patched daughter boards back from wire bonding @ Amtech
- 4 more at UCSC to load for further checks

Digital Carrier Board

- First few loaded boards at SLAC
- Checks by Larry so far:
 - Power regulation OK
 - Can program FPGA and PROM with J-tag. PROM booting OK.
 - Can R/W registers via SFP port with PGP link.
- More standalone tests to come:
 - SPI DAC
 - Triggering
 - External clock
 - Data collection

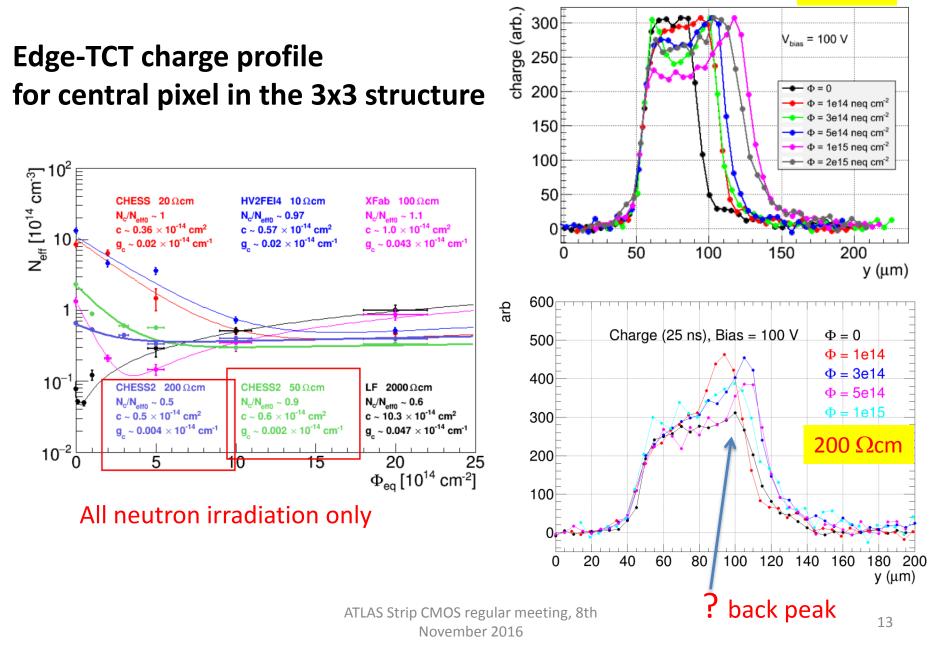
- Further tests next week with loaded daughter board:
 - o SACI interface
 - HV bias
 - o ASIC's parallel LVDS data tuning
- Martin integrating carrier board with HSIO2 readout

Edge TCT analog tests @Ljubljana

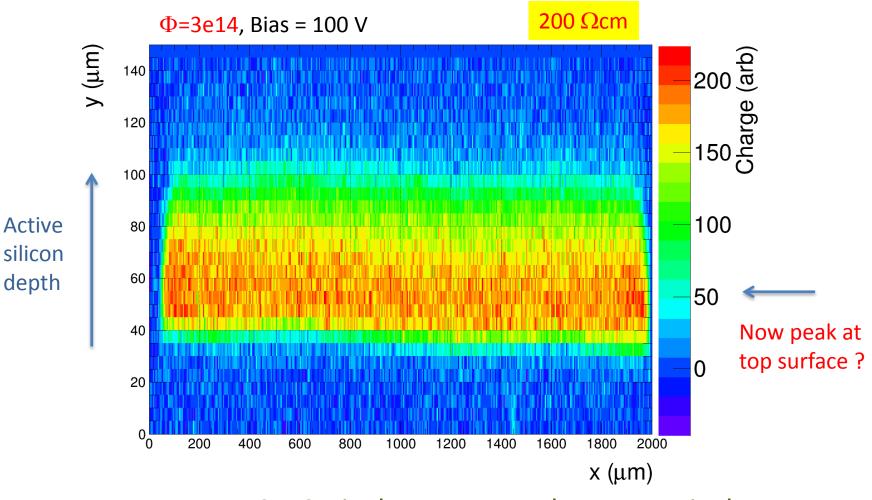


Edge TCT analog tests @Ljubljana





E-TCT



scan across 3 x 3 pixels => no gaps between pixels

Summary

- Testing for CHESS2 started in earnest
- Many puzzling effects to understand on behavior after irradiation
- All teste activities has local components:
 - SLAC designed the digital test system
 - Edge-TCT in group C Labs going online after laser safety certification
 - Cosmic telescope next and test beam later

Welcome more participants !