

# Look Closely Studies

Pelle

Trigger timing

SVT Clock Phase

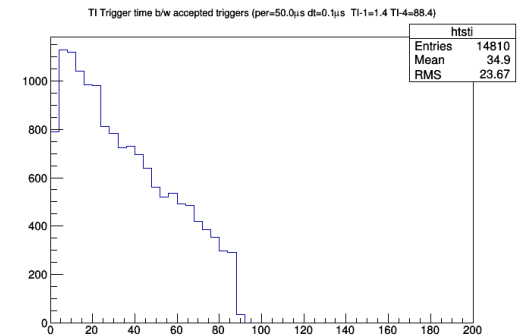
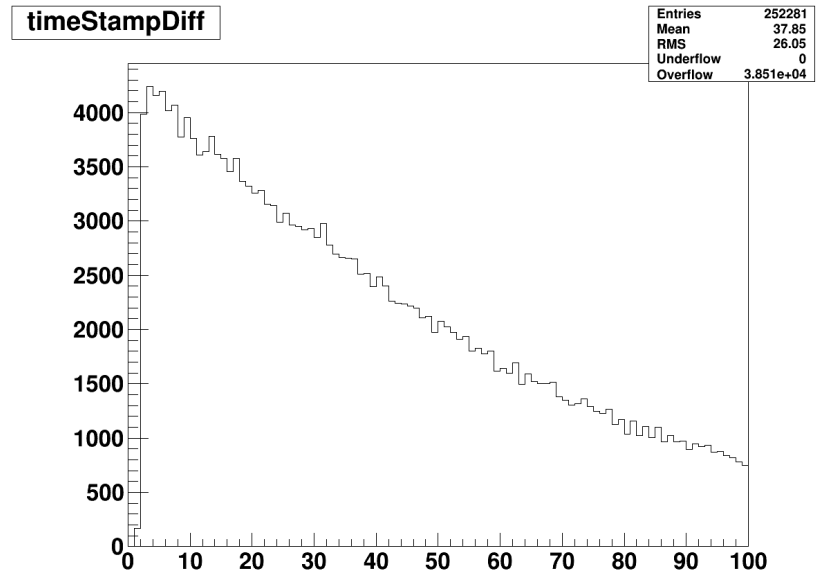
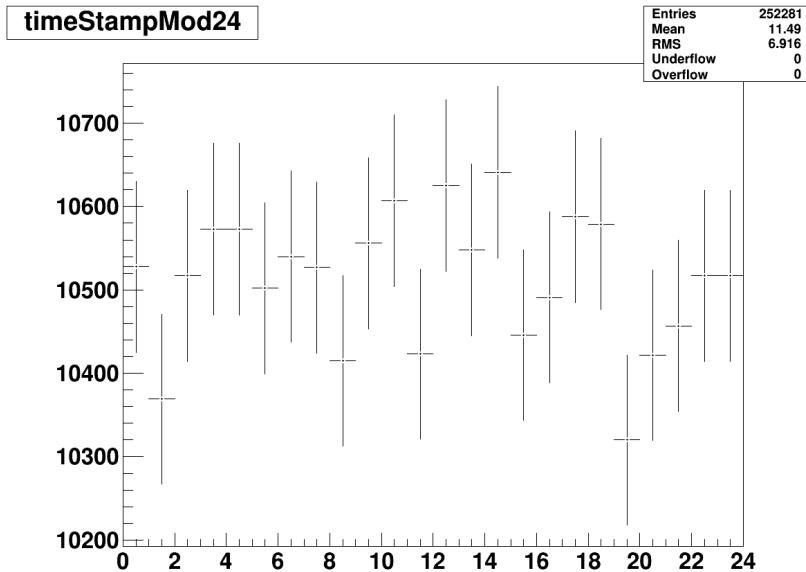
SVT Occupancy vs. time structure of triggers

Look at 5796 (next to last prod. Run at 0.5mm) here.  
Others look similar (for the stuff I checked).

# Trigger Timing

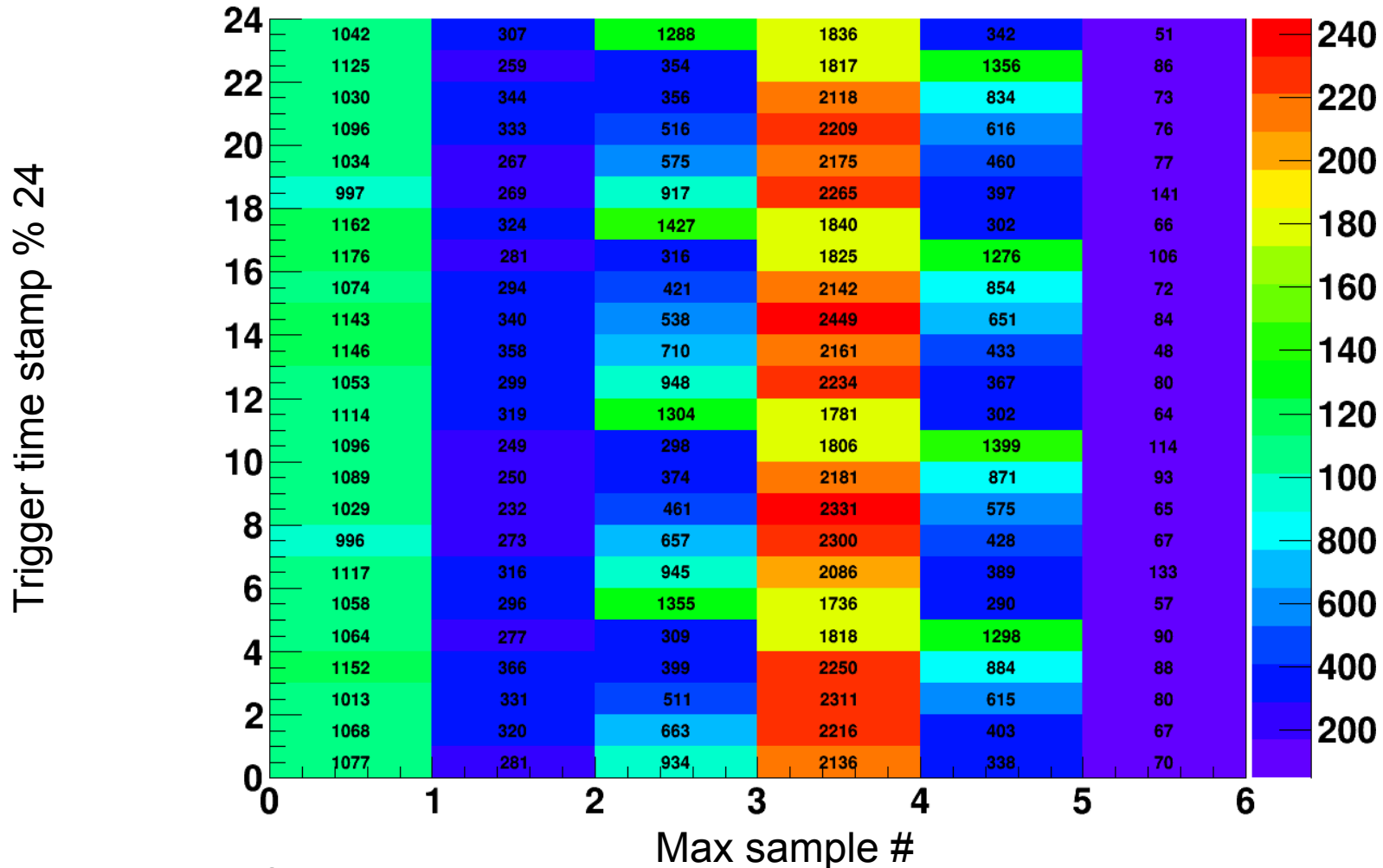
Uniform distribution of triggers in 1 APV clock cycle. Good.

Time between triggers.



# SVT Timing – Max Sample Phase Dependence

maxSamplePhaseMod24-rce-0-fpga-8-hyb-3

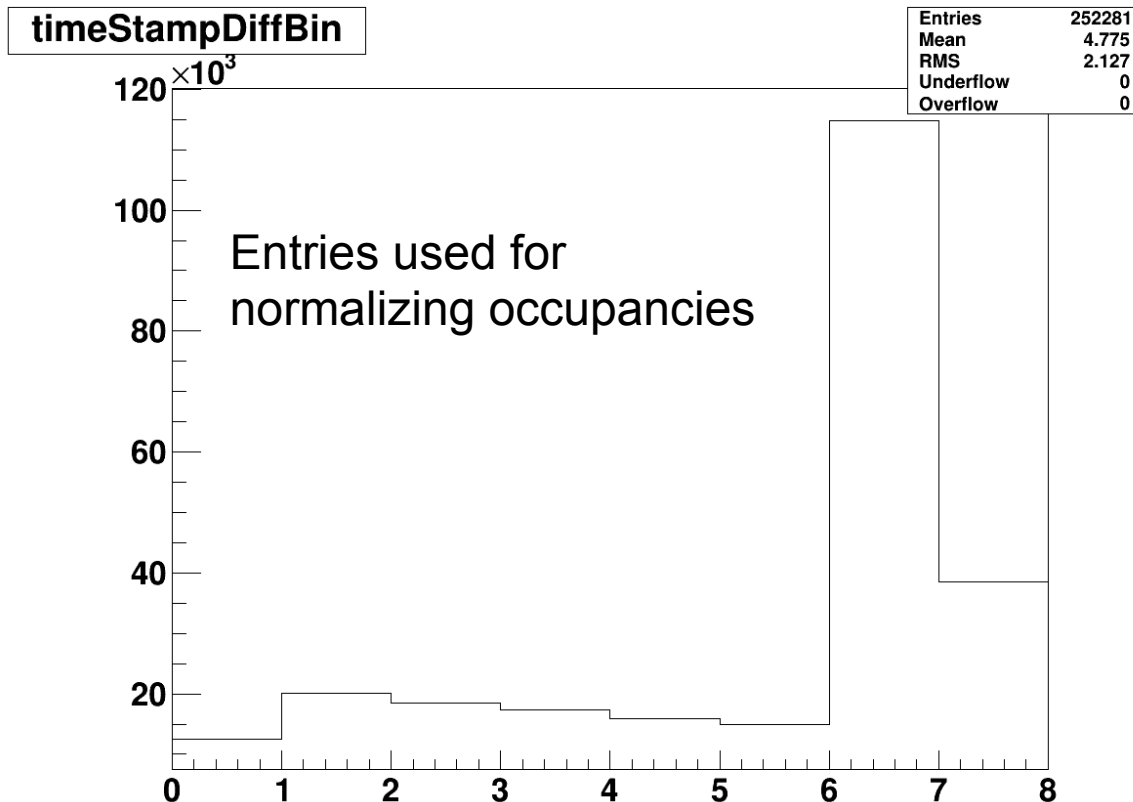


Similar pattern for all sensors



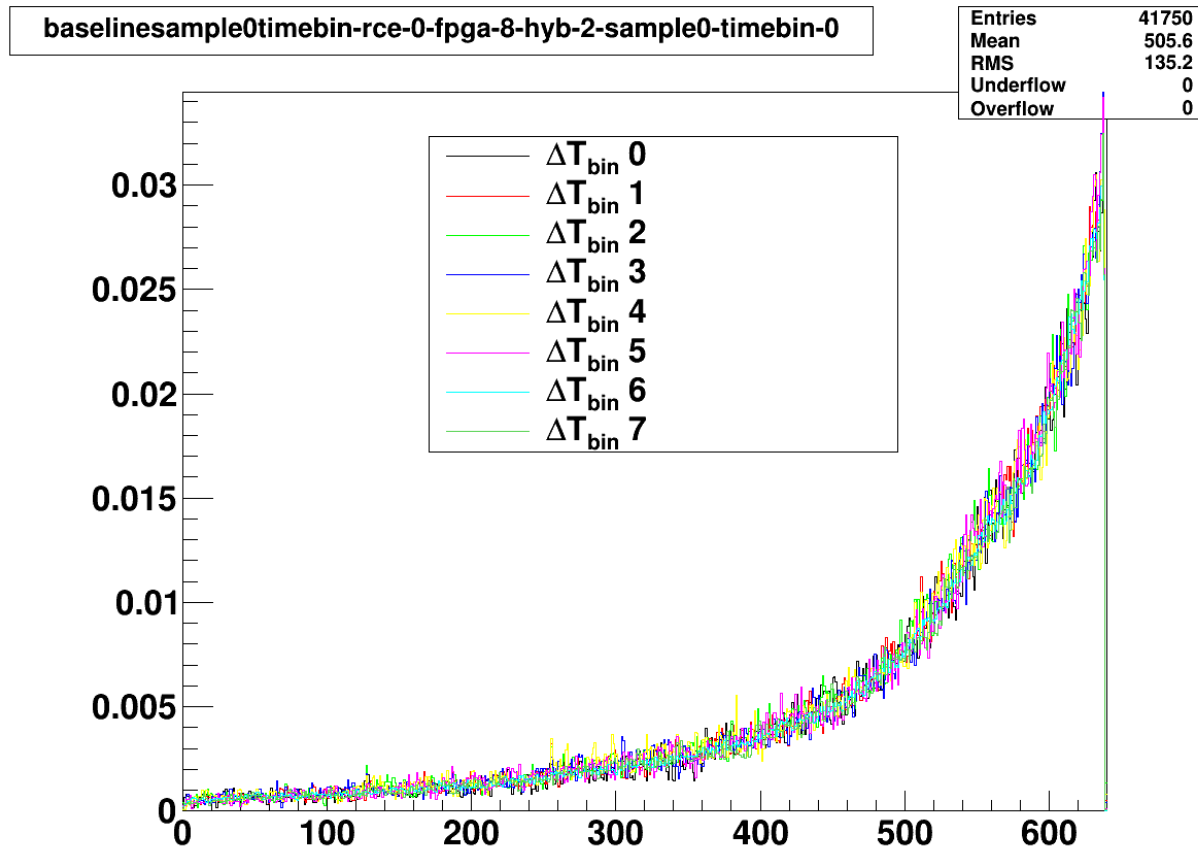
# Delta Trigger Time

Time b/w triggers binning in the following is {0,5,10,15,20,25,30,100} in us

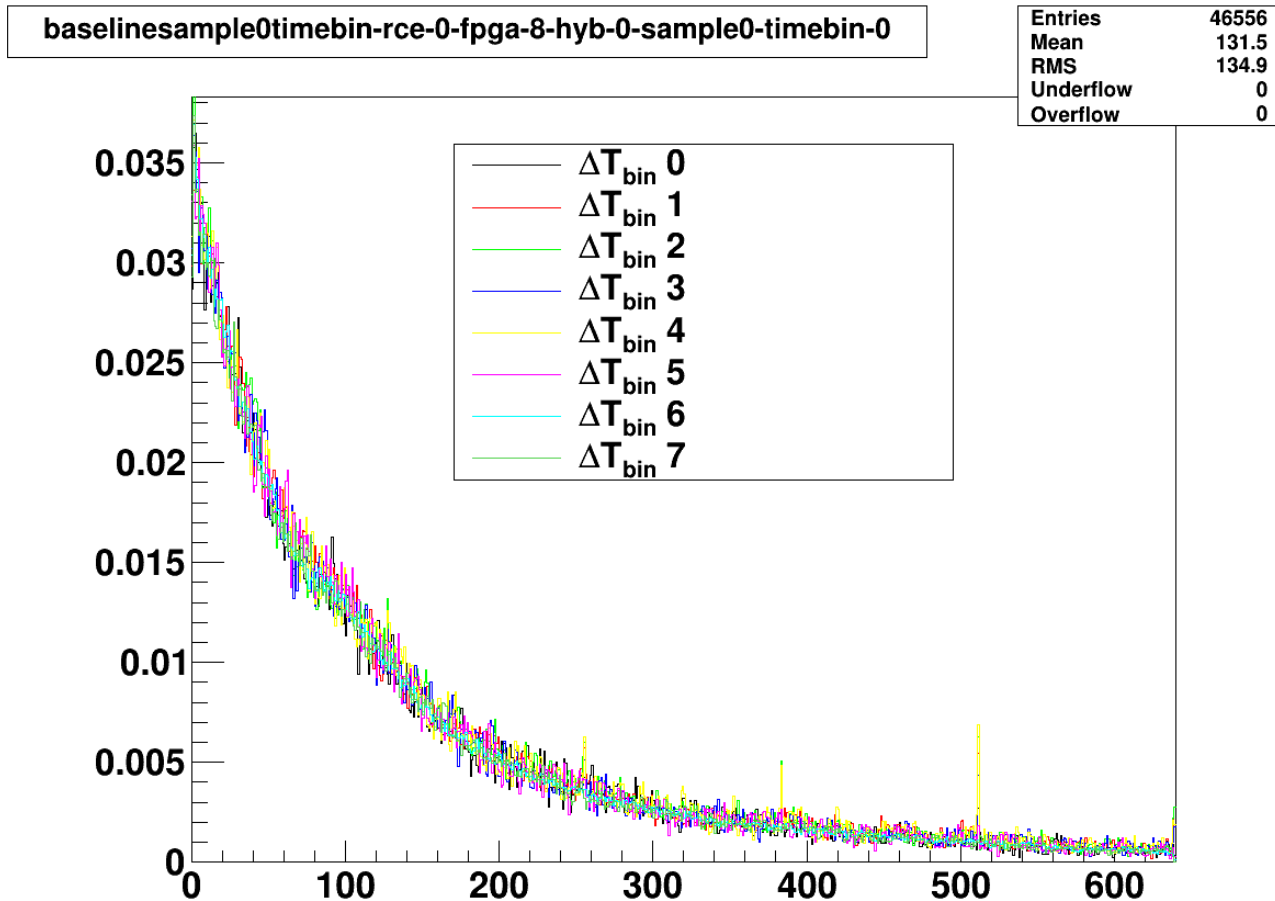


# Occupancy

Good example

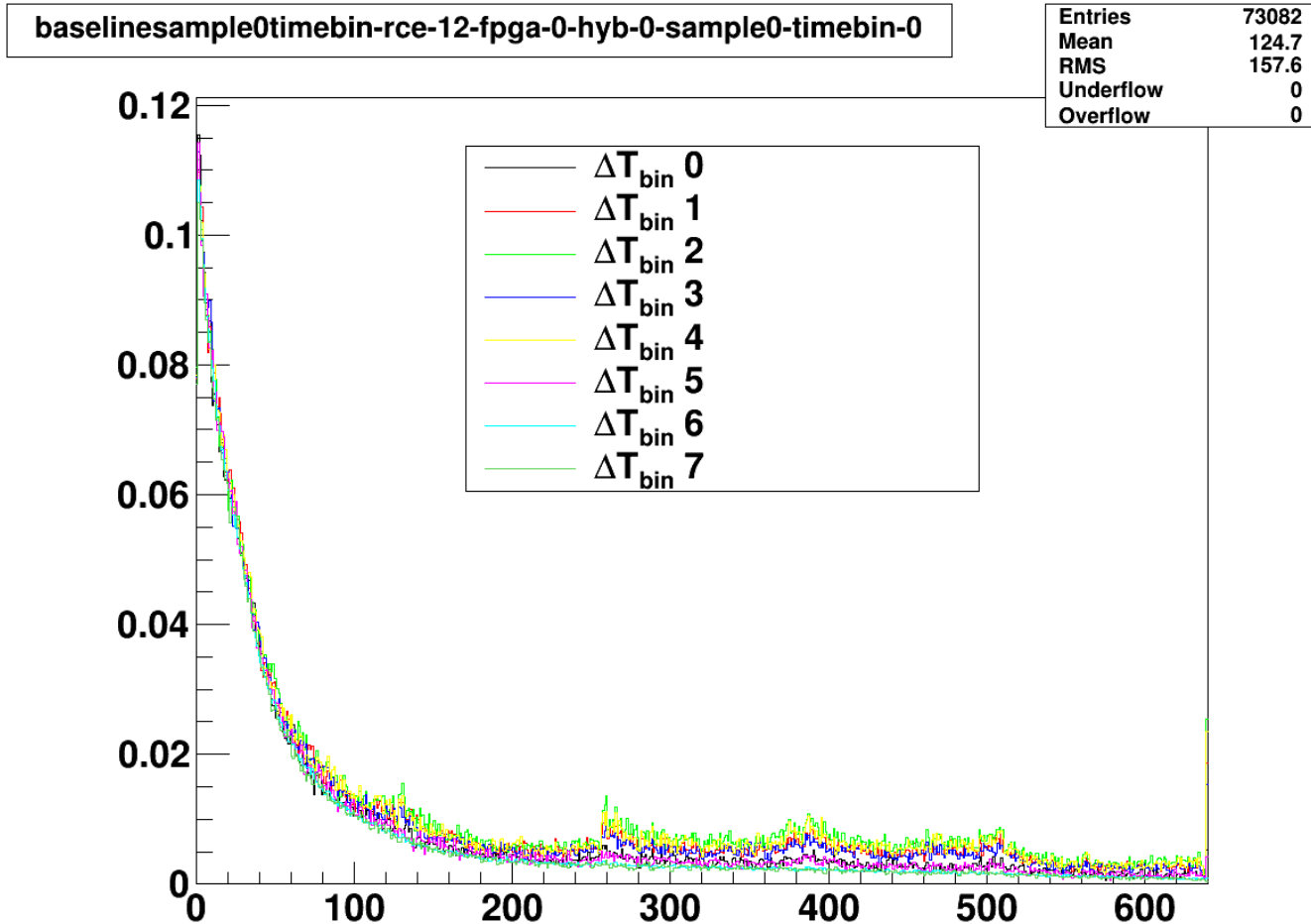


Pretty good example

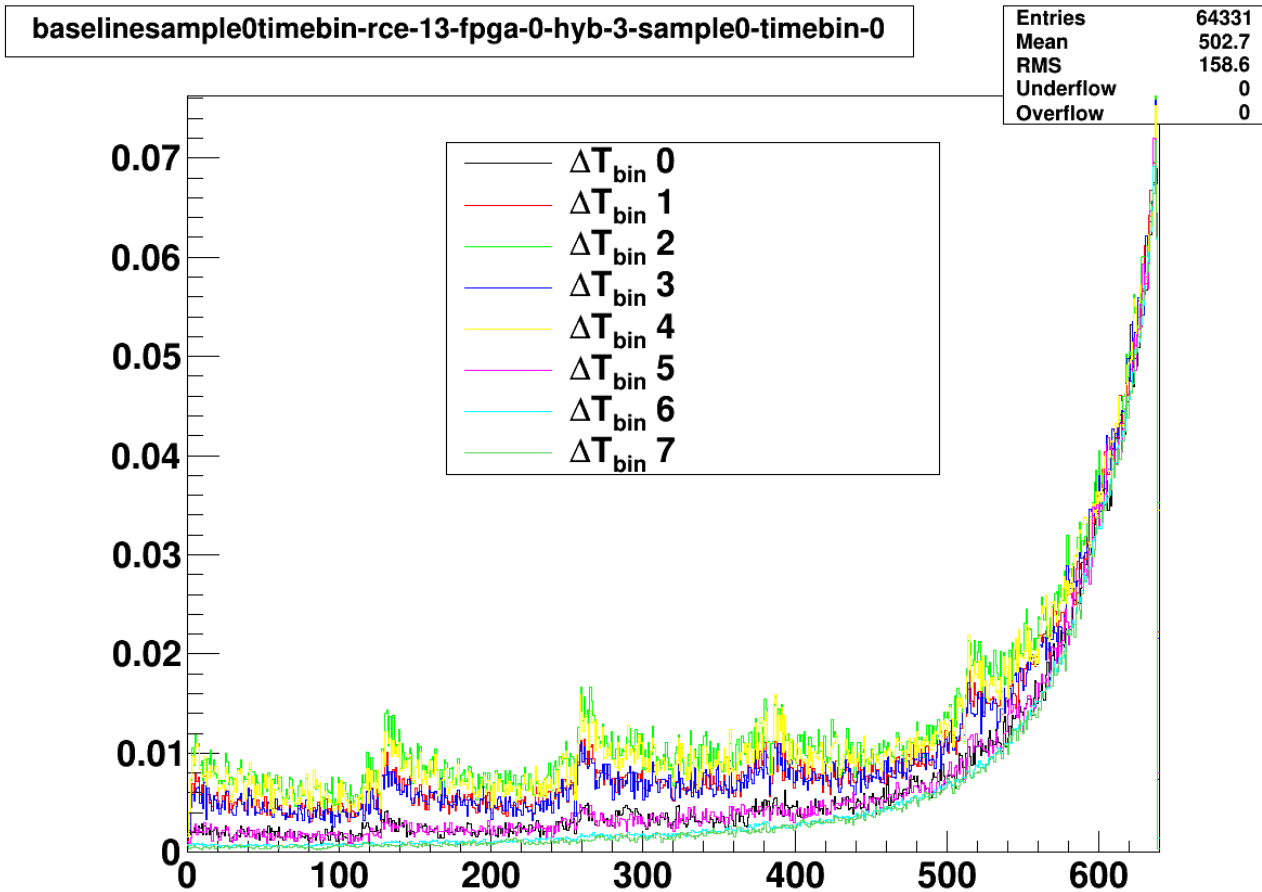




## Worse example



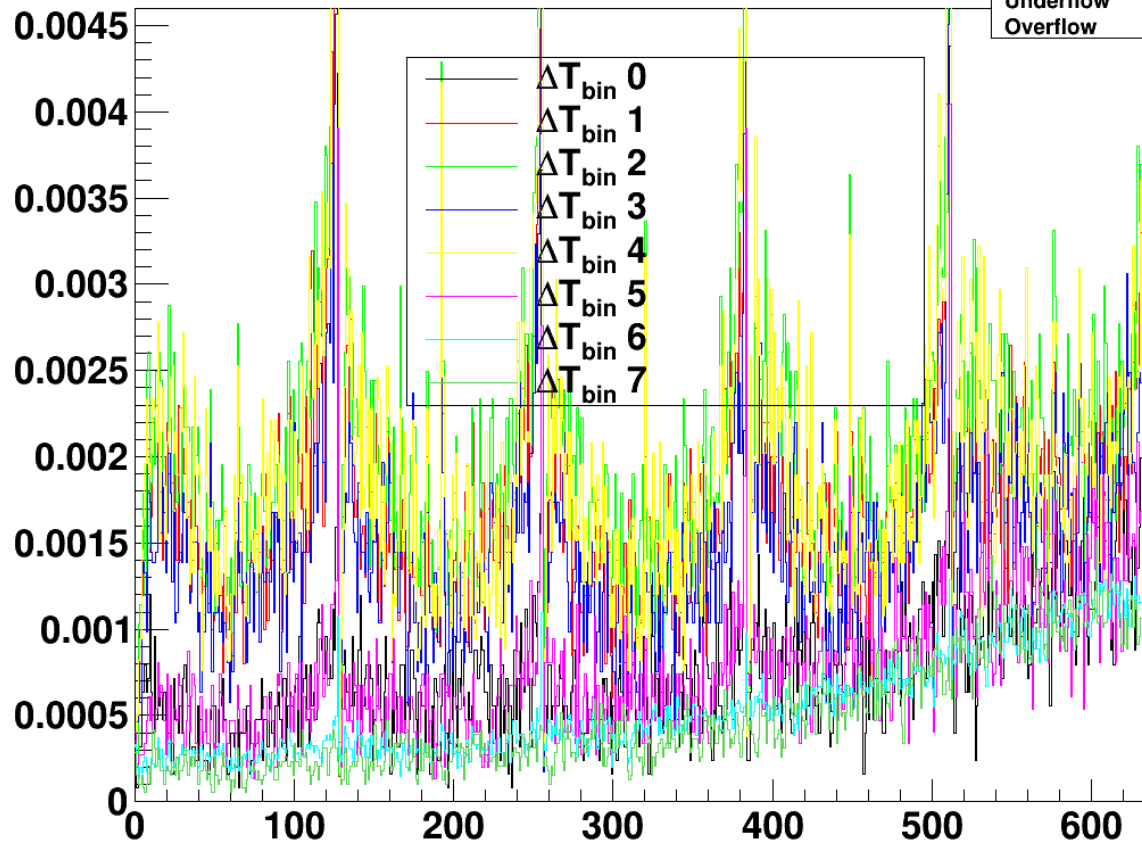
## Worse example



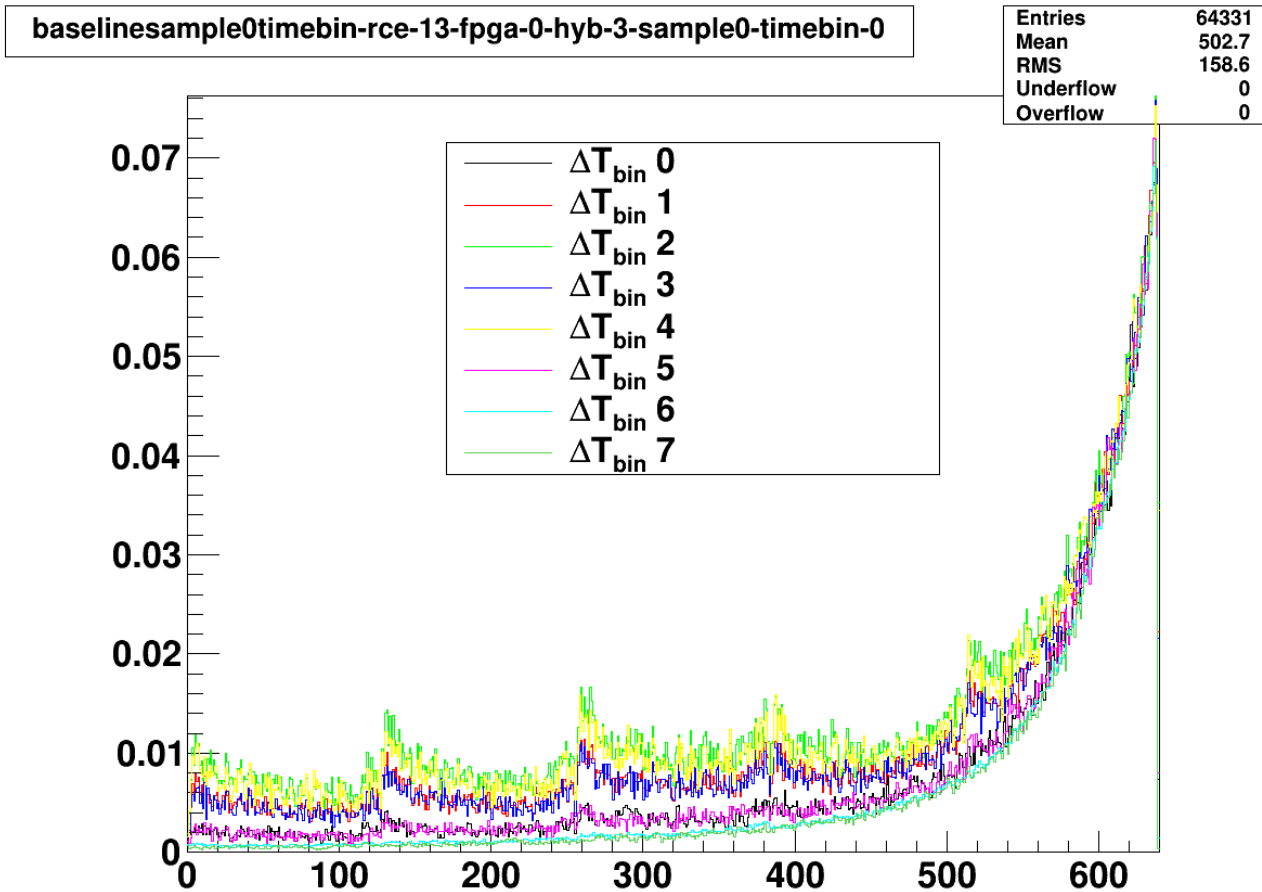
## Worse example

baselinesample0timebin-rce-2-fpga-7-hyb-1-sample0-timebin-0

Entries	6392
Mean	378.3
RMS	186.2
Underflow	0
Overflow	0



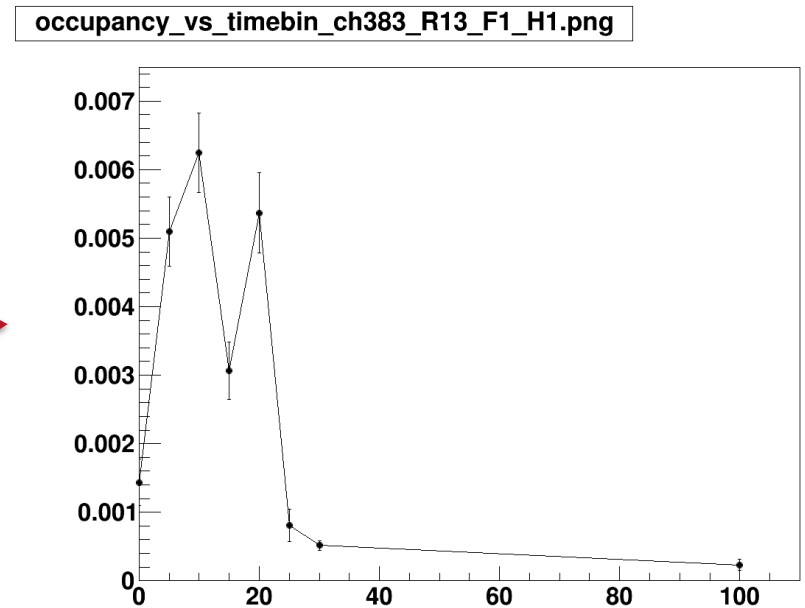
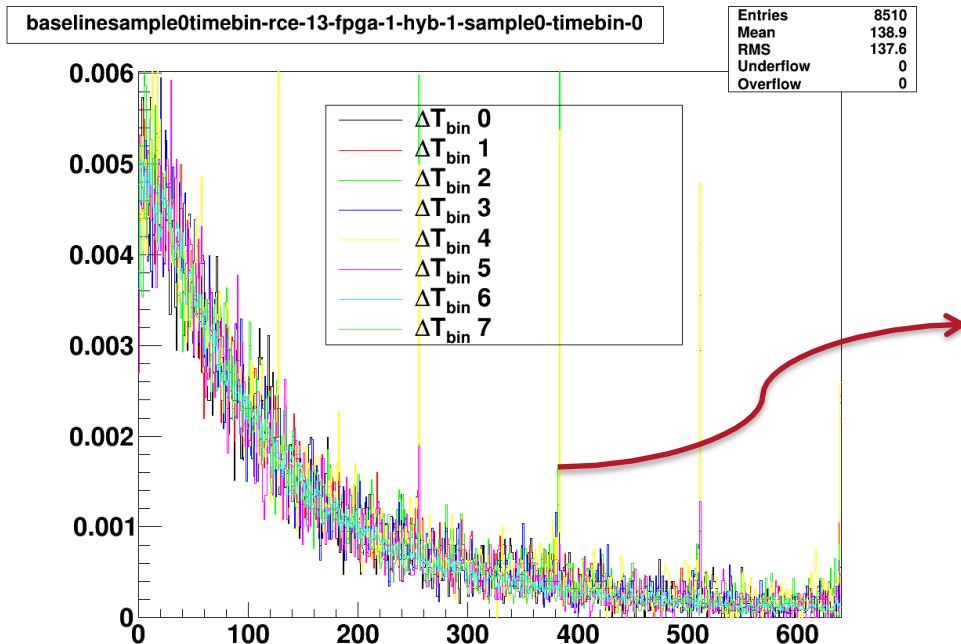
## Worse example



# Delta Trigger Time Evolution of Occupancy

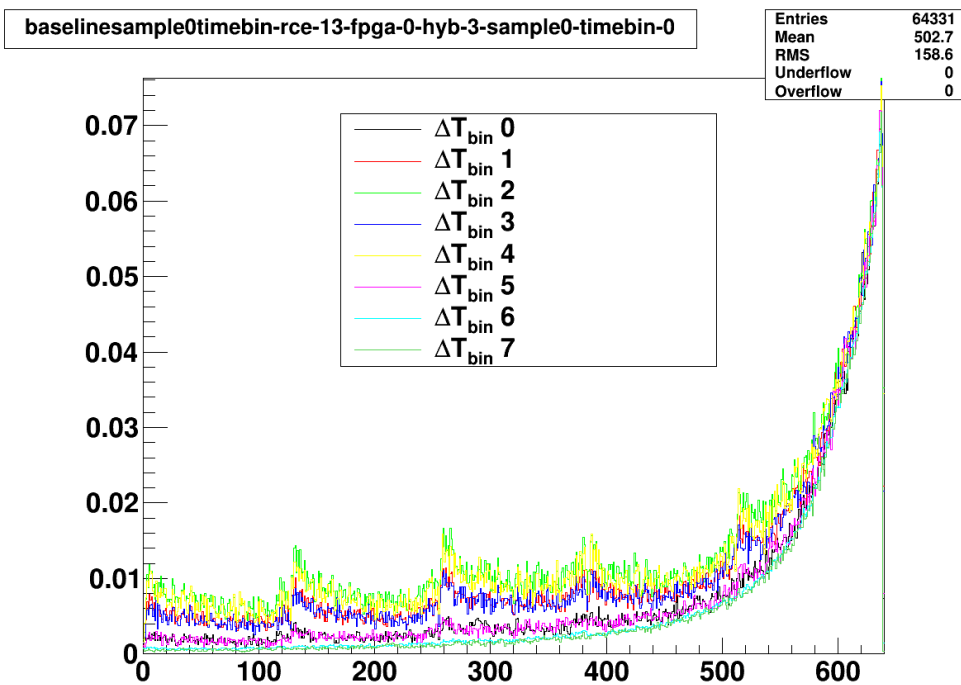
Look at channels with large occupancy changes

Plot as a function of time



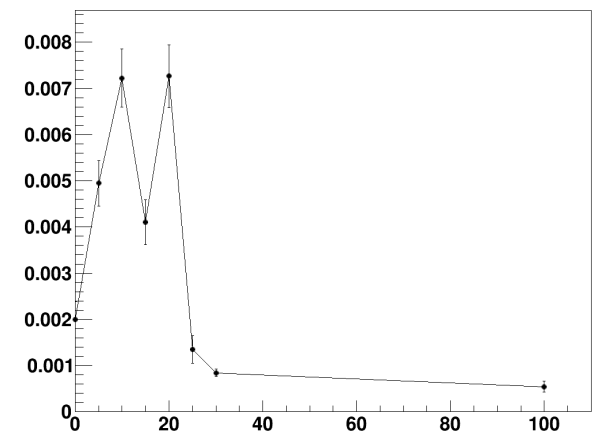
# Delta Trigger Time Evolution of Occupancy

Ex. 170 channels with x10 occupancy difference depending on trigger delta time



This structure are seen on **ALL** sensors.  
>95% of channels that I looked at share this feature (others seem statistically consistent with it...)

occupancy\_vs\_timebin\_ch101\_R13\_F0\_H3.png



occupancy\_vs\_timebin\_ch229\_R13\_F0\_H3.png

