CSC Functional blocks

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U.S. DEPARTMENT OF ENERGY
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

ASM-II

SLAC

- Chamber input signal
  - Precision (x-strip) data is from 2 ½ layers
    - 96 channels per ½ layer = 192 channels
  - Transverse (y-strip) data is from 4 layers
    - 48 channels per layer = 192 channels
  - Each of 16 HAMACs handle 12 channels = 192 channels
  - WA[7:0] selects which of 144 capacitors samples the input signal
    - All 12 HAMAC inputs are sampled on each WCLK
    - All HAMACs operate in lock step
      - Omitting a write address (to e.g., skip a bad cell) affects all 16 HAMACs
  - Mapping of strip number to HAMAC input channel is unclear
- Output is on 2 G-Links, 16 bits at 40 MHz, each
  - 4 bits of 4 channels per word on each fiber
  - SD is sampled on 8 RCLKs to build up the 8-bit read address: 0 – 143
  - HAMACs use G[1:0] signal to select between L, M, H inputs
    - Valid values are 1, 2, 3. G = 0 during the 3 (of 15) cycle setup time.
  - 4 RCLKs clock out 4 channel samples for a given G (I think)
    - 12 RCLKs clock out all 12 channel samples
  - HAMACs can operate with an 8 MHz RCLK
    - But ASM2MUX can do only 5 or 6.67 MHz (TBV)

Data format on the fibers

SLAC

Fiber B

15 12	11 8	7 4	3 0
$L1H15_{3:0}$	$L1H13_{3:0}$	$L0H11_{3:0}$	$L0H9_{3:0}$
$L1H15_{7:4}$	$L1H13_{7:4}$	$L0H11_{7:4}$	$L0H9_{7:4}$
$L1H15_{11:8}$	$L1H13_{11:8}$	$L0H11_{11:8}$	$L0H9_{11:8}$
$L1H16_{3:0}$	$L1H14_{3:0}$	$L0H12_{3:0}$	$L0H10_{3:0}$
$L1H16_{7:4}$	$L1H14_{7:4}$	$L0H12_{7:4}$	$L0H10_{7:4}$
$L1H16_{11:8}$	$L1H14_{11:8}$	$L0H12_{11:8}$	$L0H10_{11:8}$

RCLK →

Channel 1 = strips 0, 12, 24, …, 84

Channel 2 = strips 1, 13, 25, …, 85

⋮

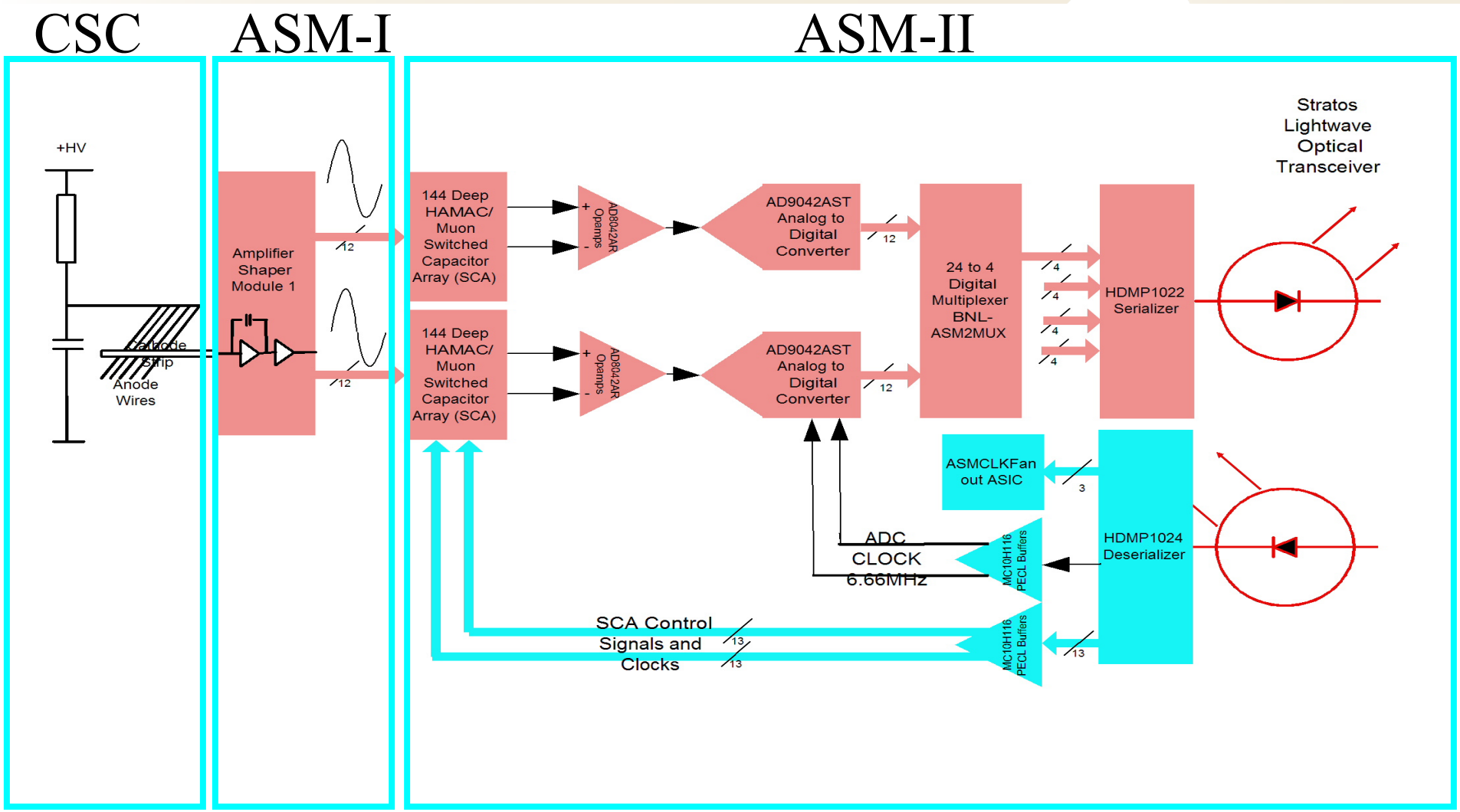
Fiber A

15 12	11 8	7 4	3 0
$L1H7_{3:0}$	$L1H5_{3:0}$	$L0H3_{3:0}$	$L0H1_{3:0}$
$L1H7_{7:4}$	$L1H5_{7:4}$	$L0H3_{7:4}$	$L0H1_{7:4}$
$L1H7_{11:8}$	$L1H5_{11:8}$	$L0H3_{11:8}$	$L0H1_{11:8}$
$L1H8_{3:0}$	$L1H6_{3:0}$	$L0H4_{3:0}$	$L0H2_{3:0}$
$L1H8_{7:4}$	$L1H6_{7:4}$	$L0H4_{7:4}$	$L0H2_{7:4}$
$L1H8_{11:8}$	$L1H6_{11:8}$	$L0H4_{11:8}$	$L0H2_{11:8}$

→

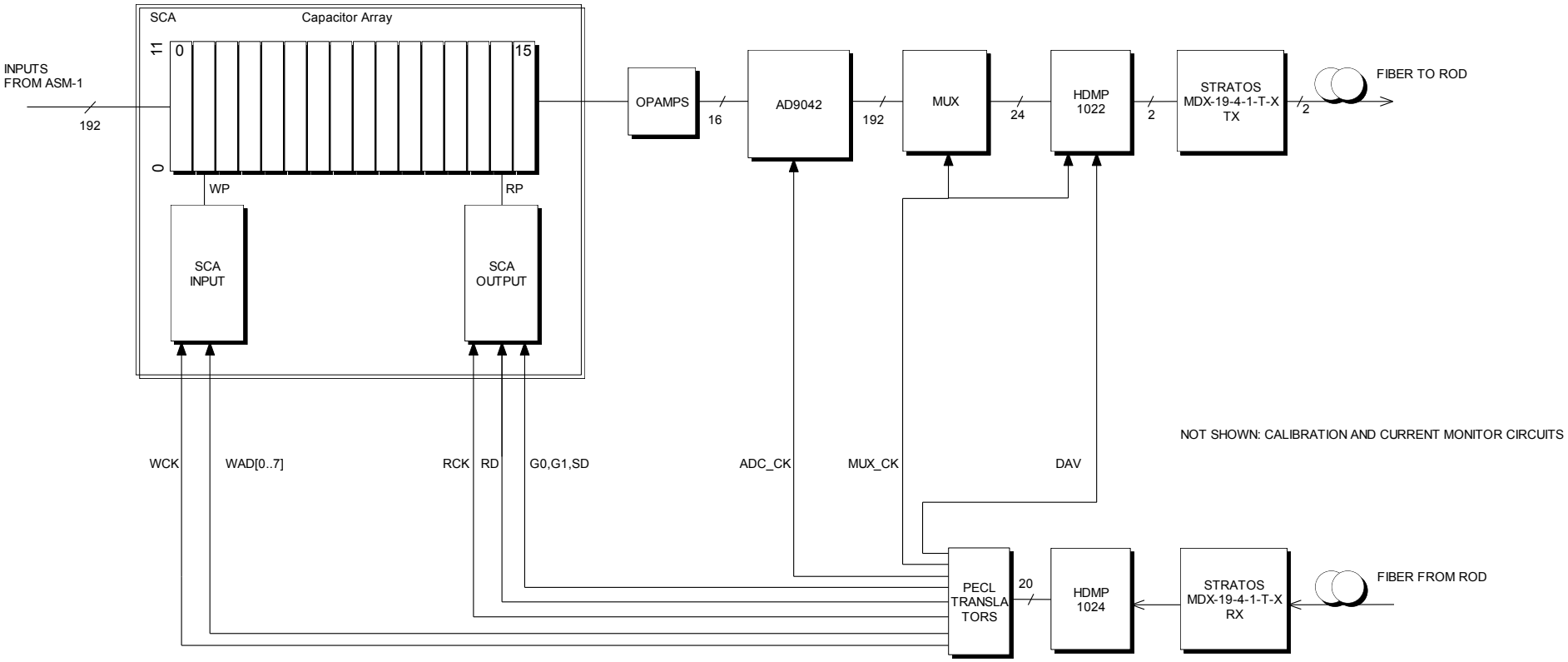
- L = Layer (0 – 1)
- H = HAMAC index (1 – 16)
- C = HAMAC channel (1 – 12)
- Strip = (H-1)*12+(C-1) (TBV)
- 4 ½ nibbles make up a word

Signal flow on CSC



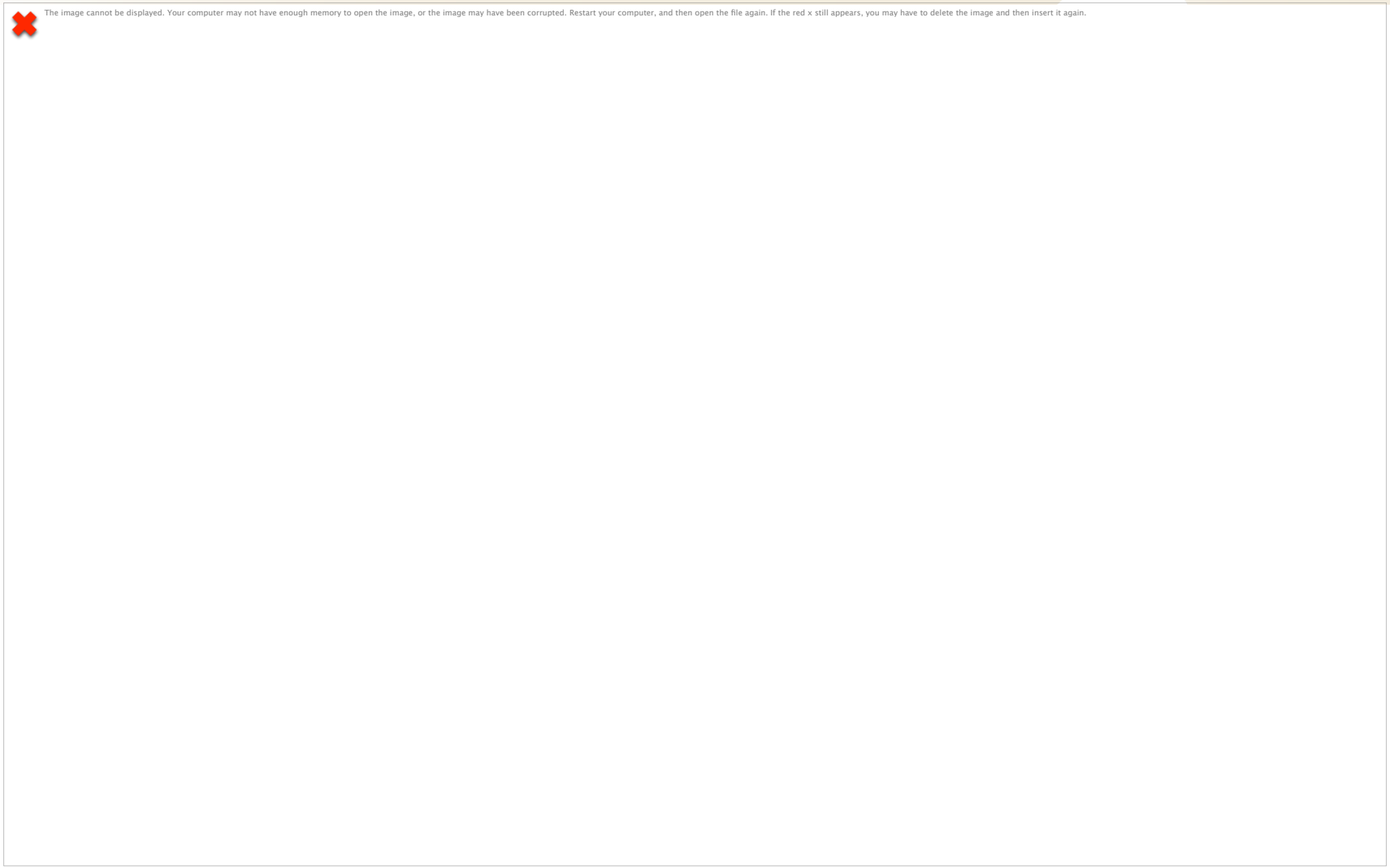
http://indico.cern.ch/materialDisplay.py?contribId=61&sessionId=35&materialId=slides&confId=0510

ASM-II architecture



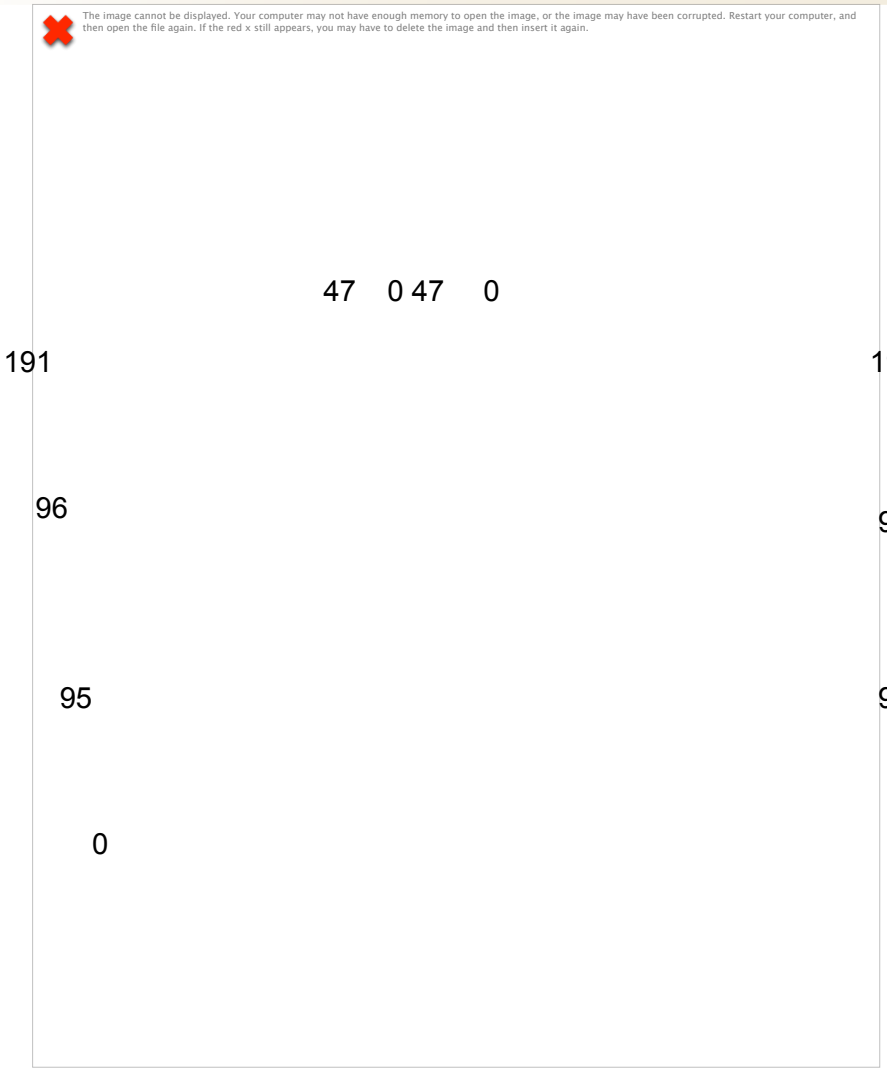
http://www.inst.bnl.gov/~poc/CSC_Documents/Review%20of%20ASM%20readout%2005-10-01.doc

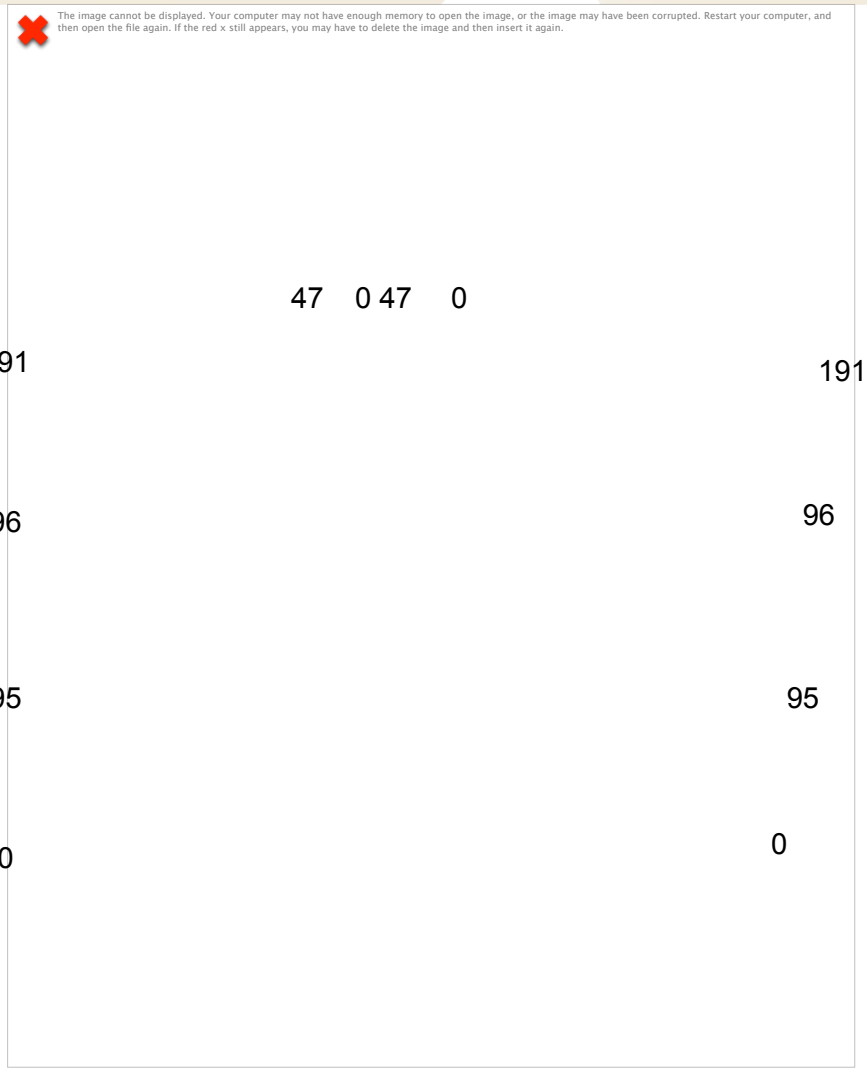
On-chamber electronics location



http://www.inst.bnl.gov/~poc/CSC_Documents/Boston%20Review%2005-05-01.pdf

Fiber Nomenclature



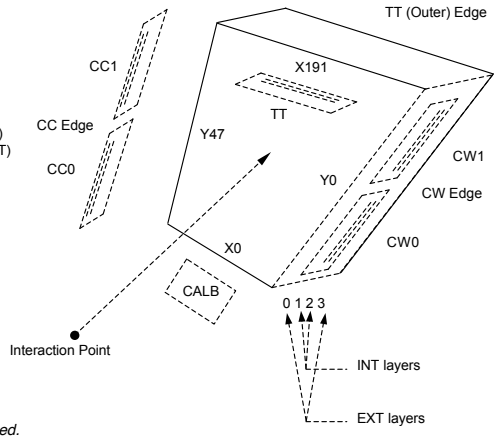


http://positron.ps.uci.edu/~schernau/ROD/CSCFibers2.pdf

Chamber Nomenclature

CSC Chamber Nomenclature Related to CTM and ROD Connections

chamber types	L, S	large and small chambers
layers	0, 1, 2, 3	layer 0 is nearest interaction point
precision strips	X0-X191	see diagram
transverse strips	Y0-Y47	see diagram
chamber edges	CW, CC, TT	see diagram
ASMII's	CC0, CC1, CW0, CW1, TT	see diagram
ASMII control link	CTL	one control link per ASMII
ASMII data links	INT, EXT	INT data link carries data from internal layers (1,2) (except TT) EXT data link carries data from external layers (0,3) (except TT)
calibration board	CALB	calibration pulser, one per chamber
CALB control link	CAL	one control link to CALB, no data links
Fiber ribbons	FC, FA, FB	12-fiber ribbons--see CTM table



Chamber

ASMII	strips	INT layer(s)	EXT layer(s)	
CW0	X0-X95	2	3	"clockwise"
CW1	X96-X191	2	3	
CC0	X0-X95	1	0	"counterclockwise"
CC1	X96-X191	1	0	
TT	Y0-Y47			"top" or "transverse"

All fibers must be routed correctly--options for reassigning control or data fibers at the CTM are extremely limited.

CTM

TX FPGA	controller*	MGT*	fiber*	control link →	chamber	ASMII ⇢	data link	layer(s)	strips*	fiber*	MGT*	RCV*	RX FPGA	DPU*	Per-slice and Loss-of-Lock Status*
TX0	SCA_C	0	FC.0	CTL	L	CC0	EXT	0	X0-X95	FA.0	0	0	RXA0	A0	
							INT	1	X0-X95	FA.2	2	1		A1	
	SCA_C	1	FC.1	CTL		CC1	EXT	0	X96-X191	FA.1	1	0		A0	
							INT	1	X96-X191	FA.3	3	1		A1	TX0 ◄► RXA0
	SCA_C	2	FC.2	CTL	S	CC0	EXT	0	X0-X95	FB.0	0	0	RXB0	B0	TX0 ◄► RXB0
							INT	1	X0-X95	FB.2	2	1		B1	
	SCA_C	3	FC.3	CTL		CC1	EXT	0	X96-X191	FB.1	1	0		B0	
							INT	1	X96-X191	FB.3	3	1		B1	
TX1	SCA_C	0	FC.8	CTL	L	CW0	EXT	3	X0-X95	FA.8	0	0	RXA1	A3	
							INT	2	X0-X95	FA.10	2	1		A2	
	SCA_C	1	FC.9	CTL		CW1	EXT	3	X96-X191	FA.9	1	0		A3	
							INT	2	X96-X191	FA.11	3	1		A2	TX1 ◄► RXA1
	SCA_C	2	FC.10	CTL	S	CW0	EXT	3	X0-X95	FB.8	0	0	RXB1	B3	TX1 ◄► RXB1
							INT	2	X0-X95	FB.10	2	1		B2	
	SCA_C	3	FC.11	CTL		CW1	EXT	3	X96-X191	FB.9	1	0		B3	
							INT	2	X96-X191	FB.11	3	1		B2	
TX2	SCA_C	0	FC.4	CTL	L	TT	"EXT"	1,3	Y0-Y47	FA.4	0	0	RXA2	A4	
							"INT"	0,2	Y0-Y47	FA.5	1	0		A4	
	SCA_C	1	FC.5	CTL	S	TT	"EXT"	1,3	Y0-Y47	FB.4	0	0	RXB2	B4	TX2 ◄► RXA2
							"INT"	0,2	Y0-Y47	FB.5	1	0		B4	TX2 ◄► RXB2
	CAL_C	2	FC.6	CAL	L	(CALB)									
	CAL_C	3	FC.7	CAL	S	(CALB)									

controller*: Each TX FPGA contains one SCA controller and one CAL controller. During system initialization, ROD software selects the controller stream each MGT will output.
MGT*: MGT = multi-gigabit transceiver. Each Tx FPGA contains four MGT's used as G-Link serializers. Each Rx FPGA contains four MGT's used as G-Link deserializers.
fiber*: 0-11 refer to channel numbers specified in the parallel fiber-optic module data sheets.The fiber fanouts may map these channels onto individual fibers with a different labeling scheme, e.g., 1-12 or 12-1.
RCV*: Each RX FPGA contains two receiver modules. Each module receives two fibers and outputs time slices to one DPU.
strips*: The CTM uses lookup tables (one per RCV*) to re-order strips (ADC samples) as needed.
DPU*: The ROD uses its Data Exchange to read out DPU's in any desired order. Transfer between ROD sides A and B is not supported.
Status*: The CTM sends fill frames on an ASMII's control link when it detects simultaneous loss of lock on both of that ASMII's data links.

http://positron.ps.uci.edu/~pier/csc/CTM/ChamberNomenclature00.pdf

Useful links

SLAC

Chamber specifications

- https://twiki.cern.ch/twiki/pub/Atlas/CscDocuments/chamberNumbers.txt

ASM-II schematic

- https://twiki.cern.ch/twiki/pub/Atlas/CscIntegration/asm2_schematic.pdf

Data stream decode map

- http://positron.ps.uci.edu/~schernau/ROD/decodemapl-2.xls

HAMAC documentation

- http://www.nevis.columbia.edu/~atlas/electronics/asics/sca/DOC_HAMAC.pdf

SCA Controller

- http://www.inst.bnl.gov/~vetter/atlas/sca_note.pdf

G-link record format

- http://positron.ps.uci.edu/~schernau/ROD/G_Link_Record_Format.xls

G-Link datasheet

- http://www.alldatasheet.com/datasheet-pdf/pdf/64650/HP/HDMP-1022.html

CTM Reference manual

- http://positron.ps.uci.edu/~pier/csc/CTM/CTM_ReferenceManual_01.pdf

Uplink – Front End Transmitters

SLAC

HDMP-1022 G-Link protocol

- Various lock types:
  - Frequency lock – Local reference clock vs. link bit rate
  - Protocol lock – G-Link protocol
  - Word lock – Correctly aligned words
- SEUs can induce loss of lock for ~500 uS
  - Monitor loss of lock rate
    - DCS uses this to power lasers down if excessive
      - Really? How?
- 5 + 1 16-bit data inputs
  - Five are used by the SCA block
  - One is used by the calibration pulser block

Uplink

SLAC

Status register:

- Lock status
- Phase fault – Incorrect CLK40 phase seen
- Phase match – Correct CLK40 phase never seen
- SCAC_DAV was active at same time as periodic DAV
  - Huh? Does this belong here?
- Next time-slice starts before all serial info received
  - Does this belong here?

Uplink

SLAC

Control register (normal run-time values underlined):

- Downlink associations: (complicated but static)
  - One bit per downlink – setting bit means downlink must lose lock before uplink is assumed to have lost lock
- Source: SCAC
  - SCAC, CAL, Test, etc.
- Fill mode: DL_LOL
  - Conditions under which fill frames are sent? Valid values:
    - None, Force, Controller, Downlink loss of lock
- MGT power down: 0
- Link reset: 0
  - Reset the MGT's buffer, i.e. recenter it
- Disrupt: 0
  - Send word with invalid protocol → force loss of lock, to e.g. test system response to loss of lock

Uplink

SLAC

Delay register:

- Vernier delay: 4
  - 0 – 9 → number of bits to delay input stream
- Coarse delay: 0
  - 0 – 15 → 1 – 16 cycles of CLK80
- Fill delay begin: 10 = 1 ms
  - 0 – 15 → 0 – 1.5 ms must elapse with downlink LOL active before fill frames are sent
- Fill delay end: 5 = 5 ms
  - 0 – 15 → 0 – 15 ms of fill frames will be sent after downlink LOL is deactivated

Uplink

SLAC

Test data register:

- Data output on G-Link when Control.Source is set to Test

Loopback register:

- Time mode: 0
  - Enter up/down-link loopback timing mode – uplink output will not be standard G-Link protocol
- Time mark: 0
  - Rising edge starts up/down-link round-trip time measurement
- Loopback: 1
  - Connects uplink to downlink – when deasserted, downlink has no input and its PLL should lose lock
- Inhibit: 0
  - Force uplink differential output to zero

Uplink

SLAC

CV_Time register (Read only):

- Uplink → downlink delay measurement, zero if no valid measurement

Latency registers (12) (Read only):

- Uplink → downlink time in bit periods – zero indicates no valid measurement
- 8 bits of value in units of 10 bit periods
- 4 bits of value in units of 1 bit period

Downlink – Front End Receivers

SLAC

HDMP-1024 G-Link protocol

- Various locks:
  - Frequency lock – Local reference clock vs link bit rate
  - Protocol lock – G-Link protocol
  - Word lock – Correctly aligned words
- SEUs can induce loss of lock for ~500 uS
  - Monitor loss of lock rate for DCS
  - Power down lasers if excessive on too many fibers
- 10 + 2 16-bit data outputs
  - 10 = 5 pairs for receiving chamber data
    - 1 pair for each ASM-II Front End Board
  - 2 channels are unused

Downlink

SLAC

Status register:

- Phase status – Incorrect CLK40 phase seen
- Phase match – Correct CLK40 phase never seen
- Excessive loss of lock – 1 bit per deserializer
- Lock state
  - Resetting
  - Attempting bit alignment
  - Attempting word alignment
  - Locked

Downlink

SLAC

Link control register:

- Latency: 79, but overwritten by configuration value
  - The length of the TTC latency pipeline, i.e. the piepline that delays DAV_N from the uplink block such that it is aligned with the DAV_N from the ASM-IIs

Receiver control register:

- LASTP_DATA: 23
  - Last data paragraph in time slice, typically set to 192/8 - 1 = 23
    - (for 192 12-bit ADC samples)
- LASTP_STAT: 24
  - Last status paragraph in time slice, typically set to LASTP_DATA + 16/8
    - (for 16 12-bit status words)
- INVERT_RCLK: 0
  - 1 → invert RCLK, i.e., use DCM's CLK180 instead of CLK0
- NOINV_FLAG_ERR: 0
  - Do not invalidate slices because of flag errors
- POWERDOWN: Unused channels
  - Can be used to power down unused MGT's, e.g., those attached to the two spare fibers

Downlink

SLAC

Readout sequencer control register:

- RSEQ_LENGTH: 52
  - Readout sequence length in output triplets (3 16-bit halfwords) – typically set to (192+16)*12/16/3 = 52
    - (for 192 12-bit ADC samples and 16 12-bit status words)
- OTEST_PATTERN: None
  - Output test pattern: None, Alternate, Count
- RSEQ_ENABLE: 1, except for unused channels
  - 1 → enable output sequencer, else its output is zero – this is independent of OTEST_PATTERN

Loss of lock override register:

- Mask: (unused channels)
  - Which channels are affected by the override

Downlink

SLAC

Status counter registers:

- Protocol error
- Flag error
- Data error
- Lock error
- Uplink invalid
  - Uplink asserting INVALIDATE, as extended in this block

(Not sure whether these are occurrences or durations (counts of some clock while true))

Downlink

SLAC

Reformat Mask register:

- REFORMAT_MASK: 0x800
  - xor'd into the 12-bit ADC samples before they are output
- RECEIVER_ID: 0 – 5, 8 – 13 (0 – 3 → X0 – X3, 4 → Y, 5 → unused)
  - Data stream identifier sent in status words

RCLK phase register: (Scanned)

- RCLK phase control – writing 0/1 steps phase +/- (hardware saturates phase in both directions)

Downlink

SLAC

Delay register (read only):

- Delays as determined by deserializer's lock acquisition mechanism – zero when not locked
  - Course – units of 10 bit
  - Fine – units of 1 bit

Readout LUT X setup register:

- Used to deconvolve data organization on the link
- See `WriteLUT_Standard()` in `ctm_rcv.cpp`

Readout LUT Y setup register:

- Used to deconvolve data organization on the link
- See `WriteLUT_Standard()` in `ctm_rcv.cpp`

SCA Controller

Control register:

- SCAC_RUN
- BUSY threshold
- BUSY enable

Status register:

- FAULT_SCAC_FREE_FIFO
- FAULT_SCAC_WRITE_ADDR
- FAULT_READOUT_SEQ

SCA Controller

Setup register:

- Number of time slices to read out per trigger (8 bits)
  - 4, but want to go as high as at least 8
- Enable simultaneous read/write, else SCA write address does not advance during readout (1 bit)
  - 1
- Read clock phase w.r.t write address (1 bit)
  - 0
- Read clock rate: 0 = 5 MHz, 1 = 6.67 MHz (1 bit)
  - 1
- Write clock rate (2 bits):
  - 00 = 20 MHz, CLK_20M toggled, 0 phase
  - 01 = 20 MHz, CLK_20M toggled, 180 phase
  - 10 = 20 MHz, CLK_20M held low
  - 11 = 40 MHz, CLK_20M held low
- Reset lookup table address register (1 bit)
  - Obsolete and unused
- Tx mode (2 bits)
  - 00 = Drive Tx with SCA control
  - 01 = Drive Tx with test pattern
  - 10 = Drive Tx with simulated ASM-II data
  - 11 = reserved

SCA Controller

SLAC

Readout sequencer setup (ROSEQ_Setup) register:

- DAV delay in RCLK periods (6 bits)
  - (RDCLK == 6.67 MHz ? 6 : 8) * 2 + 9 → 21
- LUT select (1 bit)
  - Obsolete and unused
- SD phase w.r.t RDCLK in 40 MHz counts (3 bits)
  - 0
- ADC clock phase w.r.t RDCLK in 40 MHz counts (3 bits)
  - (RDCLK == 6.67 MHz ? 6 : 8) – 1 → 5

SCA Controller

SLAC

LatencyCells register:

- Number of SCA cells to use (8 bits)
  - 144
- Depth of latency pipeline in clock cycles (8 bits)
  - 20, value is loaded from configuration DB

SCA Controller

SLAC

Look-up tables:

- Unexercised (by us) diagnostic modes allow filling the LUT with user-supplied pattern
- LUT is readable by software

Readout Sequence LUT:

- Calculated at configuration time
  - Depends on read clock rate (5 vs 6.67 MHz)
  - See `WriteROSEQ_LUT_Standard()` in `ctm_scac.cpp`
- 91 entries of 256 used in normal running
- “Successful operation typically requires ~50 <= N <= 145 entries”

Gray LUT:

- Calculated at configuration time
  - Depends on SCA cell count choice
  - See `WriteROSEQ_LUT_Standard()` in `ctm_scac.cpp`

SCA Controller

SLAC

Uplink data:

- RD_CLK (Bit 0)
  - 6.67 MHz
  - Active during SCA readout
- SD (Bit 1)
  - Serial read address data
    - 8 bits shifted in on RD_CLK
- RD (Bit 2)
  - Read frame
    - High during readout
    - Rising edge stores serial address data
- GA[1:0] (Bits 4:3)
  - Gain address bits
  - Used to select gain for readout in calorimeter (4 channels, 3 gains)
  - Used as high order channel address bits in MUON readout sequence (12 channels)
- WA[7:0] (Bits 5:12)
  - Write address for incoming data
  - Which of the 144 SCA storage locations to put data
  - Updated once per write clock (once every receive word?)
- TRIG_DATA (Bit 13)
  - Appears to be unused, but `CTM_ReferenceManual.pdf` indicates this goes to DAV~ of HDMP-1022s
- ADC_CLOCK (Bit 14)
  - ADC conversion clock
  - Adjustable phase to RD_CLK
- SCA_WRITE_CLOCK (Bit 15)
  - SCA write clock
  - Max frequency is 20MHz if really used (one half cycle per received word)
  - Firmware suggests jumper on ASMII to use serial recovered clock
    - Jumper does not appear on schematic

SCA Controller notes

SLAC

- 40 MHz word rate on uplink fiber, 16 bit words = 640 Mbits/sec
  - "The ROD transmits a clock and 17 parallel control bits to the ASM-II" (16 + FLAG?)
  - "Read cycle requires 15 read clock cycles to read out 12 channels of one time sample." – See `HAMAC_readout_timing.pdf` in `reseng CSC_working` repository
  - 1 bit per word allocated to RCLK
  - Toggle every (=> RCLK rate => 4 sample readout time => Max L1 rate):
    - `8 words => 5    MHz => 12.0 uS =>  83 KHz`
    - `7 words => 5.7  MHz => 10.5 uS =>  95 KHz`
    - `6 words => 6.67 MHz =>  9.0 uS => 111 KHz`
    - `5 words => 8    MHz =>  7.5 uS => 133 KHz`
    - `4 words => 10   MHz =>  6.9 uS => 167 KHz`
  - 5 MHz = minimum: ADC constraint
  - RCLK can only be 5 or 6.67 MHz due to 2*12 to 4 bit MUX chip used on ASM-II
    - If we used 8 MHz, only 20 of the 24 bits will be presented to the G-link transmitter
- 20 vs 40 MHz WCLK
  - Unclear whether 40 MHz is really supported by ASM-II w/o jumper changes
- WCLK of 20 MHz and 4 samples
  - To capture 140 ns features
- 40 MHz word rate on downlink fiber, 16 bit words → saturation occurs at:
  - (2 fibers * 16 bits/word * 40 MW/sec) / (192 channels / time-slice * 12 bits / channel)
  - 556 K time-slices / second = 138 KHz L1 rate

Calibration controller

Control registers:

- Main
  - Assert time: 10 – valid range is 0 - 0x3f
    - Number of uS pulser output is asserted in response to a single-cycle CAL
  - Pulser enables: 0
    - One enable bit for each CAL board pulser line
    - Calibration is typically one layer at a time
  - Pulser polarities: 0
    - One invert bit for each CAL board pulser line
- Link
  - Attenuation: 0x20
    - Attenuation level – 64 0.5 dB steps to 31.5 dB
  - Invert TTC CAL: 0
    - Chooses edge of TTC CAL pulse that causes CAL board output pulse
      - Probably never used, because TTC CAL pulse should be active for just one clock cycle
  - Link Enable: 0
    - 0 → G-link data lines will be zero and fill frames sent (if serializer is set up to use CAL controller's link enable, which it typically is not)
  - Ground output: 0xf
    - One ground bit for each CAL board pulser line

Calibration controller notes

- Same G-Link method as used on the ASM-II:
  - HDMP- 1024
  - 40 MHz word rate on uplink fiber, 16 bit words
  - FLAG is used as extra data bit, but is unconnected
- Four independent channels
- Programmable attenuator is PE4302
  - http://www.psemi.com/pdf/datasheets/pe4302ds.pdf
- When not in use, fill frames are sent to keep lock
  - Outputs are grounded
- Control word bit mapping:

G-Link Data Bit	Function	Notes
D0	0.5dB	1 = Attenuate
D1	1.0dB	”
D2	2.0dB	“
D3	4.0dB	“
D4	8.0dB	“
D5	16.0dB	“
D6	Pulser 0	Inverting
D7	NC	
D8	NC	
D9	Pulser 1	Inverting
D10	Pulser 2	Inverting
D11	Pulser 3	Inverting
D12	Analog Switch 0	1= ground output
D13	Analog Switch 1	“
D14	Analog Switch 2	“
D15	Analog Switch 3	“
D16..19	NC	

https://twiki.cern.ch/twiki/pub/Atlas/CscPulser/CSC_Pulser_H.pdf

Timing, Trigger and Control (TTC)

SLAC

- Trigger message definition:
  - TBD, but includes L1ID, BCID, ECR, BCR, CAL, Orbit
  - Convert to Trigger Information Stream (TIS)
- Assign Trigger message ID (TID) to TIS
  - Synonymous with L1ID?
  - Want to avoid increasing size of TIS
- Pass 32-bit TID to FEX RCEs
  - Two (?) trigger kinds: L1A, CAL
  - Can not allow a TID (= a TIS) to cause more than one readout
    - Can we check for this? E.G., Read-out Request counter != TID => bugcheck
  - Tag outgoing data with TID
- Pass TIS (includes TID) to Fmt RCEs
  - TIS arrives earlier than data
  - Fill in event contribution header and trailer as much as possible
  - Event build two data contributions according to TID
  - Complete and wrap with header and trailer
  - Hand off to ROL

TTC

SLAC

- Originally implemented in the SL FPGA
- Ability to locally construct TIS needed?
  - Yes, if operation without Trigger fiber is to be supported
- Capture Extended L1ID and Orbit number from trigger message
  - EL1ID increments after each L1A
- BCID, EL1ID and Orbit counter programmatically settable
  - Needed for stopless recovery
- Incomplete trigger message reception detection?
- L1ID rollover before ECR detection
- Unexpected BCR or BCID value detection
  - Requires BCID_MAX value = 3563 (= no. BCs per orbit?)
- Any status too look at about the TTC fiber link?
  - E.G. link loss (disconnected), error rate

Data Presenter

SLAC

- Deconvolves data from fiber order to order desirable for FEX

Feature Extraction (FEX)

SLAC

- Three possibilities
  - Software
  - Firmware
  - Some of each

Read Out Link (ROL)

SLAC

- Basically a ½ duplex optical link
  - Xon / Xoff is the only signal returned

Build system

SLAC

- One or more of these?
  - Firmware
  - Software framework
  - FEX