Large area pnCCD DAQ and Electronics

MPI semiconductor laboratory

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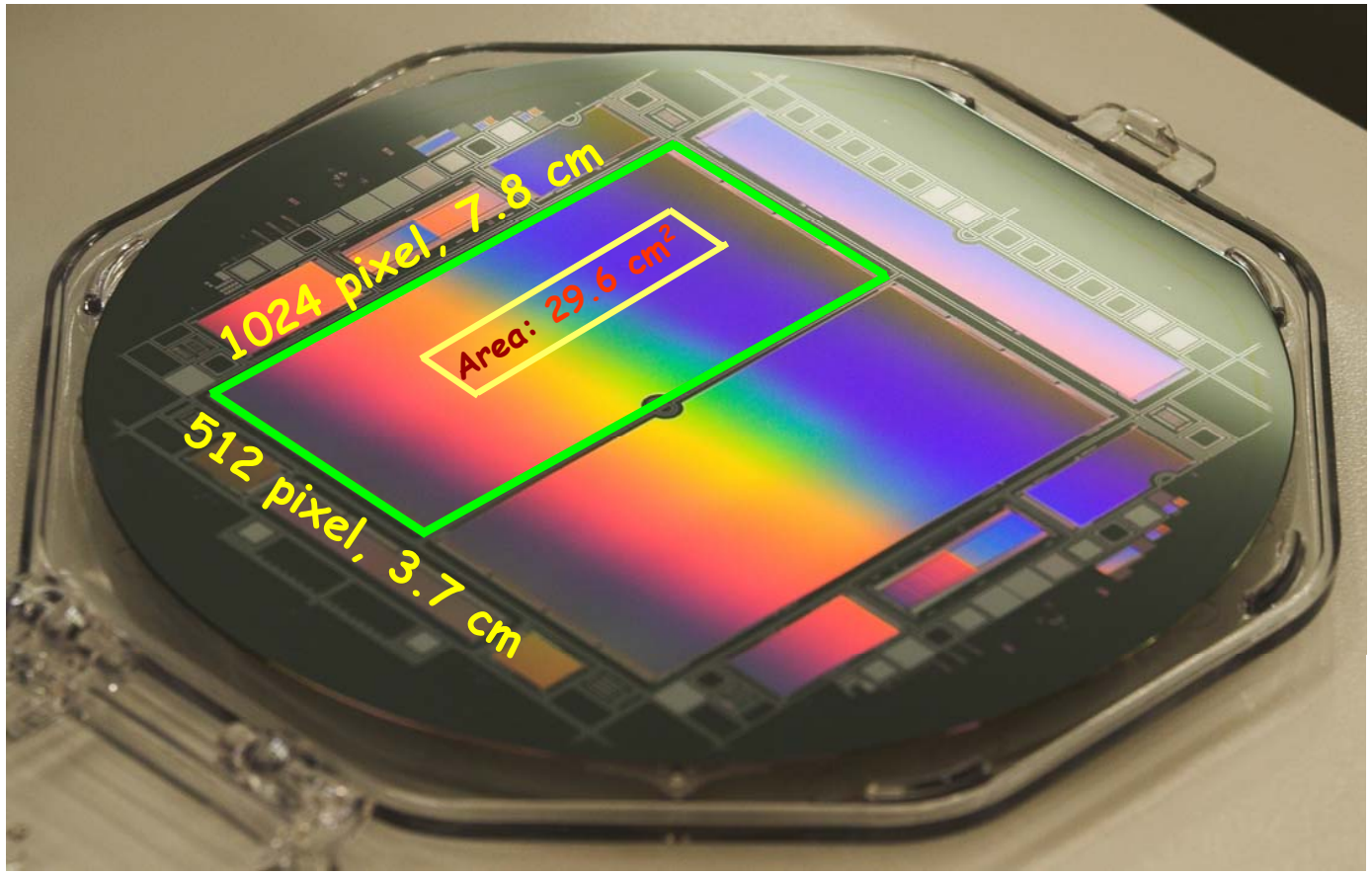
The pnCCD detector

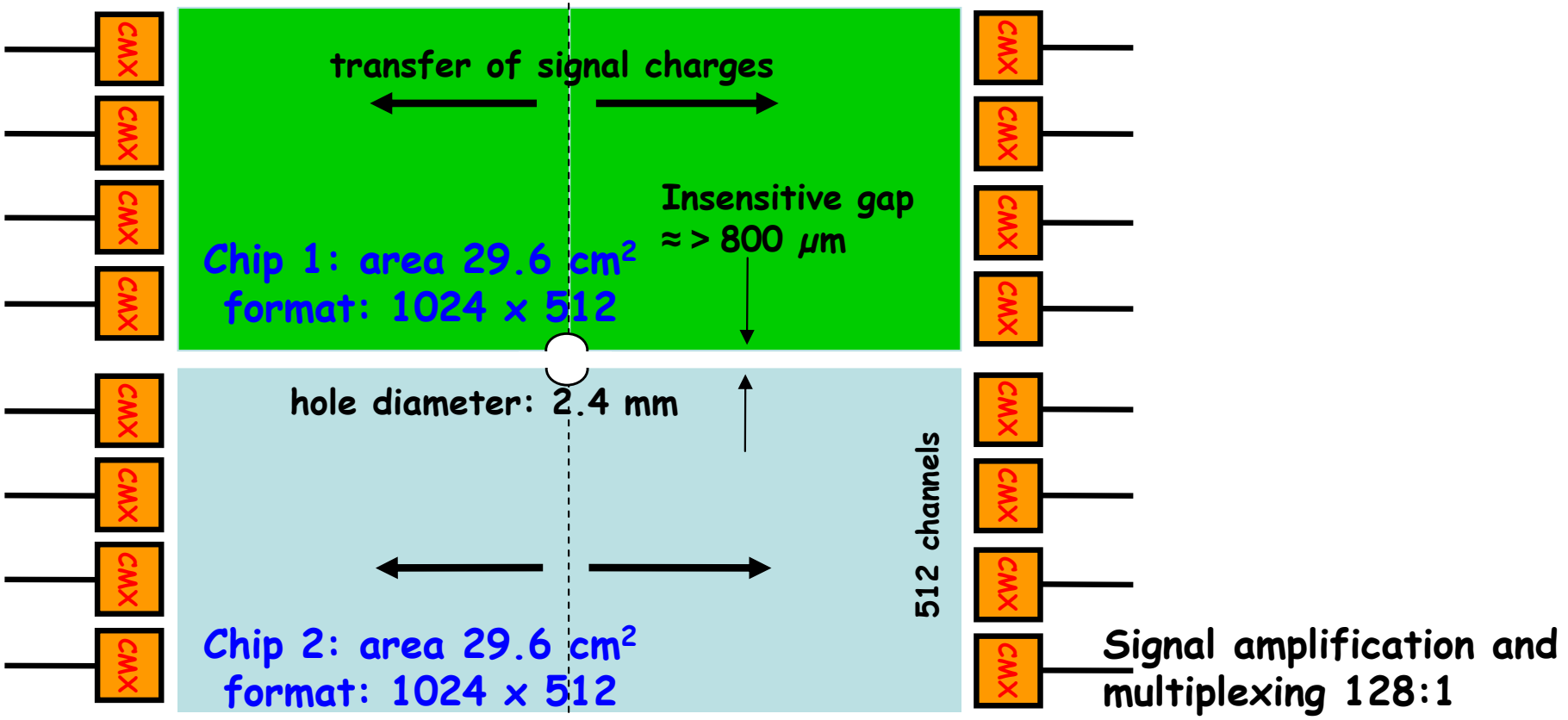


Size of one pnCCD chip:

- 1024 x 512 pixel
- 29.6 cm^2 area
- pixel size: 75 x 75 μm^2

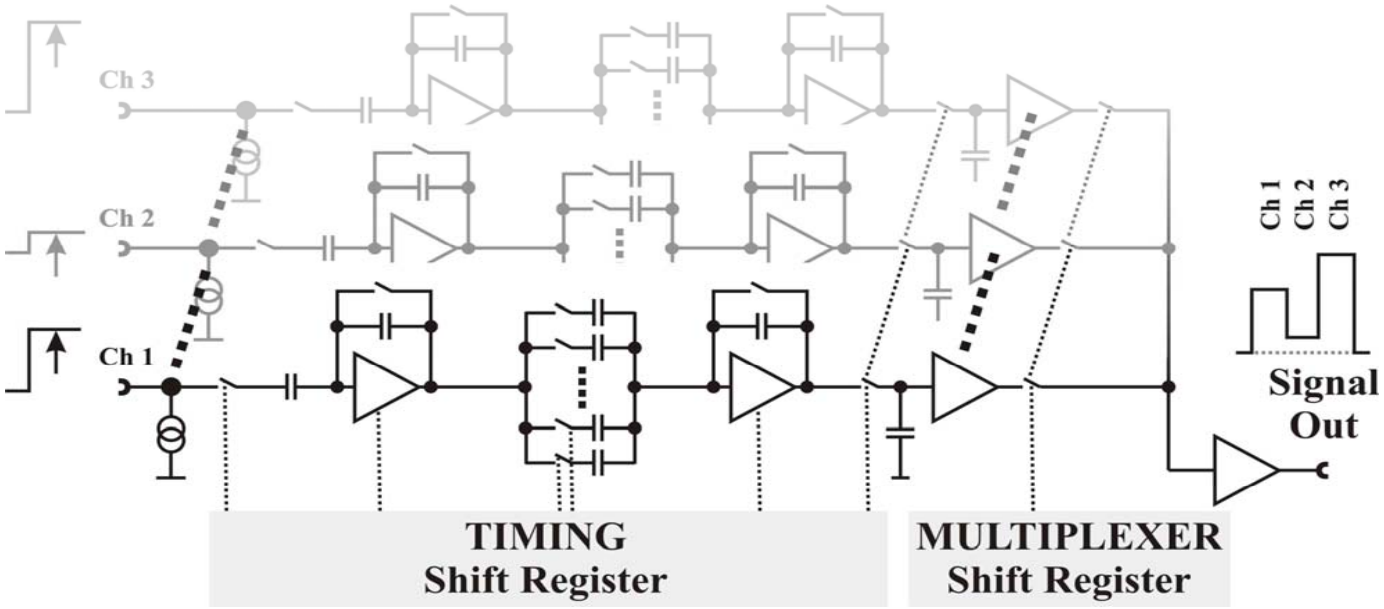
2 pnCCD chips will form one detector with central hole (open diameter 2.4mm) for direct beam aperture

pnCCD readout architecture



- CCD with column parallel readout
- Readout and signal amplification with 16 CAMEX (CMX) ASIC chips
- 128 input channels to 1 output node multiplexing per CAMEX chip
- In total 16 analog readout nodes per detector

CAMEX readout ASIC



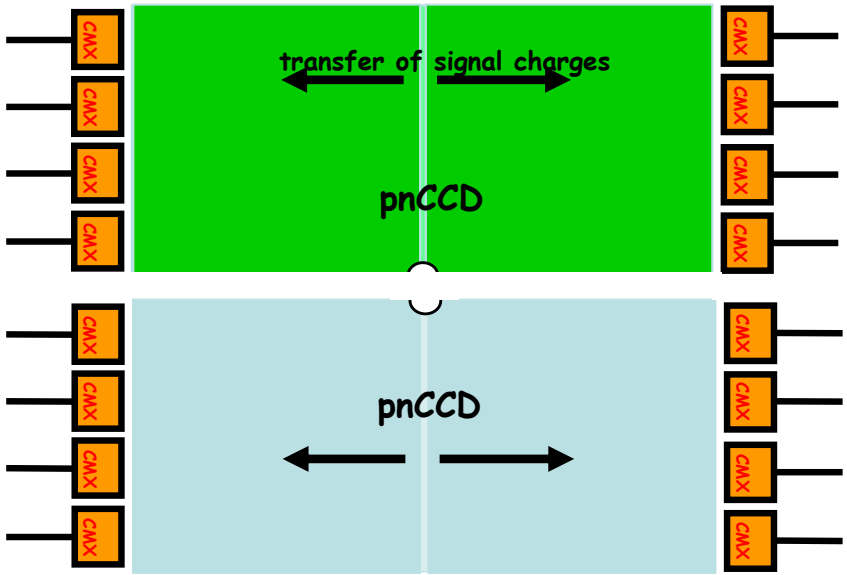
- Multi-correlated double-sampling filtering (MCDS)
- Signal processing of all 128 channels in parallel
- Serialized readout parallel to analog signal-processing
- Selectable gains and operating modes
- Electronic noise contribution less than 1 electron ENC
- Readout-speed up to 10MHz (i.e. 12.8µs per line)

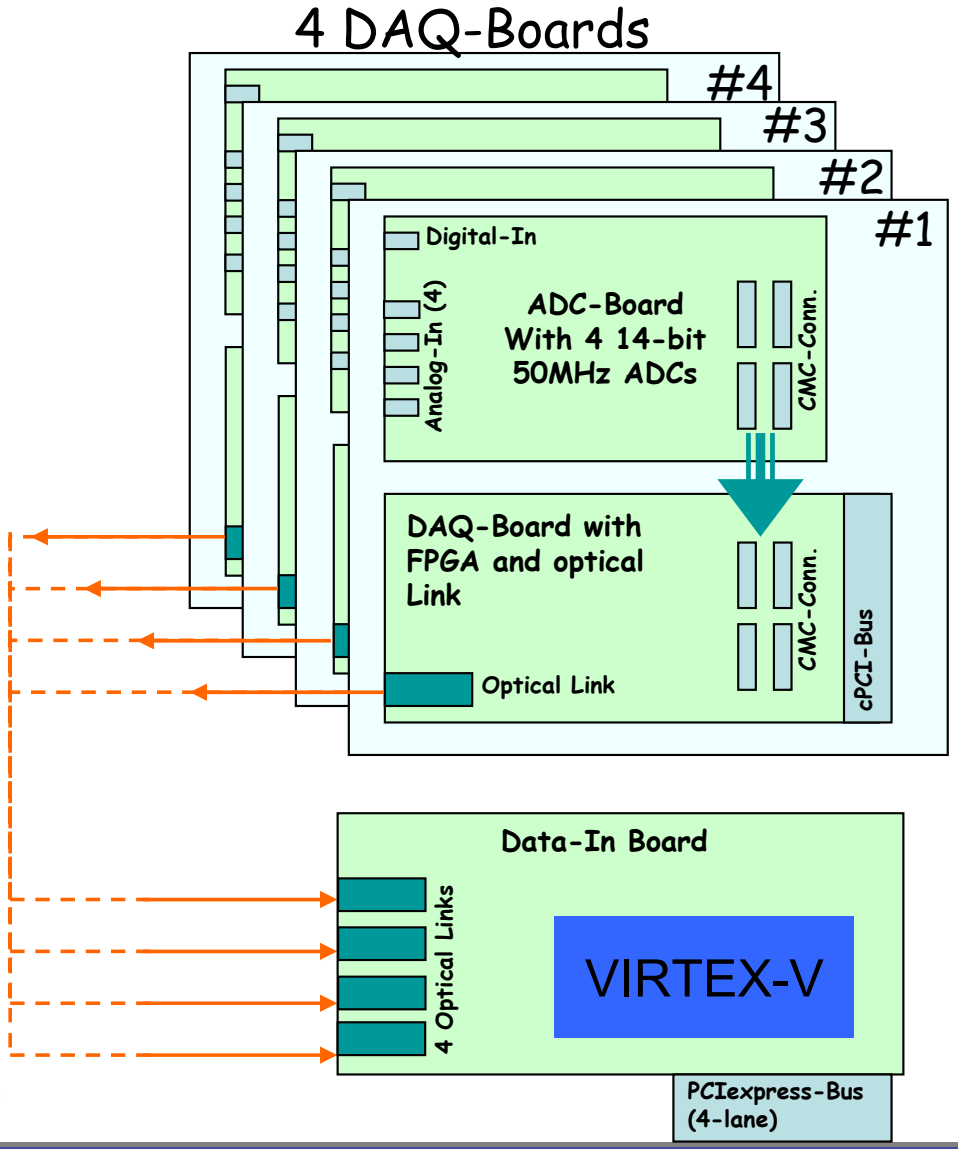
pnCCD detector readout

- LCLS to be operated at 120Hz
  - ⇨ one detector image to be readout within 8ms
- 512 lines to be readout due to split-frame transfer mode
  - ⇨ 16µs per line (2×(2×512) = 2048 pixel per line)
- Distributed on 16 readout nodes
  - ⇨ 15µs for 128 pixel = 8.5 MP/s clock per readout node
- In total 136 MP/s, split on 16 nodes
  - ⇨ 136 MP/s peak value, in mean 120 MP/s

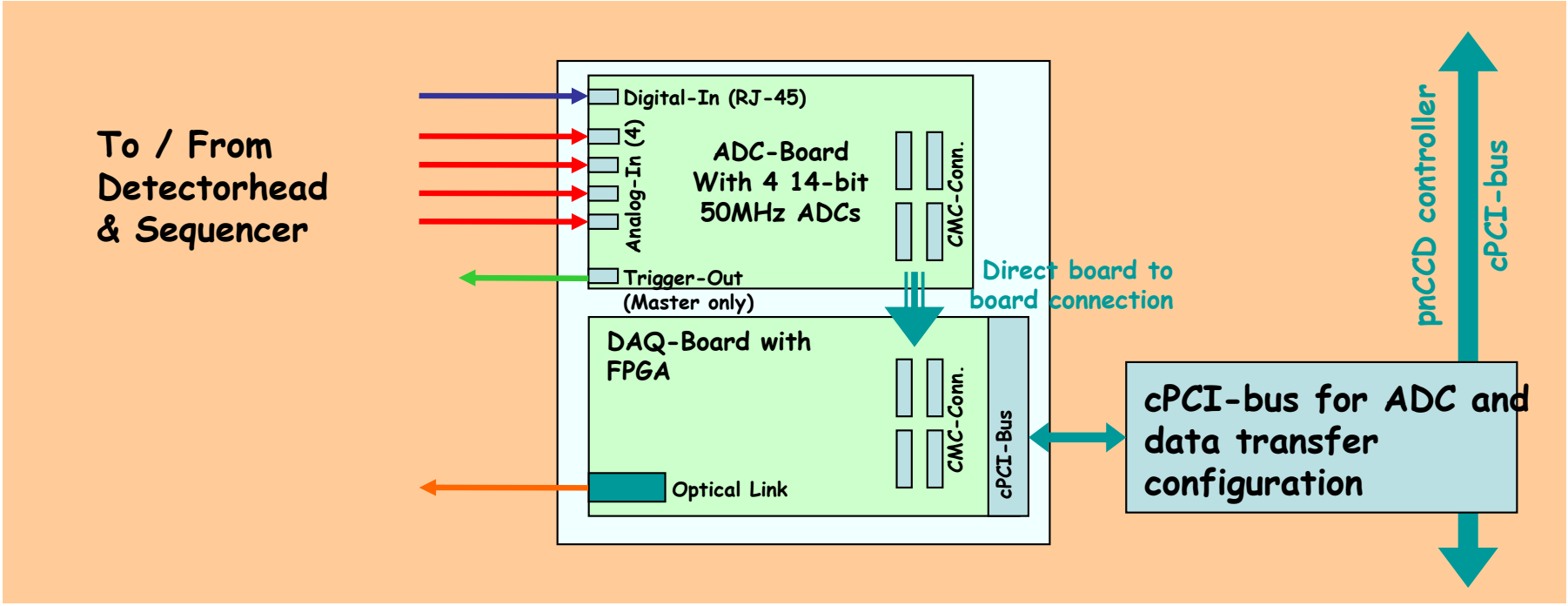
pnCCD DAQ architecture

1 Detectors with 1k×1k Pixel @ 120Hz
(→ 240 MByte/sec. in total @ 16 nodes)





ADC sub-system - I

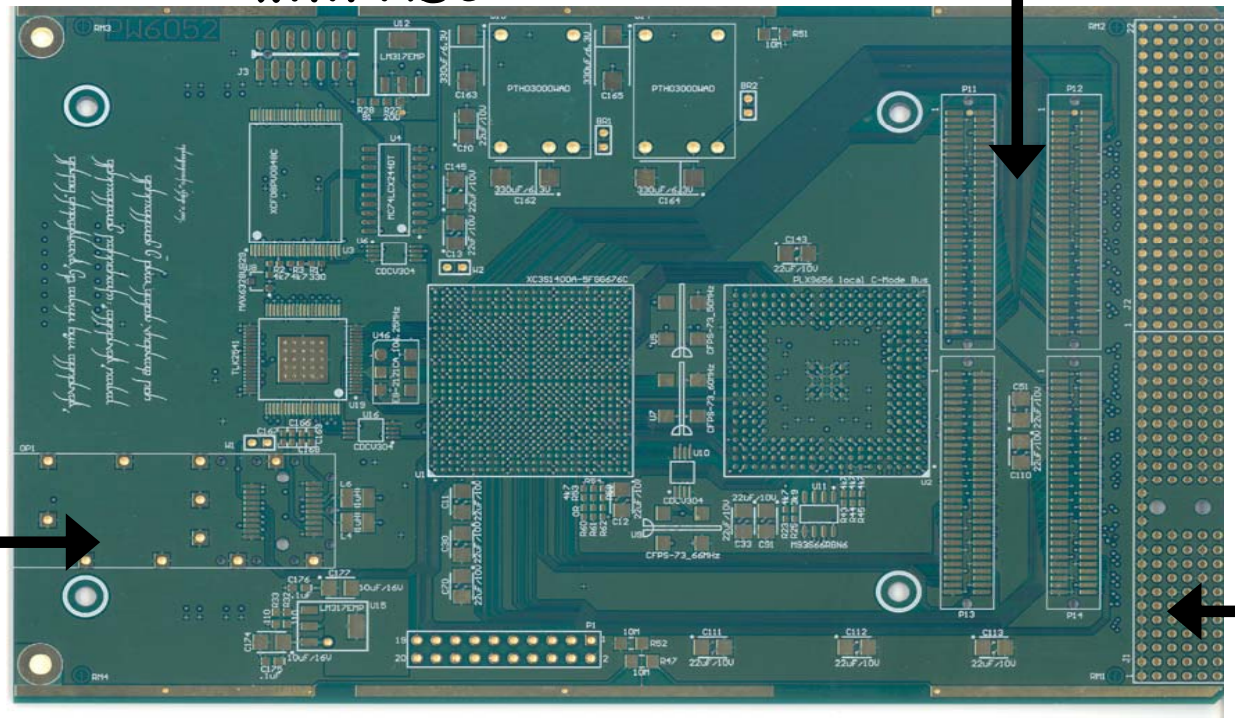


ADC board within pnCCD controller, hosts

- 4 ADCs, 14bit, 50MSPS high-resolution ADCs
- FPGA carrier board, configured via Compact-PCI bus
- Controll of ADC (e.g. analog offset adjustment, gain settings, readout mode)
- Check for data integrity
- Communication via 2.5 Gbit/s optical link with DAQ-PC
  - Handshaking via special characters
  - fast down-stream mode
- Max. Data speed 100 Mbyte/sec.

ADC sub-system - II

CMC-connectors for
board-to-board conncetion
with ADC

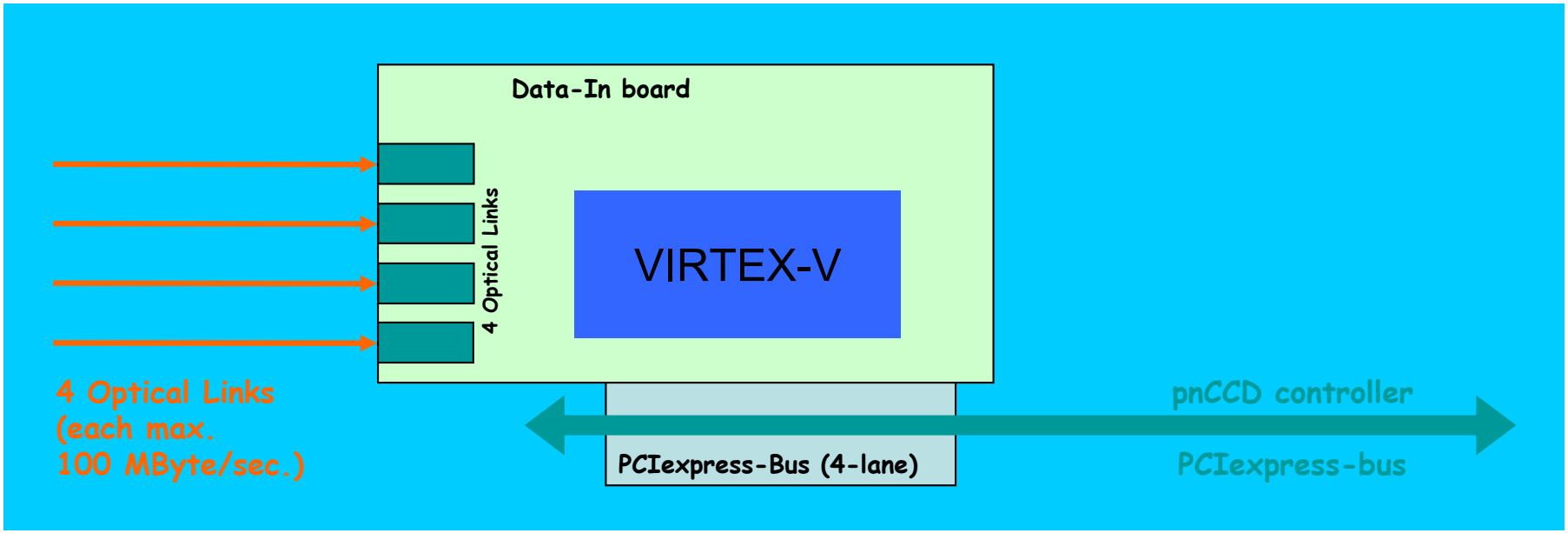


Optical link

64bit cPCI interface

Photography of cPCI-DAQ board
Status: Dec. 05, 2008
Fully equipped and under test now

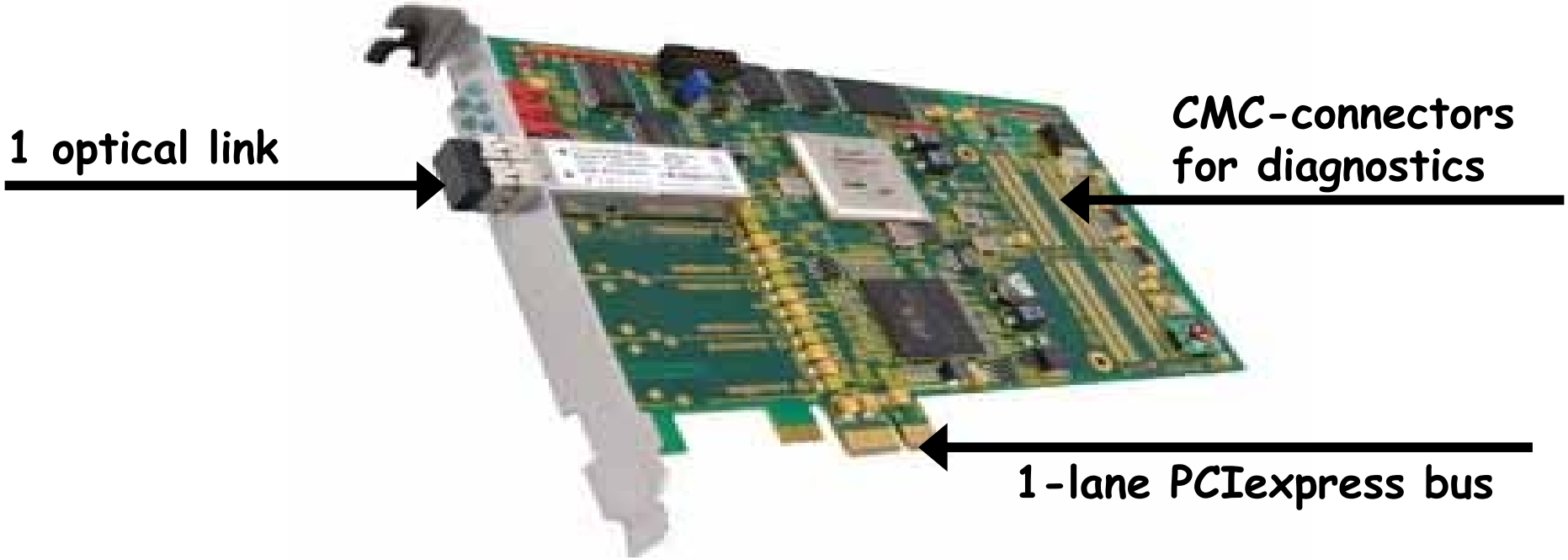
High-speed data interface - I



DAQ board within pnCCD Control-PC, hosts

- 4 optical links, 2.5 Gbit/s
- Communication with up to 4 ADC-boards from pnCCD controller
- Max. Data speed 100 Mbyte/sec. each
- VIRTEX-V FPGA
- 4-lane PCIexpress bus connection
- Check for
  - data integrity
  - communication status
  - optical connection status
- Sorting of data (line structure of pnCCD) → low latency
- Future option: Real-Time Data correction and reduction

High-speed data interface - II



Photography of 1st prototype of high-speed data interface board
Status: Nov. 20, 2008
Under test now

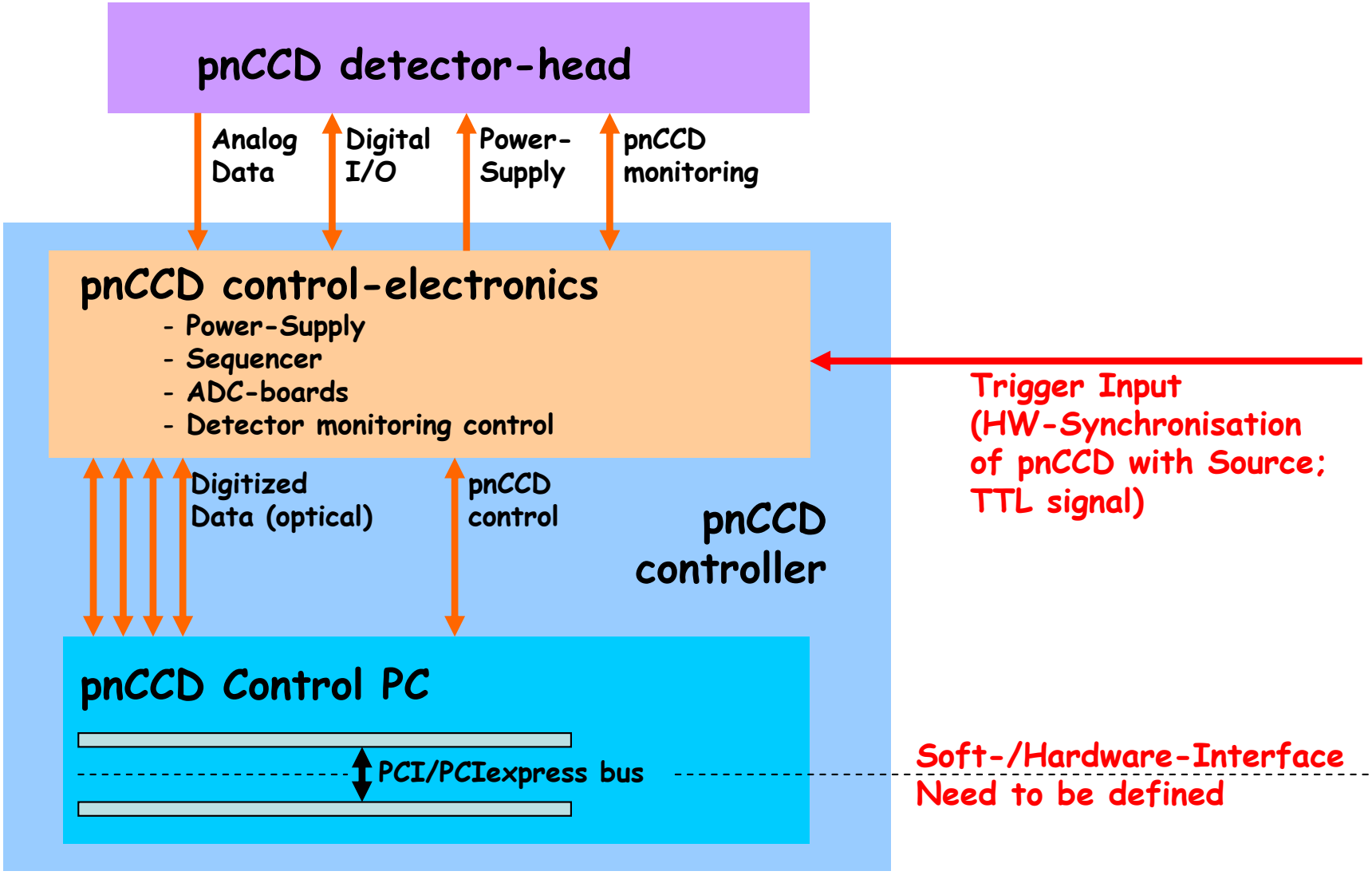
Final board (4 optical links, 4-lane PCIexpress) under construction

High-speed data control PC

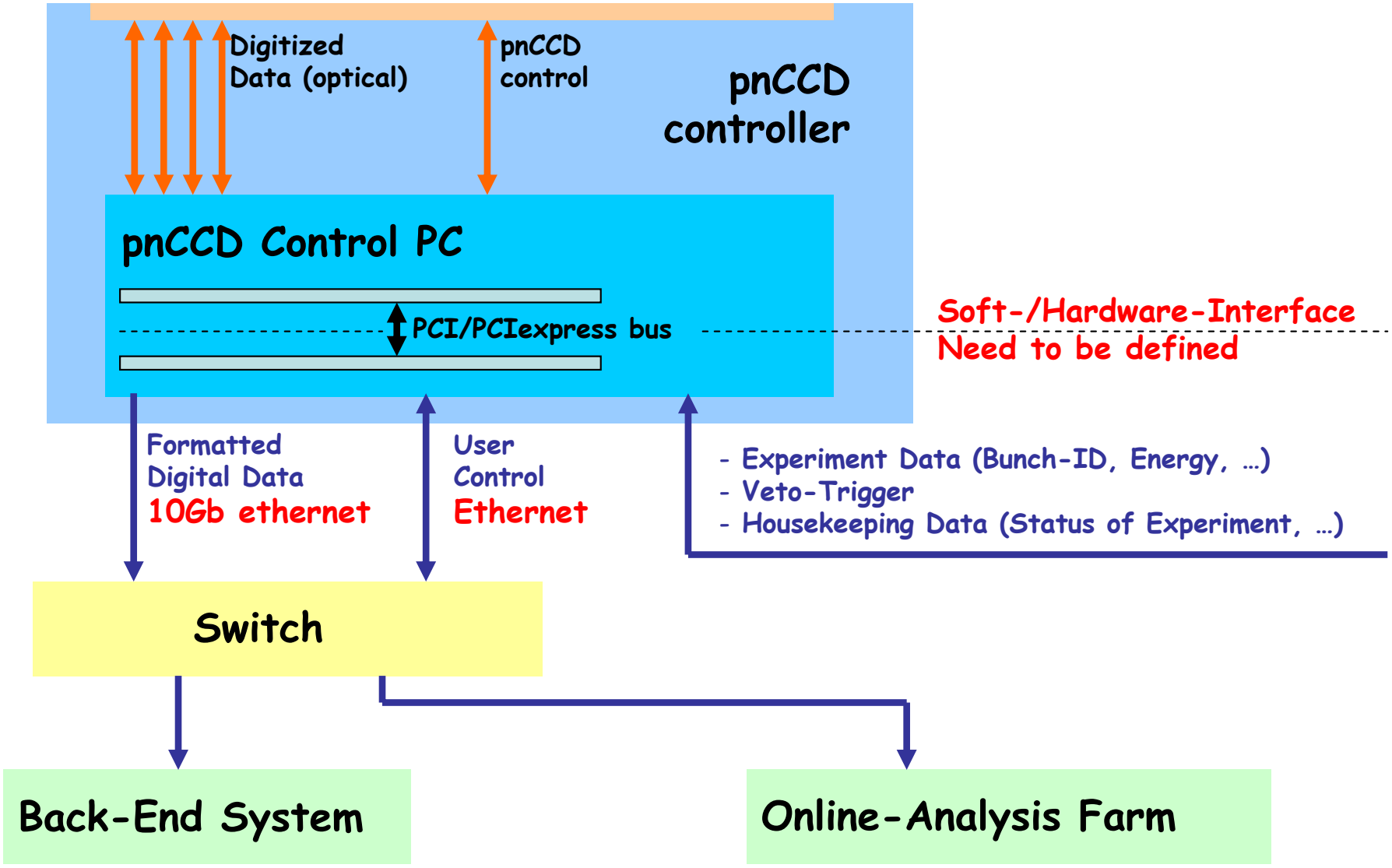
Receives pnCCD data on PCIexpress bus
⇨ max. speed 400MB/s

- Receives pnCCD monitor and house-keeping data
  ⇨ e.g. temperature, power-supply status, ...
- Receives external data
  ⇨ e.g. Bunch-ID, Bunch-time, ... (optional)
- Compiles all data to frame data
  (data format t.b.d.)
- Provides frame data on fast 10-Gb ethernet connection
  (other bus connection optional)
- Local DAQ for diagnostics and commissioning

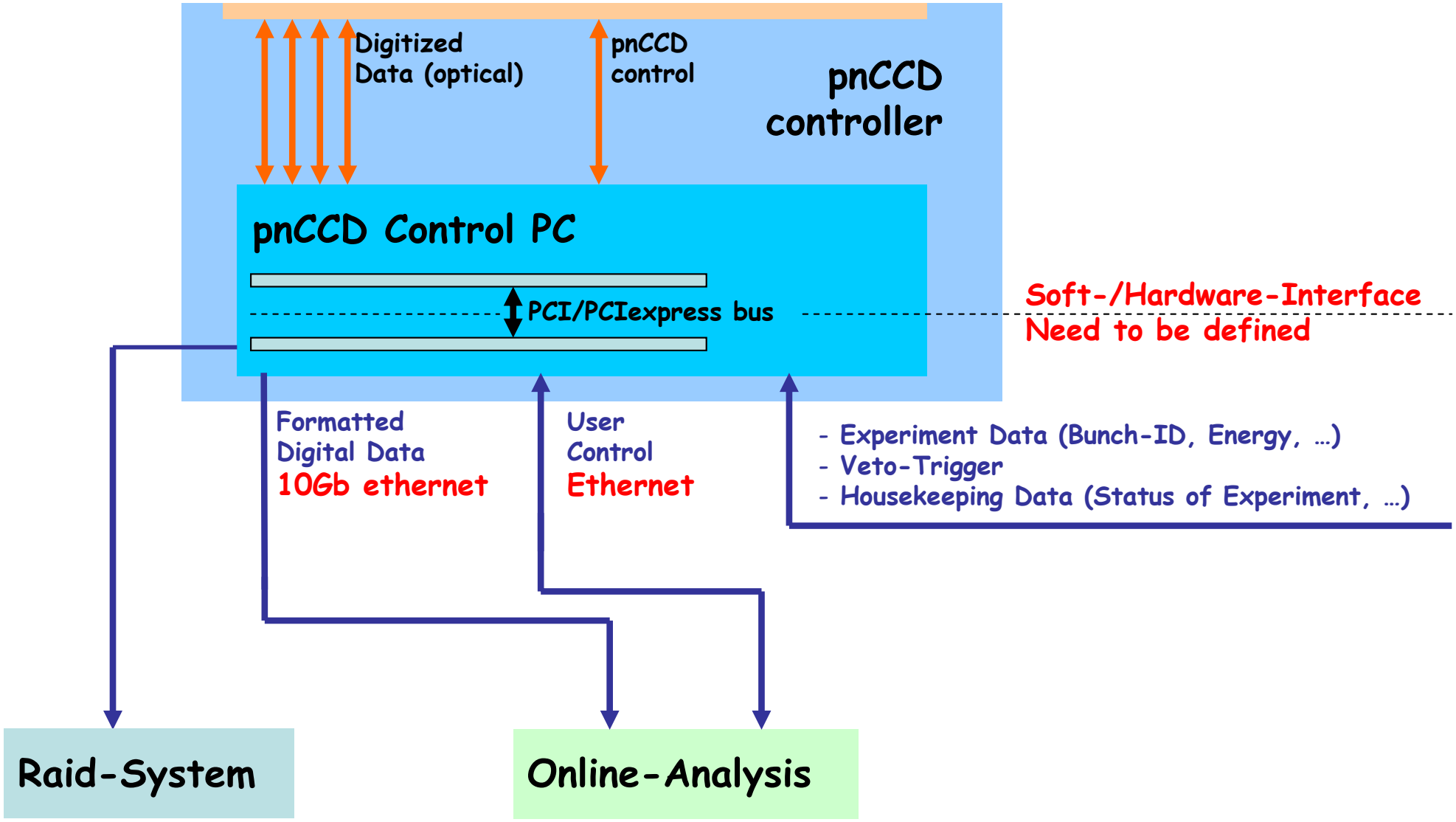
pnCCD controller architecture



pnCCD controller - site integration



pnCCD controller – stand alone



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pnCCD controller – lab version

pnCCD camera controller (19" crate, laboratory version), hosts

- Max. Distance to detector: < 5m (15ft)
- Power-Supply
  - potential-free low-noise DC voltages
  - fully computer controllable
- Sequencer
  - 5ns/10ns 32bit pattern generator
  - LVDS conform differential signal levels
- ADC-boards
  - 4 ADC-boards, hosting 4 high-speed ADCs each
- Detector monitoring control
  - detector temperature control
  - power supply status

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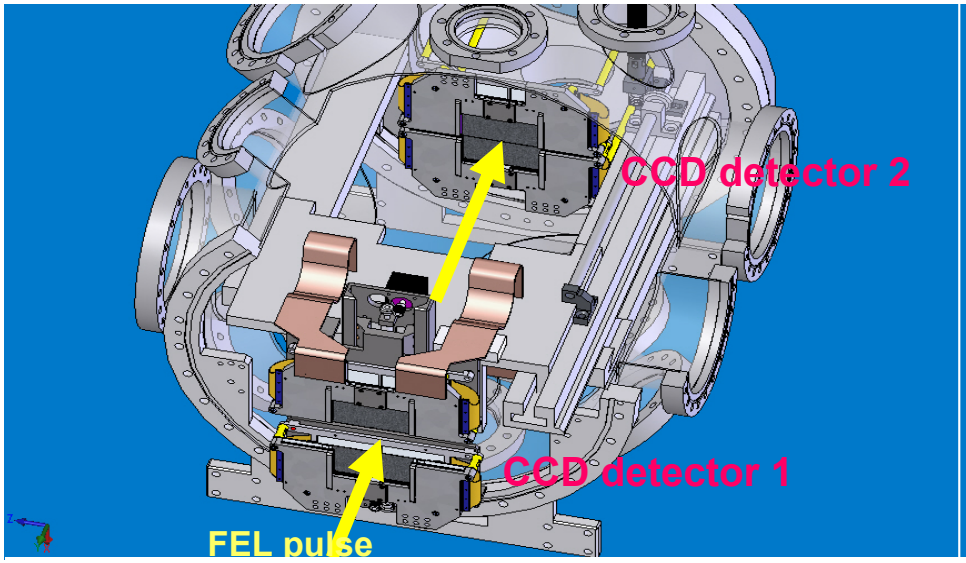
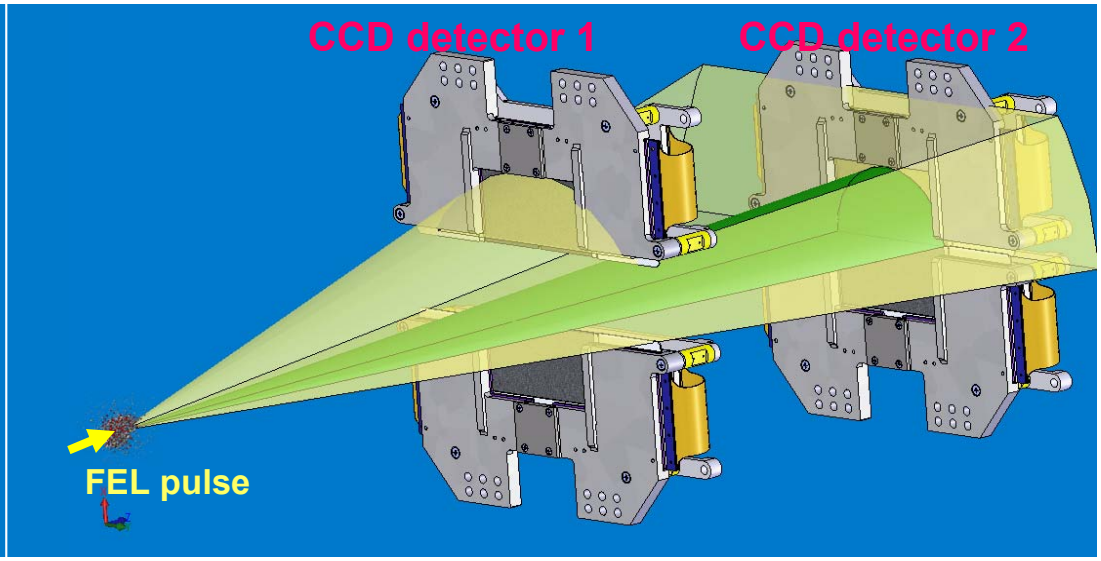
Integration in „CAMP“ setup



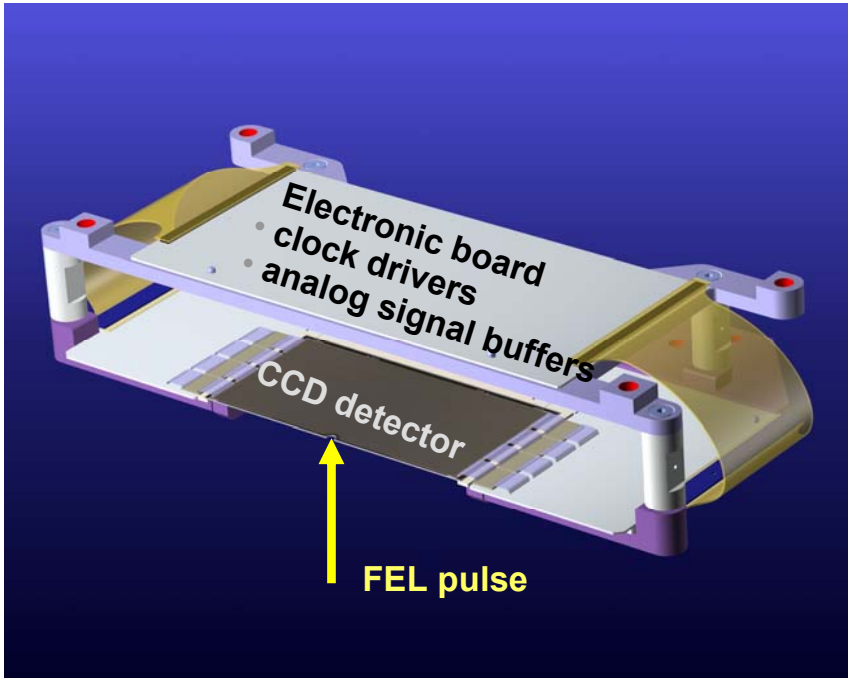


Two detectors are placed behind each other to
- cover a are large solid angle up to 60°
- increase angular resolution for in the center region up to 0.5 arc sec.

The direct FEL beam passes through the central hole of the CCD detectors and hits a high count-rate detector which is placed behind the second CCD detector for an absolute calibration of the number of photons per pulse.

Two entire detector systems are going to be setup!

pnCCD detector module



Each detector module hosts one pnCCD detector chip comprising 512×1024 pixel together with

- eight 128-channel, low noise readout ASICs
- CCD clock drivers
- analog signal buffers

UHV compatible materials are used as much as possible.

One full detector system is composed of two of these modules which allow to be mounted on moving vacuum stages.

Summary

- 2 entire pnCCD systems will be setup in „CAMP" system
- Each system is autarkic
  - ⇨ Detector and system control can be joined
  - ⇨ Control via standard ethernet
- Each system generates 240MByte/s of raw data
  - ⇨ in total 480MB/s raw data are generated
- High speed data transfer via 10Gb ethernet
  - ⇨ custom made interface based on PCIexpress possible