HPS Trigger DAQ Review, JLAB February 25, 2014

TDAQ - SVT Integration

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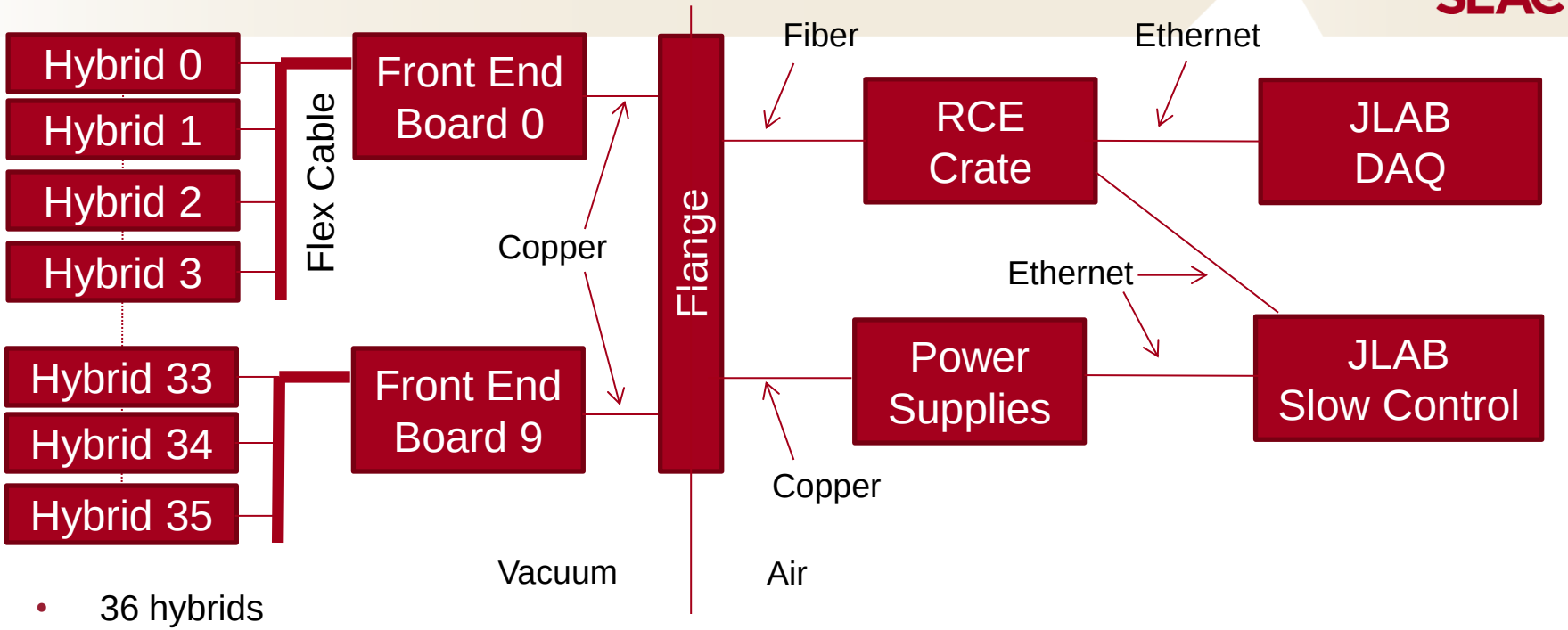
Overview

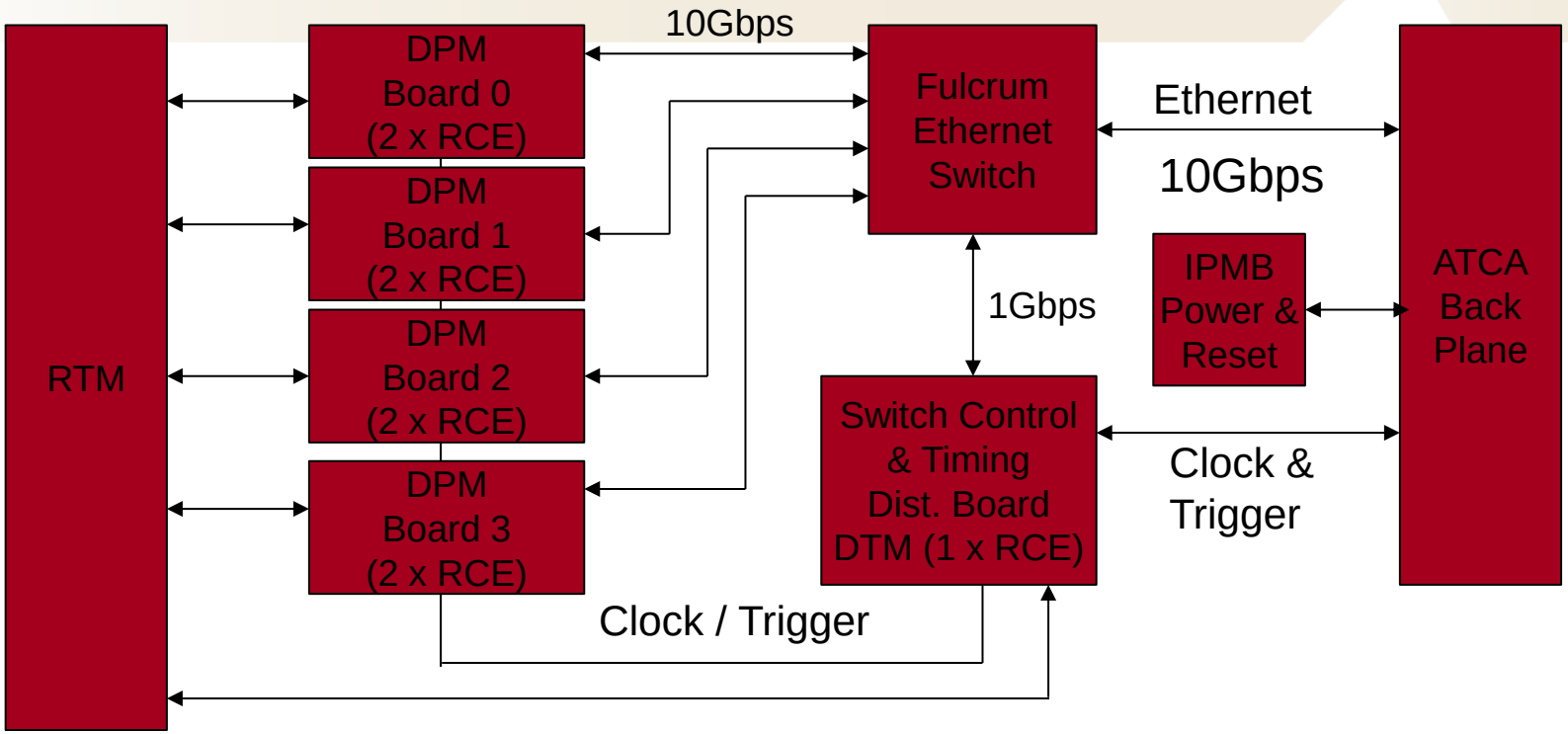
- SVT DAQ Overview
- Trigger Implementation in SVT
- Trigger distribution in SVT
- ROC Instances in SVT
- CODA States

SVT Overview



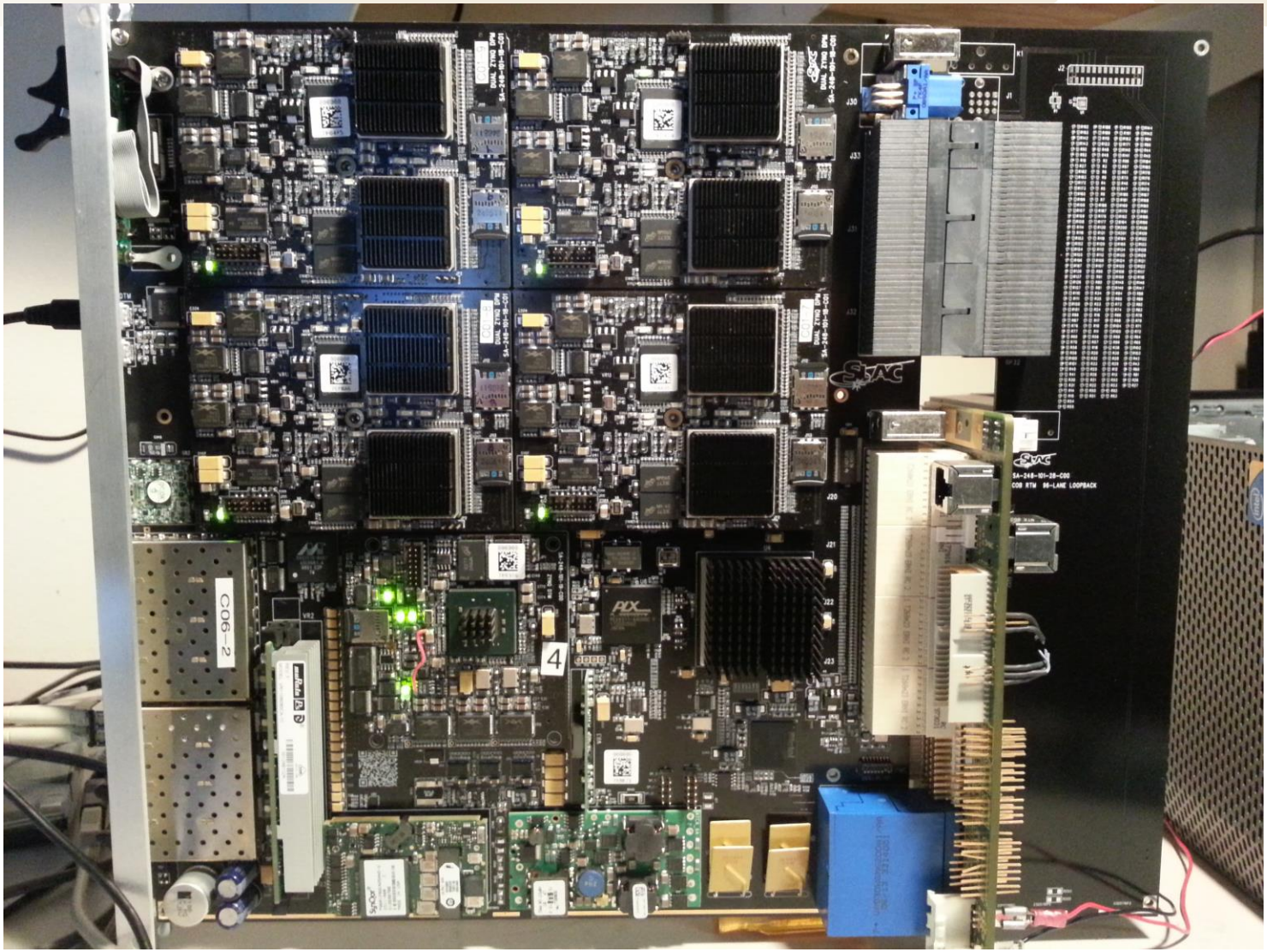
- 36 hybrids
  - 12 in layers 0 – 3 (4 per layer, 2 top, 2 bottom)
  - 24 in layers 4 – 6 (8 per layer, 4 top, 4 bottom)
  - 3.33Gbps raw ADC data per hybrid
- 10 front end boards
  - 4 servicing layers 1 – 3 with 3 hybrids per board
    - 10 Gbps raw ADC data per board
  - 6 servicing layers 4 – 6 with 4 hybrids per board
    - 13 Gbps raw ADC data per board
- RCE crate for event building and data reduction

SLAC Gen3 COB (Cluster on Board)



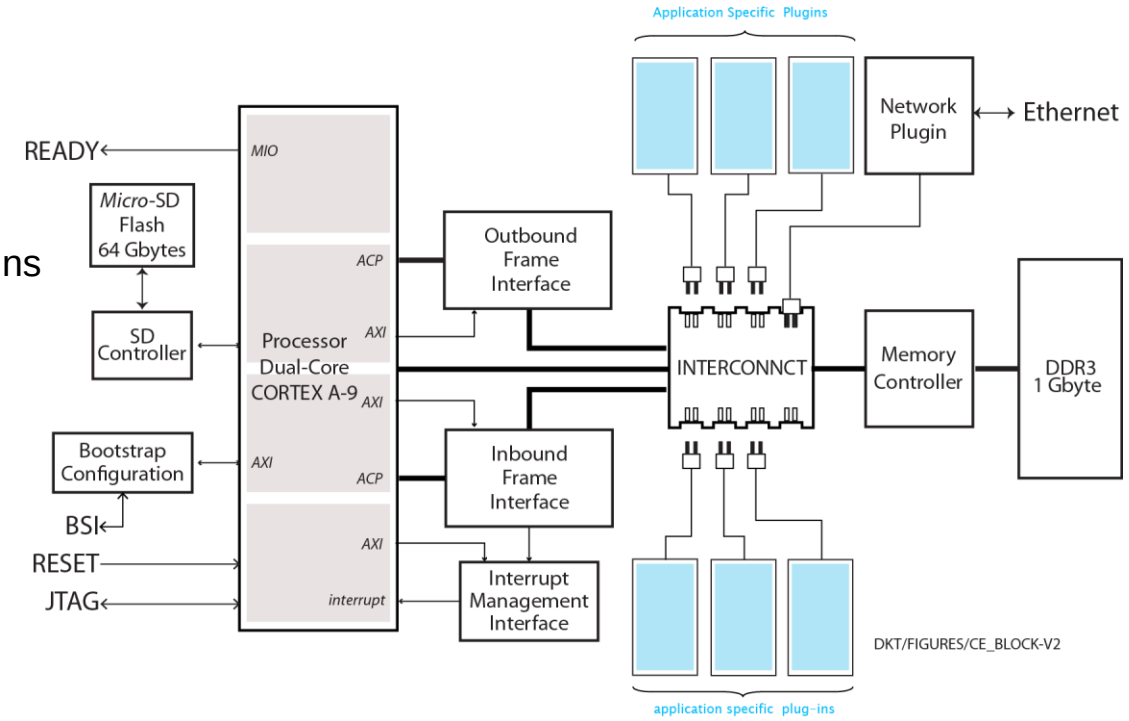
- Supports 4 data processing FPGA mezzanine cards (DPM)
  - 2 RCE nodes per DPM
  - 12 bi-directional high speed links to/from RTM (GTP)
- Data transport module (DTM)
  - 1 RCE node
  - Interface to backplane clock & trigger lines & external trigger/clock source
  - 1 bi-directional high speed link to/from RTM (GTP)
  - 6 general purpose low speed pairs (12 single ended) to/from RTM
    - connected to general purpose pins on FPGA

RCE GEN3 COB



RCE (Reconfigurable Cluster Element)

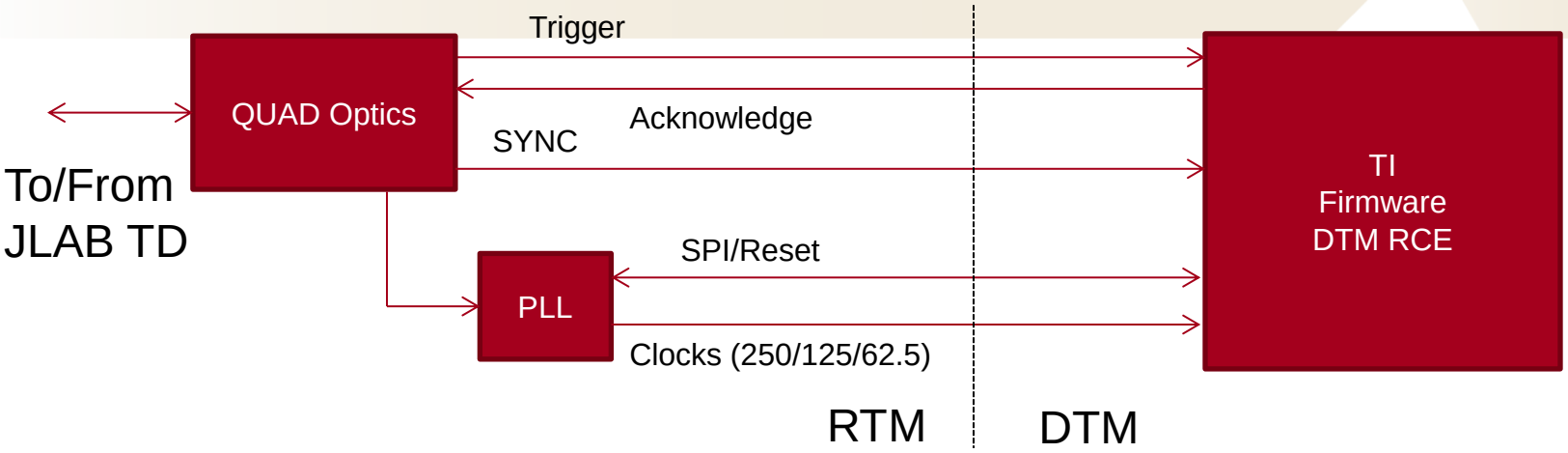
- Two versions
  - 2 x Zynq XC7Z045 FPGA for DPM
  - 1 x Zynq XC7Z030 FPGA for DTM
- ARM (dual-core) A-9 @ 900 MHZ
  - 1 Gbyte DDR3
  - Micro-SD (removable)
  - 10-GE MAC
- Bootstrap configuration via IPMI
- Frame based Socket Interface for plugins
  - 10Gbps bandwidth into memory
- Software (bundled with CE):
  - Linux
    - Based on 3 series kernel
    - Archlinux distribution
  - RTEMs
    - Open Source Real-Time kernel
    - POSIX compliant interfaces
  - TCP/IP stack
  - Plugin socket library
- External serial interfaces
  - 12 GTX channels per RCE (96 per COB)
  - Up to 10Gbps



SVT RCE Allocation

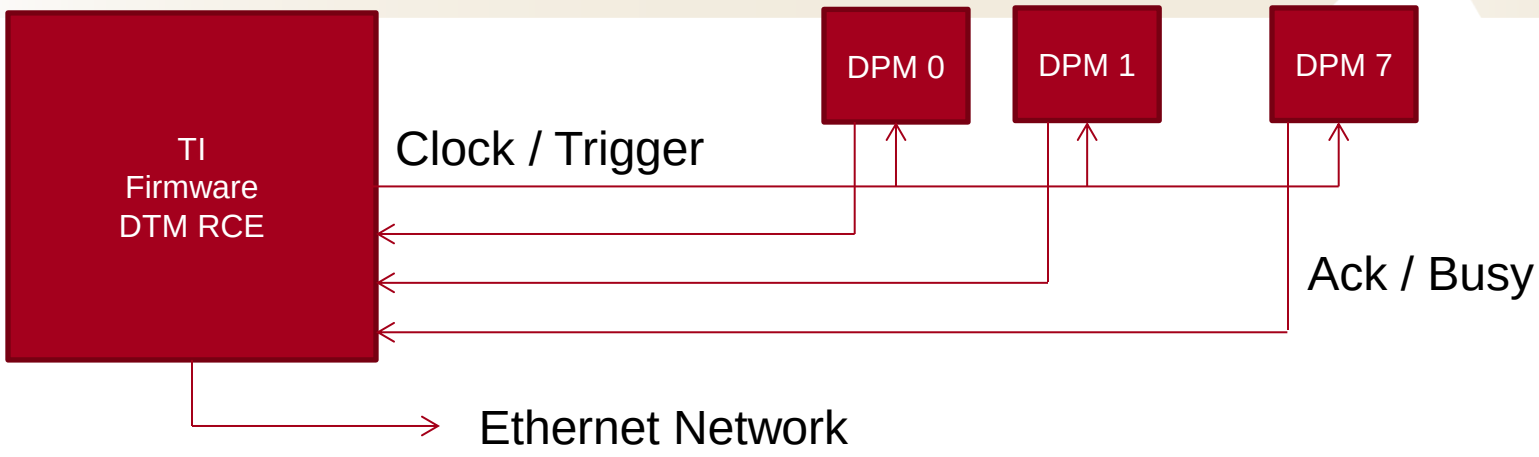
- Two COBs utilized in the SVT readout system
  - 16 RCEs On DPMs (2 per DPM, 4 DPMs per COB)
  - 2 RCEs on DTMs (1 per DTM, 1 DTM per COB)
- 7 RCEs on each COB process data from ½ SVT
  - 18 Hybrids total per COB
  - RCE 0 = 2 hybrids (layer 0)
  - RCE 1 = 2 hybrids (layer 1)
  - RCE 2 = 2 hybrids (layer 2)
  - RCE 3 = 3 hybrids (3 from layer 3)
  - RCE 4 = 3 hybrids (1 from layer 3 / 2 from layer 4)
  - RCE 5 = 3 hybrids (2 from layer 4 / 1 from layer 5)
  - RCE 6 = 3 hybrids (3 from layer 5)
- RCE 7 on COB 0 manages all 10 FE Boards
  - Configuration and status messages
  - Clock and trigger distribution to FE boards & hybrids
- RCE 7 on COB 1 has does not have an SVT specific purpose

SVT Trigger Interface



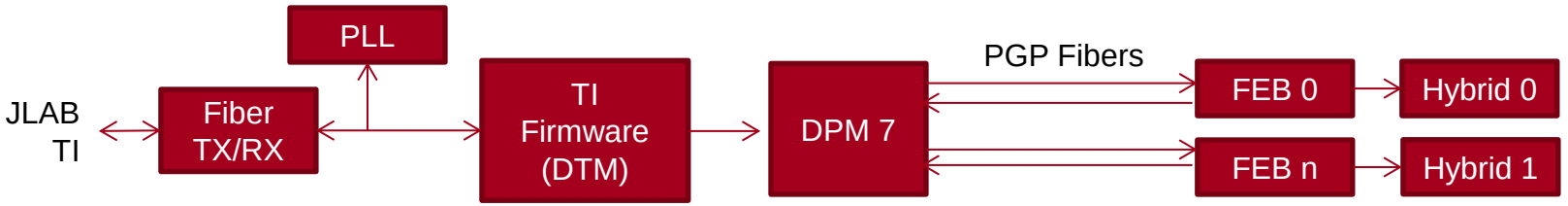
- Replicates portion of JLAB TI Board
- Quad optics and PLL exist on RTM
- TI firmware implemented in RCE FPGA
- Fully allocated available signals between RTM and DTM
  - 1 high speed pair for trigger & SYNC
  - 1 low speed pair for SYNC
  - 2 low speed pairs for PLL SPI and Reset signals
  - 3 low speed pairs for PLL generated clocks (250/125/62.5 Mhz)

SVT Trigger Distribution



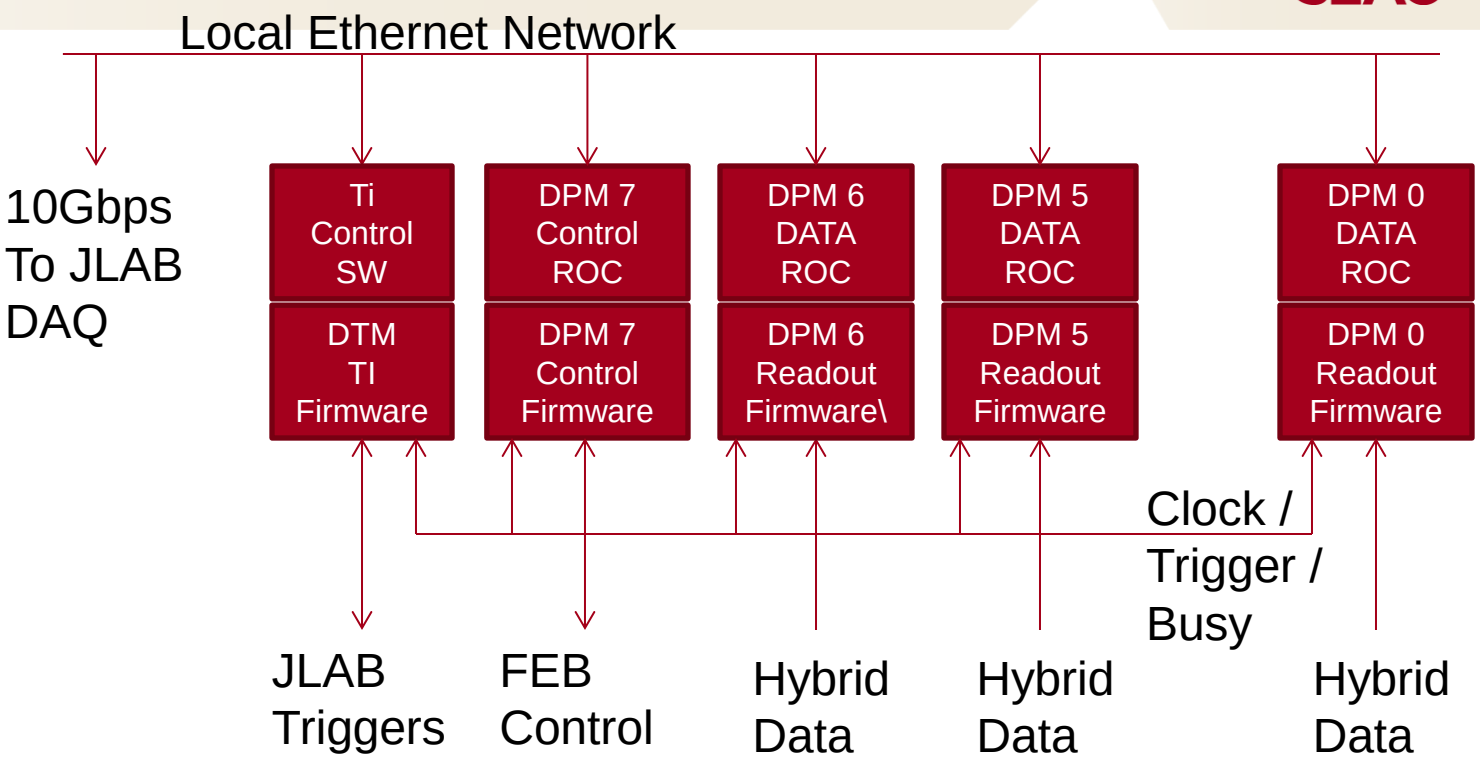
- DTM FPGA has ability to distribute clock and trigger to DPMs
  - Clock and trigger wired as fan out to DPMs
  - Individual feedback signals from each DPM
- 1 pair for clock fan out
- 1 pair for trigger fan out
  - 125Mhz serial protocol transfers 8-bit codes (easily expanded to longer words)
  - Used to distribute event codes to DPMs
    - System clock sync, APV25 sync & JLAB triggers
- 1 pair per DPM for feedback
  - Similar 8-bit op-code
  - Readout and trigger acknowledge
  - Busy
- Ethernet network used to distribute bulk trigger records to DPMs

Front End Timing Distribution



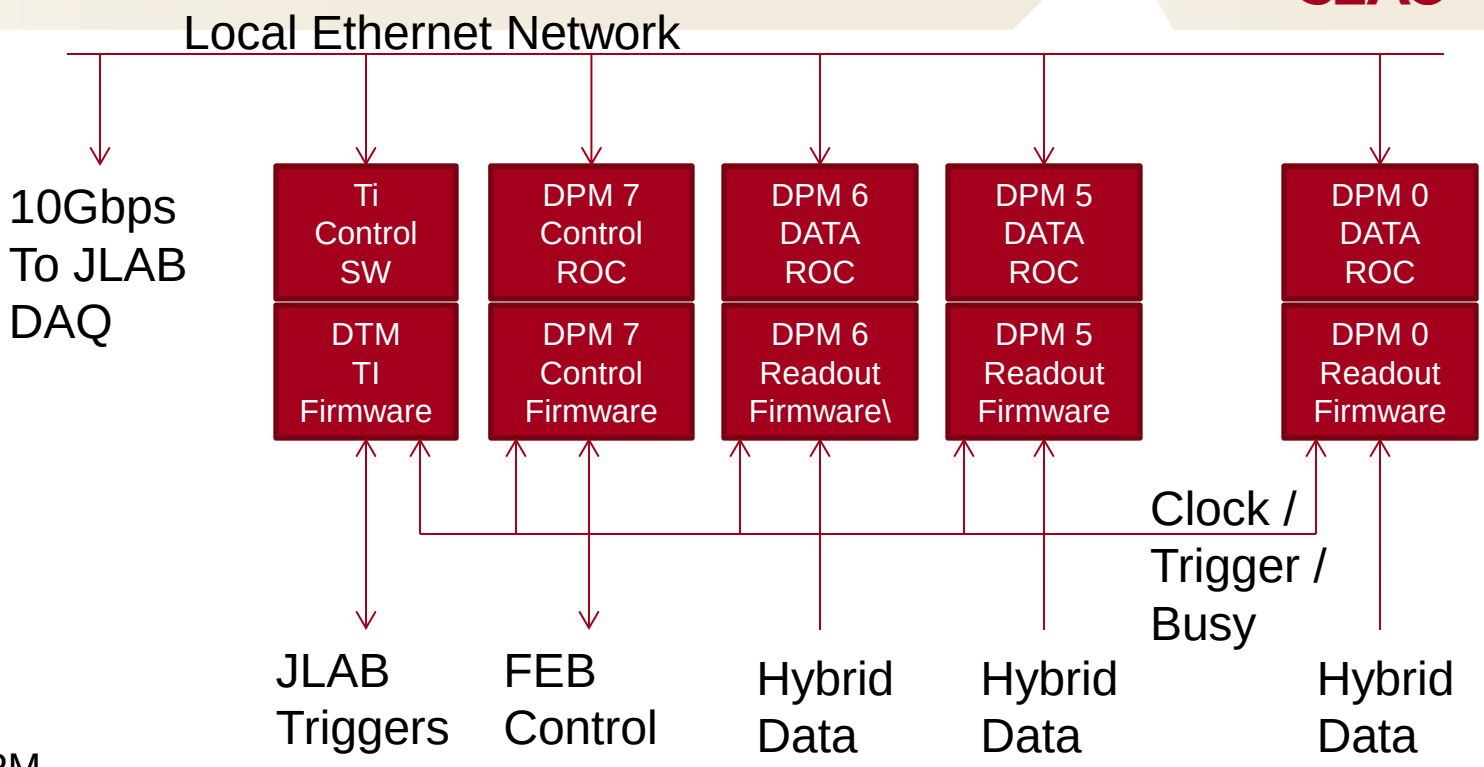
- Control DPM forwards timing information to front end boards over PGP
  - Clock encoded into serial data stream which the front end board recovers
  - Fixed latency path for encoded PLL reset and trigger signals
  - Upstream link echoes encoded clock and encoded signals back to DPM
  - Round trip latency is measured and compensated for by adjusting delay elements in DPM
    - Front end boards aligned in time domain

ROC Instances On SVT



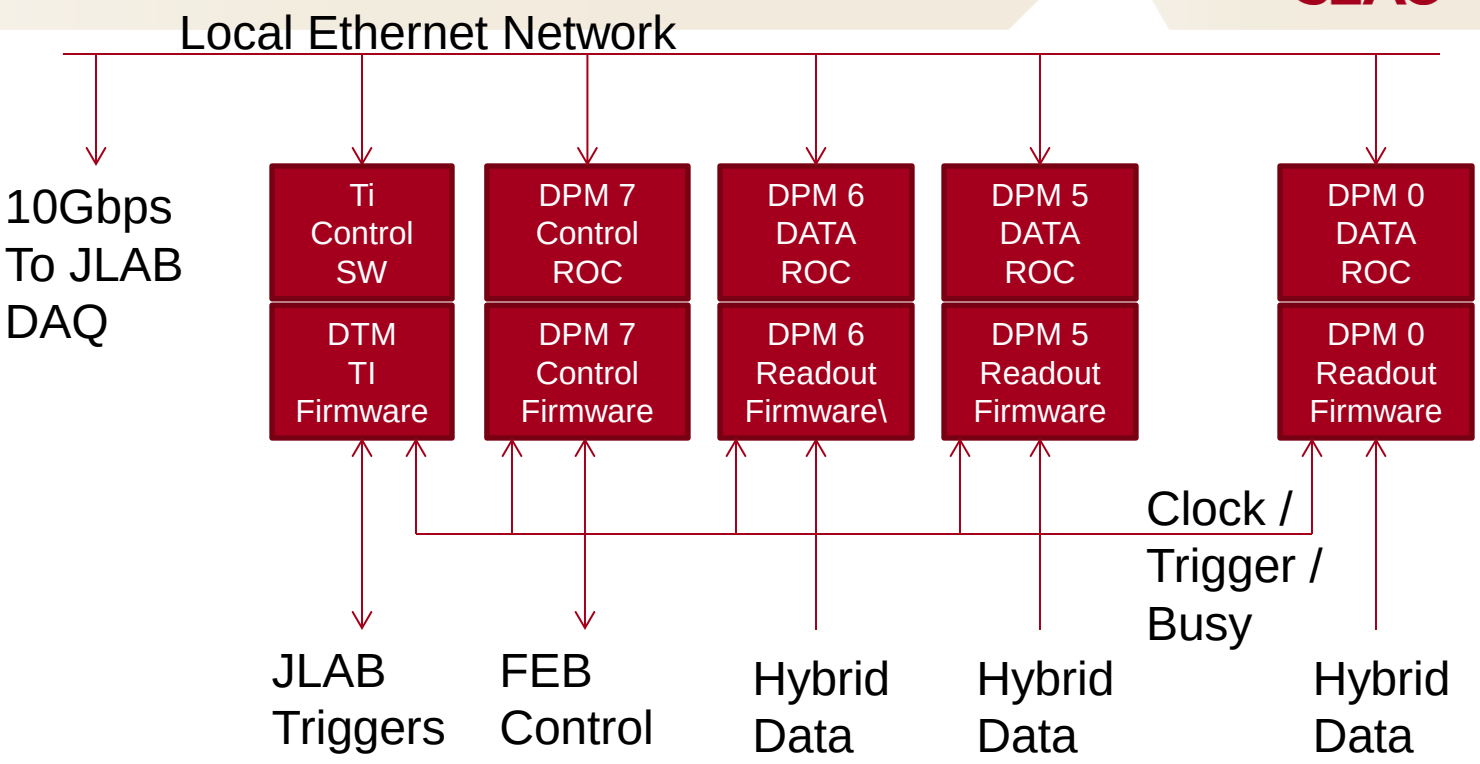
- Data DPM
  - Data processing ROC application
  - Builds event record for 2 or 3 hybrids
    - APV25 ADC Data
    - Hybrid environmental data
  - Operates as slave when interfacing to TI firmware
  - Clock and trigger received over COB signals
  - Busy and acknowledge passed over COB signals
  - Trigger event data passed over Ethernet from TI control software

ROC Instances On SVT



- Control DPM
  - FEB control and configuration
  - Trigger processing ROC application
  - Formats FEB environmental event data
  - Master ROC application for TI firmware
    - Register access over TCP/IP to local TI software
  - Clock and trigger received over COB signals
  - Busy and acknowledge passed over COB signals
  - Trigger event data passed over Ethernet from TI control software

TI Control Software



- TI Control Software
  - Direct access to TI register space
  - Slaves to control ROC application for CODA transitions
  - Bridge to data ROC applications
  - Sends out readout block trigger record to data DPMs & control DPM

CODA States

- Download
  - Control ROC
    - Opens link to control software application
    - Configures FEBs and Hybrids
    - Configures data processing DPM firmware
    - Configures TI firmware
  - Data ROC
    - Opens link to data path software
- Prestart
  - Control ROC
    - Generates APV25 sync command through TI bridge software
    - Monitors APV25 sync status
  - Data ROC
    - Registers with TI through TI bridge software
- GO
  - Data ROC
    - Retrieve trigger/block info from TI through bridge software
    - Enable local data path
  - Control ROC
    - Enable the TI to accept triggers when all data DPMs have retrieved trigger/block information

CODA States

- Trigger
  - Data ROC
    - Receives trigger mask from DTM over COB signals
    - Send acknowledge over COB signals to DTM
    - Receive associated trigger block data over TCP/IP
  - Control ROC
    - Send triggers and mask data over COB signals
    - Send trigger block data to data DPMs over network
- End
  - Control ROC
    - Request TI firmware to disable
    - Wait for ROCs to acknowledge last block
    - Disable triggers
  - Data ROC
    - Acknowledge last triggers
    - Disable data path