HPS TDAQ Review: DAQ

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Requirements

- 50kHz event rate
- 100MB/s data rate (calorimeter 25MB/s, muon 6MB/s, SVT 33MB/s)
- Dead time < 1%

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DAQ: System Overview

- Calorimeter Readout: 442 channels of 12bit 250MHz Flash ADCs for Calorimeter (2 VXS crates)
- SVT readout system (1 ATCA crate)
- Optional: 85ps resolution pipeline TDCs with discriminators
- Maximum 5 crates (2 VXS, 1 ATCA, 2 VME64(opt))
- JLAB CODA DAQ software

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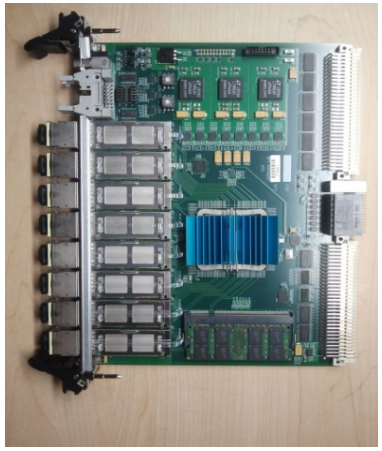
DAQ/Trigger: all modules are available

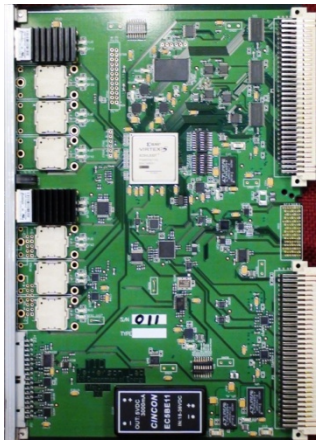
FADC250 Flash ADC

Crate Trigger Processor



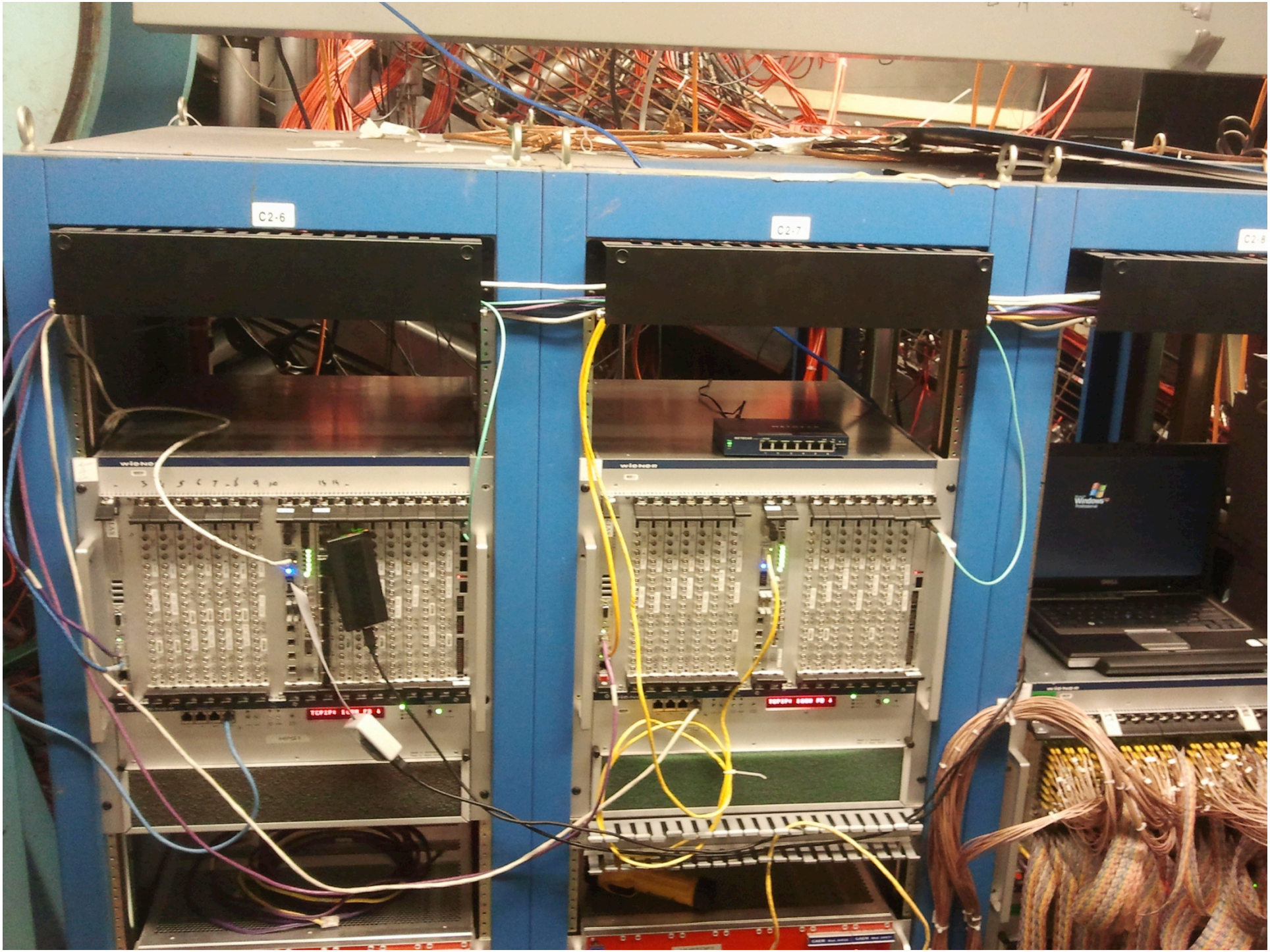
Sub-System Processor

Signal Distribution

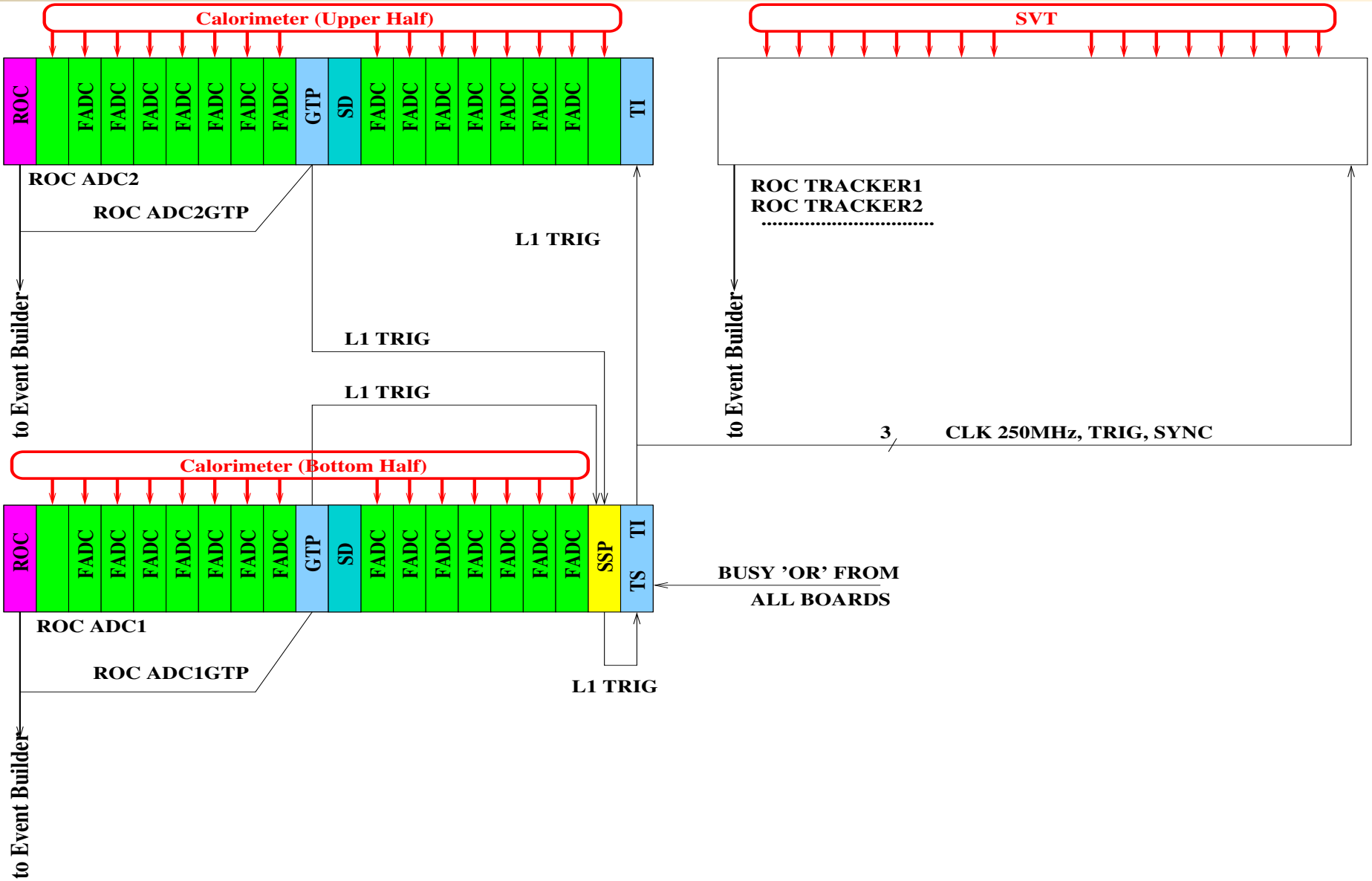


Trigger Interface

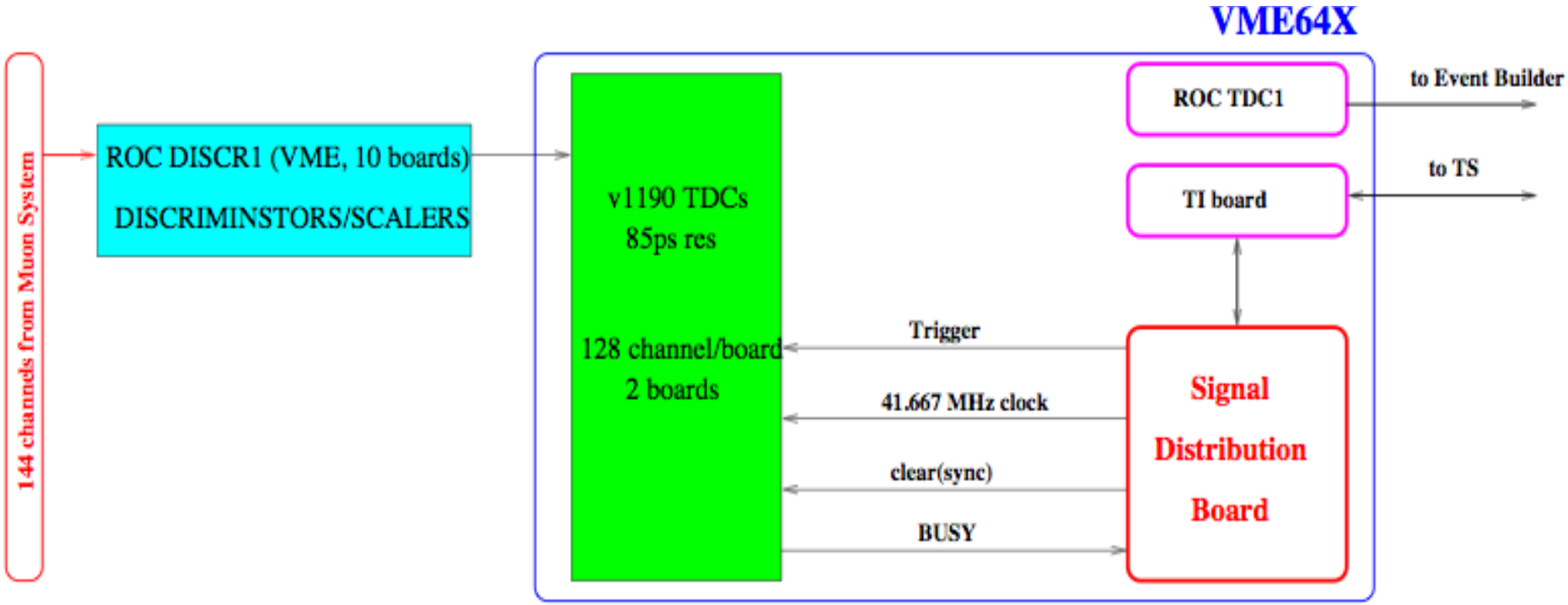

EXIT


C2-6
C2-7

DAQ/Trigger: Flash ADC and Trigger System (VXS)



DAQ: Pipeline TDC System (VME64X/VME)

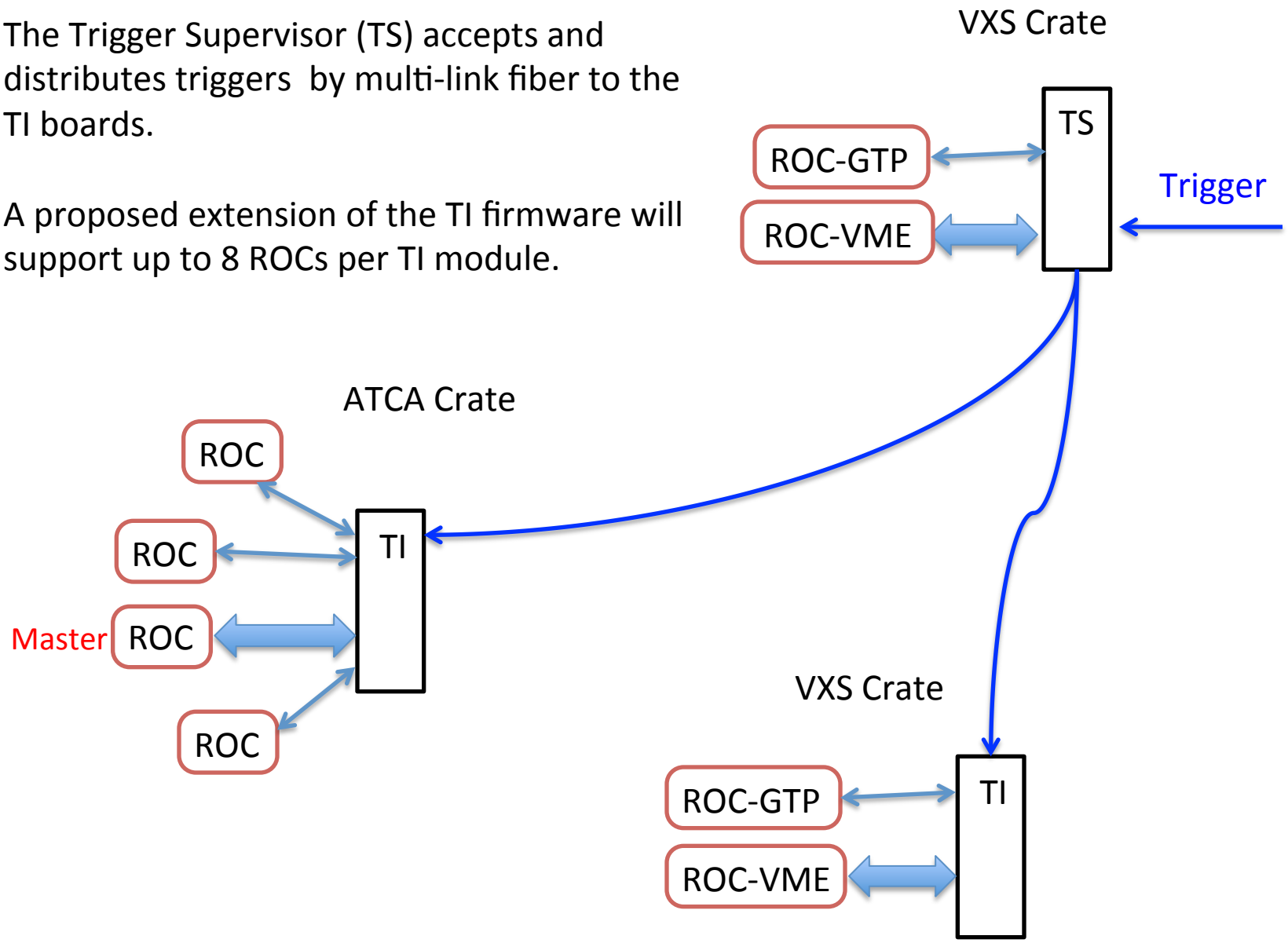


NOTE: will not use it if FADCs produce timing and scalers (timing is not tested yet)

The CODA Trigger Distribution System With TI as TS

The Trigger Supervisor (TS) accepts and distributes triggers by multi-link fiber to the TI boards.

A proposed extension of the TI firmware will support up to 8 ROCs per TI module.



DAQ: SVT integration

- CODA was ported on ARM processor (zed board) with SLAC help and successfully tested with dummy readout list
- TI firmware keeps changing, SVT-TI section must be adjusted accordingly
- Configuration procedures must be integrated
- Starting May 2014, JLAB part of DAQ will be ready for integration with SVT

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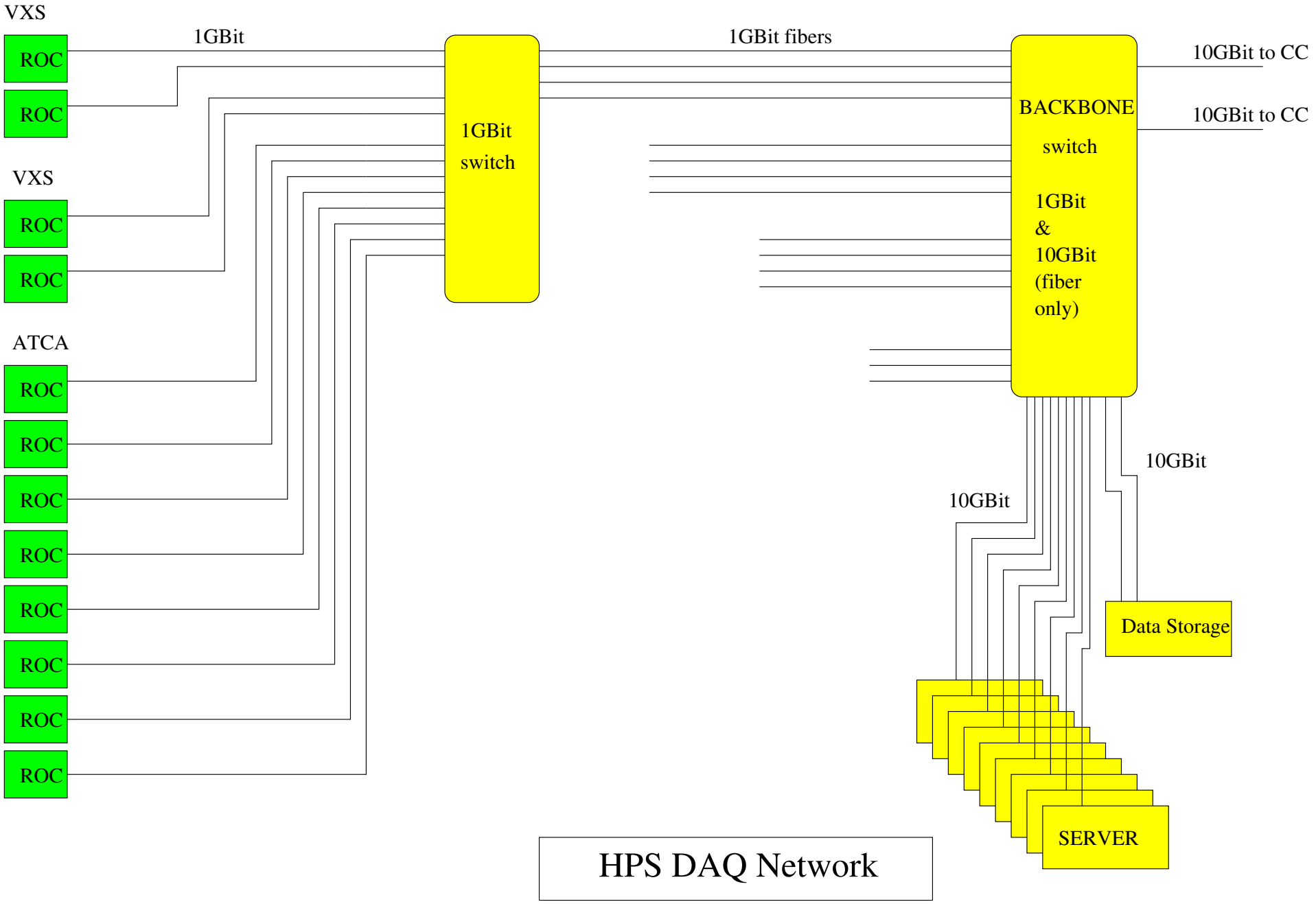
VXS
ROC
ROC
VXS
ROC
ROC
ATCA
ROC
ROC
ROC
ROC
ROC
ROC
ROC
ROC
1GBit
1GBit
switch
1GBit fibers
BACKBONE
switch
1GBit
&
10GBit
(fiber
only)
10GBit to CC
10GBit to CC
10GBit
10GBit
Data Storage
SERVER
HPS DAQ Network


4200ACV
4200ACV
hallb-rtr
Catalyst
4506-E
1-12 68-net
13-24 69-net
25-36 168-net
37-48 96-net

Timeline

- 2 VXS crate setup is ready, supporting trigger system development conducted by Ben Raydo: now - March 15
- TDAQ commissioning starts (Ben and Sergey): March 15 – May 1, with possible extension to May 31
- Ready for SVT integration: June 1

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Conclusion

- DAQ in 2012 test run was nearly final configuration, do not expect any problems in final HPS DAQ system
- JLAB part of DAQ hardware 100% available and installed, trigger development is in progress
- JLAB part of DAQ will be ready by the end of May; SVT integration have to follow