LAMP PNCCD User Manual

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April 11, 2014

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Contents

1 Introduction

The LAMP PNCCD camera system is a low-noise high-speed CCD detector designed for X-ray imaging and spectral analysis at LCLS and is the successor to the CAMP PNCCD detector [**?**]. As well as with CAMP, the LAMP camera features two detector planes with 1024x1024 pixels sized 75 µm on a back-side illuminated fully depleted PNCDD. Additionally to the outstanding imaging capabilities the detector can also measure photon energies from 50 eV to 25 keV and single photons can be detected. The typical frame rate is 120 Hz. The PNCCD detectors in the CAMP (CFEL-ASG-Multi-Purpose) chamber [**?**] stimulated experiments carried out from December 2009 to July 2012, including measurement of fluorescence of highly ionized noble gas atoms, nanocluster dynamics, nanocrystallography, and recording diffraction patterns for 3D reconstruction of small particles and biological samples like proteins and viruses. A list of publications from Max Planck Institute for Extraterrestrial Physics with several papers about PNCCDs can be found at `http://www.hll.mpg.de/07_publication/index.html`.

In chapter 2 a brief overview of the complete detector system is given. The basic physical principles of the PNCCD detector are outlined in chapter 3. The mechanical setup (mounting and unmounting the detector modules) is described in a separate manual. The setup of the detector system is divided in electronic setup (chapter 4) and software initialization (chapter 5). Chapter 7 covers the every day beamtime steps for users.

2 System overview

One detector plane consists of two PNCCD detector modules (each 512x1024 pixels), vacuum flex leads, two data boxes, cables (in air) and one control rack with power supplies, timing sequencer, ADCs and IOCs as shown in Figure 1.

Figure 1: LAMP PNCCD camera components for the front plane: Detector modules, vacuum flex leads, data boxes and the control rack. The LAMP vacuum chamber is visualized transparent. The rear detector plane differs only in the length of the vacuum flex leads.

A functional diagram of the electronic components up to the control rack is shown in Fig. 2. As both detector planes are independent, one detector plane can be transferred from AMO to another hutch while the other one is still operational.

The electric connection between detector module and the feedthrough flange is handled by vacuum compatible flex leads. Directly on the air side of the feedthrough flange the data box houses hardware modules for ADC-buffers, Sequencer level translators/drivers and CCD/CAMEX power supply filters. The data box is connected to the control racks with 6 m cables. The control rack houses power supplies, the timing sequencer and the ADCs as well as IOCs and monitoring devices.

Figure 2: Function diagram of the LAMP camera components. Only one half of the detector module is shown for better clarity.

A more detailed scheme of the control rack is shown in Fig. 3. There are two PCs in the control rack. One is dedicated to the data acquisition (DAQ) and is equipped with PCI-bridge to connect to the cPCI rack containing the timing sequencer and the analog-digital converters (ADCs). Data from the ADCs are being routed through the DAQ PC via fibers to fast ethernet (FEZ). A switch connects the regular ethernet to DAQ PC, IOC PC, GPIB gateway and WIENER powersupply. The IOC has mainly the function to communicate with the power supplies (WIENER and R&S) and housekeeping (Keithley).

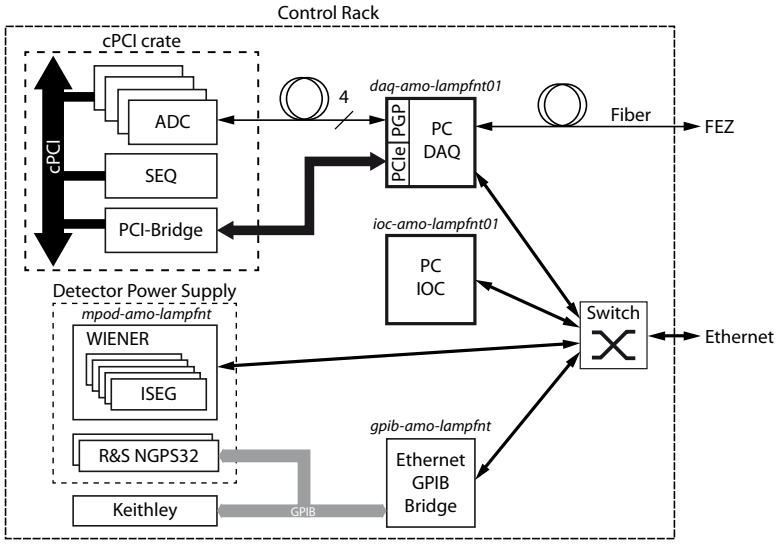
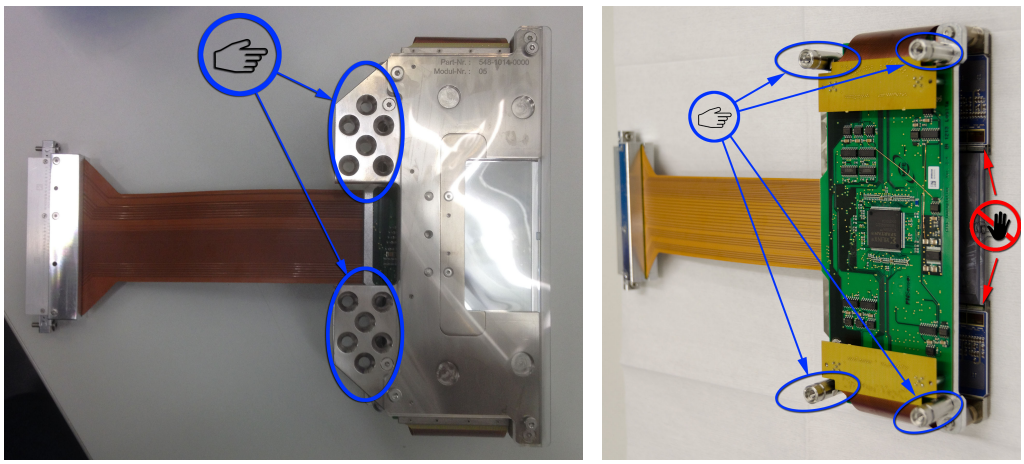


Figure 3: Function diagram of the front Control Rack. The rear Control Rack differs only in the DNS device names: daq-det-pnccd02, ioc-det-pnccd02 and gpib-det-pnccd02.

The detector module consists of a titanium base plate which is directly connected to the LAMP cooling assembly. A photo of one PNCCD detector module with the protective plastic attached is shown in Fig. 4. The PNCCD-chip is glued on a silicon cooling block attached to the titanium base plate for optimal thermal performance. The read out ceramics with the ASICs and filters for supply voltages are mounted on the titanium base plate as well. The detector module with removed inner PCB is shown in Fig. 5. The inner PCB is thermally isolated from the cooled titan base plate by PEEK spacers. On the inner PCB there are further supply voltage filters, drivers for the PNCCD reset and shift registers and buffers for the analog output of the CAMEX ASICs. The FPGA on the inner PCB is for communication between CAMEX ASICs and the Sequencer "SEQ".



(a) front side (b) rear side

Figure 4: Photo of PNCCD detector module. The Module number is imprinted on the titanium base plate. Here the protective transparent plastic shield is mounted on the front side active area. The Hypertac connector and electric flex lead is part of the inner PCB.

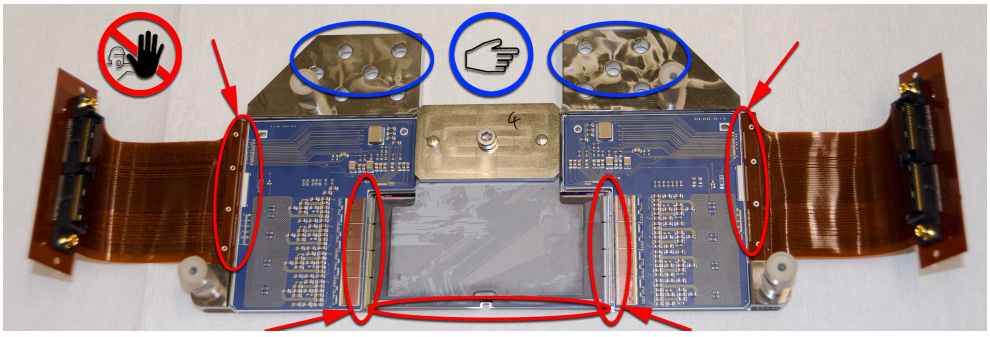


Figure 5: PNCCD Detector module with removed inner PCB (only for visualization purposes). The user must not disassemble the module! The readout ceramics with the CAMEX ASICs bonded to the PNCCD chip are visible. The red areas contain bonding wires and the edge of the PNCCD chip. Do not touch red areas! Only handle module in blue marked areas!

The PNCCD detector module should only be handled with extreme care in a clean environment. It is safe to hold the module at the regions with the 12 mounting screw holes (marked with blue circles) or the four pedestals on the backside of the module. Although the transparent plastic shields protects the front side of the CCD chip from accidental touching, the edge of the CCD and nearby ASICS and bonding wire

connections are unprotected. Take extra care not to touch the detector module anywhere on the CCD or near the CCD-edge or the regions with bonding wires. Avoid cleaning attempts with pressured air near the bonding wires, as they might be bent together and get short circuited.

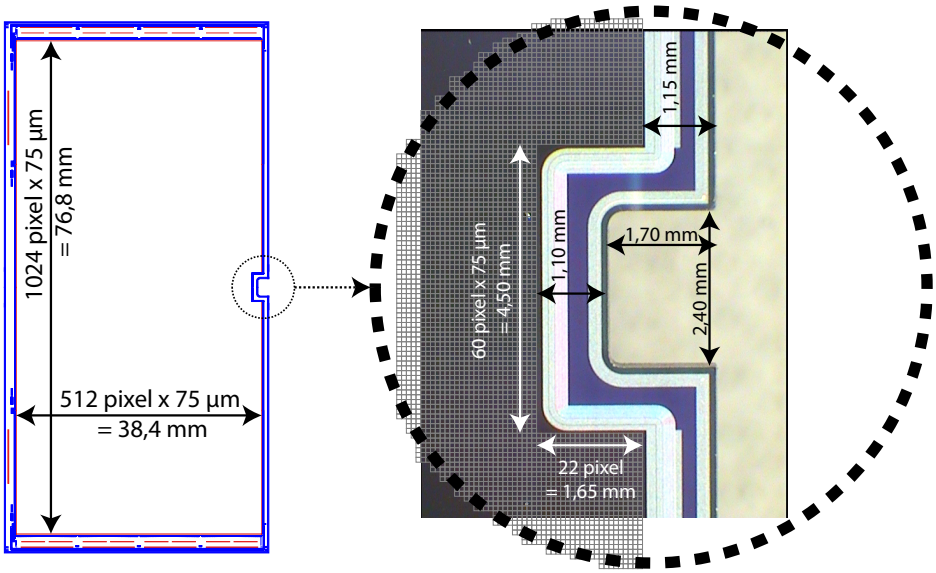


Figure 6: Dimensions of the sensitive area of the PNCCD chip and a magnification of the hole area.

One detector plane is shown in Fig. 7. The viewer looks on the sensitive area of the PNCCDs, which is divided into four quadrants. A complete detector plane consists of a top detector module and a bottom detector module. Each detector module is logically divided in the middle, giving two quadrants per module or four quadrants per focal plane. All detector modules are interchangeable.

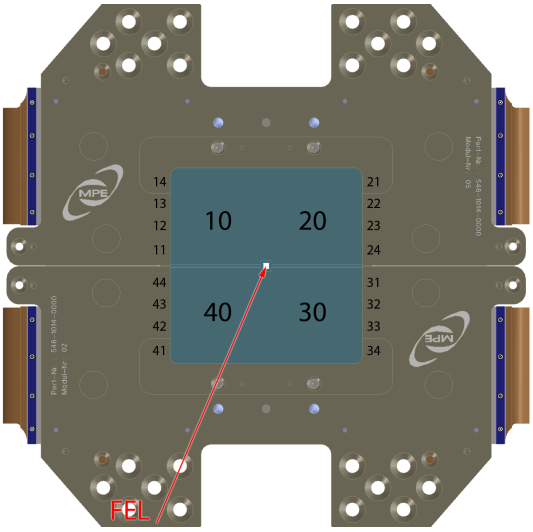


Figure 7: CAD drawing of two detector modules joined for one detector plane. The direction of the FEL is shown with the red arrow. The four quadrants are called 10, 20, 30 and 40. The CAMEX ASICs positions and their names on the detector modules are shown with small numbers.

3 Basic principles

The PNCCD camera system uses a fully depleted PNCCD where incident photons create charges [**?**, **?**]. These charges are shifted to the border of the PNCCD where the charges are processed by ASICs [**?**, **?**]. A schematic view of the PNCCD chip and the first amplifying stage by the CAMEX ASIC is shown in Fig. 8.

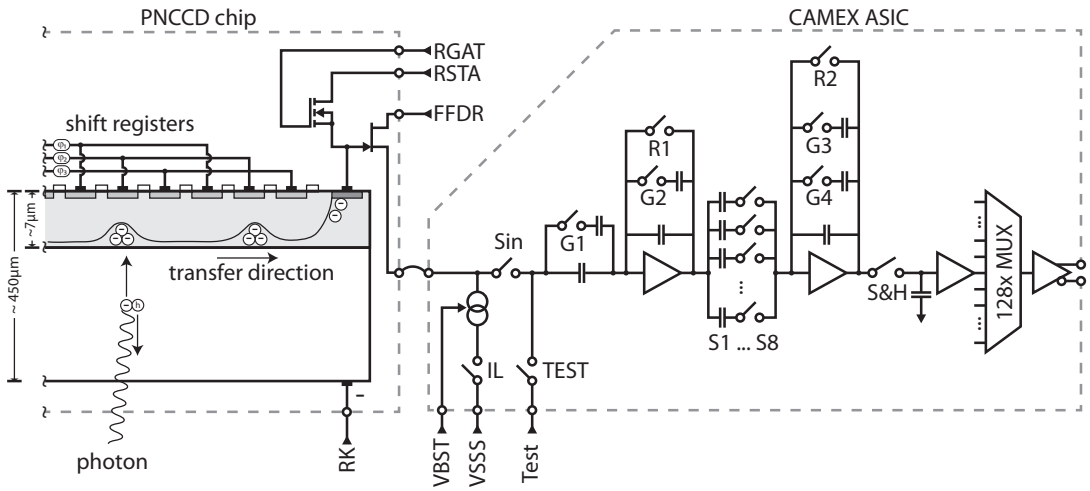


Figure 8: Schematic of the PNCCD chip and CAMEX ASIC. Only one channel of the PNCCD and the CAMEX is shown. A reverse voltage RK depletes the silicon, photon-generated charges are transported by variable voltages on the shift registers φ_i to the readout anode. The CAMEX uses correlated double sampling with different gain options (G1 to G4). Each of the 128 separate channels of one CMX is being multiplexed to a differential output driver.

The PNCCD chip is fully depleted by applying a high reverse voltage[1]. An X-Ray photon enters the silicon through the backside located entrance window and generates a wavelength/energy dependent number of electron-hole pairs inside the $450\,\mu$m thick depleted bulk. The electrons move to the front side where they get temporarily stored in a subpixel potential well. Cyclic rotating voltages on the shift registers change these potential wells such that the photon-generated electrons are shifted successively towards the read out anode and the gate of the on-chip readout FETs, also called First FET (FF). The on-chip reset structure is located on the PNCCD chip as well. The reset anode potential is "RSTA" and the reset gate is controlled by "RGAT". Further details for the PNCCD can be found in [**?**]. The First FET Drain (FFDR) from the PNCCD is directly wire bonded to the input stage of the CAMEX.

The CAMEX (CMOS Multichannel Analog MultiplEXer) is a custom ASIC made by Frauenhofer Institute for Microelectronic Circuits and Systems and the Max Planck Institute for Physics and Astrophysics. One CAMEX provides 128 parallel channels of correlated double sampling (CDS) for low-noise charge sampling with programmable gains and multiplexing capabilities [**?**].

Depending on the photon-induced charges on the read out anode the FF gate modulates the current between "FFDR" (First FET DRain) and "VSSS". The internal current source in the CAMEX is enabled by the programmable switch "IL" and the current is controlled by a control voltage on "VBST". The gain of the charge sensitive amplifiers can be configured by modifying the capacitances with the programmable switches G1 to G4. CDS uses a baseline sample (before photon interactions) and a signal sample (after the photon interactions). The result is stored in sample and hold circuits until it is multiplexed to an analog output.

[1] about 200 V, named "RK" for German Rück-Kontakt (backside contact)

4 Electronic Setup

Each detector plane consists of two PNCCD detector modules. The detector modules are in vacuum and are connected via flex leads to a feedthrough flange with separate air-side data boxes for each module. Each data box is connected via cables (REDEL for power, round LEMO for analog signals and SCSI for digital timing) to the control rack. One control rack is needed for one detector plane consisting of two PNCCD detector modules.

The control rack holds power supplies for the PNCCD modules, a sequencer for timing, ADCs for the analog CCD signal readout and devices for housekeeping. Every crucial component is backed up by a UPS capable of supplying power for about 10 additional minutes in case of a power outage.

Most of the PNCCD detector module supply voltages are generated by the WIENER Mpod crate using ISEG medium and low voltage modules (EMQ F6x2-F and ELQ F6x1-F). Some supply channels for the PNCCD only need an electric potential. In this case the load is very high-impedance and there is essentially no current. As switched power supplies (as the ISEG) are usually designed to only regulate with an existing load the ISEG modules have been modified internally by the manufacturer to include additional resistors as load to enhance the regulating capabilities on external high-impedance loads.

The system performance is particularly sensitive to the stability of some voltages (FFDR). These are supplied by two separate power supplies, the Rohde & Schwarz NGPS 32 with the GPIB IDs 17 (top module FFDR) and 18 (bottom module FFDR).

Housekeeping is done by a Keithley 2700 (at GPIB ID 19) with two switcher cards: 7706 and 7700. It reads out 10 temperature sensors per plane and is also used for monitoring FFDR currents and enabling/disabling temperature sensors on CCD.

A CompactPCI crate holds the sequencer and the ADCs, both manufactured by FZ Jülich. Additionally there are current sources for the CCD temperature readout in the crate. A GPIB bridge by Agilent translates between Ethernet network and GPIB-devices (Keithley 2700 and Rohde & Schwarz NGPS32).

4.1 Internal connections in the control rack

This section describes the internal electric connections of the control rack. An overview for the rear side connections is shown in Fig. 9 and specified in Section 4.1.1. The front side connections are explained in Fig. 10 and Section 4.1.2.

4.1.1 Rear side control internal rack connections

The **Main power supply** has two separate rails with different voltages: 120 V / 60 Hz and 230 V / 50 Hz. The first chain is a 120 V / 60 Hz power distribution unit with NEMA-5 sockets for motor power supply, Lake Shore temperature controllers and IOC computers. The second rail has an **online double-conversion UPS** (Effekta ACX11MHR3K000MP1) to protect the delicate PNCCD from sudden power outage. It is connected to the PNCCD power supplies, sequencer and ADCs. The UPS has an input voltage range 160 V to 275 V and is powered by a 208 V / 60 Hz L6-30 power outlet. The UPS output voltage is 230 V / 50 Hz and is distributed inside the control rack with a PDU with IEC 60320/C13 sockets. BE SURE TO CONNECT ONLY COMPATIBLE DEVICES TO THE 220 V CHAIN. Keep in mind that every additional device on the 230 V chain will reduce bypass time of the UPS. The battery pack is connected with as special cable to the UPS (not shown in Fig.9).

The **Agilent GPIB bridge E5810A** is connected via an IEC C13/C14 cable to the 230 V PDU backed up by the UPS. Network communication is done by copper ethernet (not shown in Fig.9). The GPIB devices are being daisy chained from the Keithley 2700 to the bottom NGPS32 and finally to the top NGPS32.

The **Keithley 2700** is connected to the 230 V PDU via a IEC C13/C14 cable. The upper expansion card 7706 in slot 1 has a cable with a DSUB-9 connector leading to the back of the cPCI rack. This connection is for reading out the temperature on the PNCCD chip. The lower expansion card 7700 is placed in slot 2 and has a cable with a DSUB-25 connector to be placed in the AUX-Connector box just next to the Keithley. This connection is for reading out PT1000 temperature sensors on the detector module and the currents for the FFDR supplies.

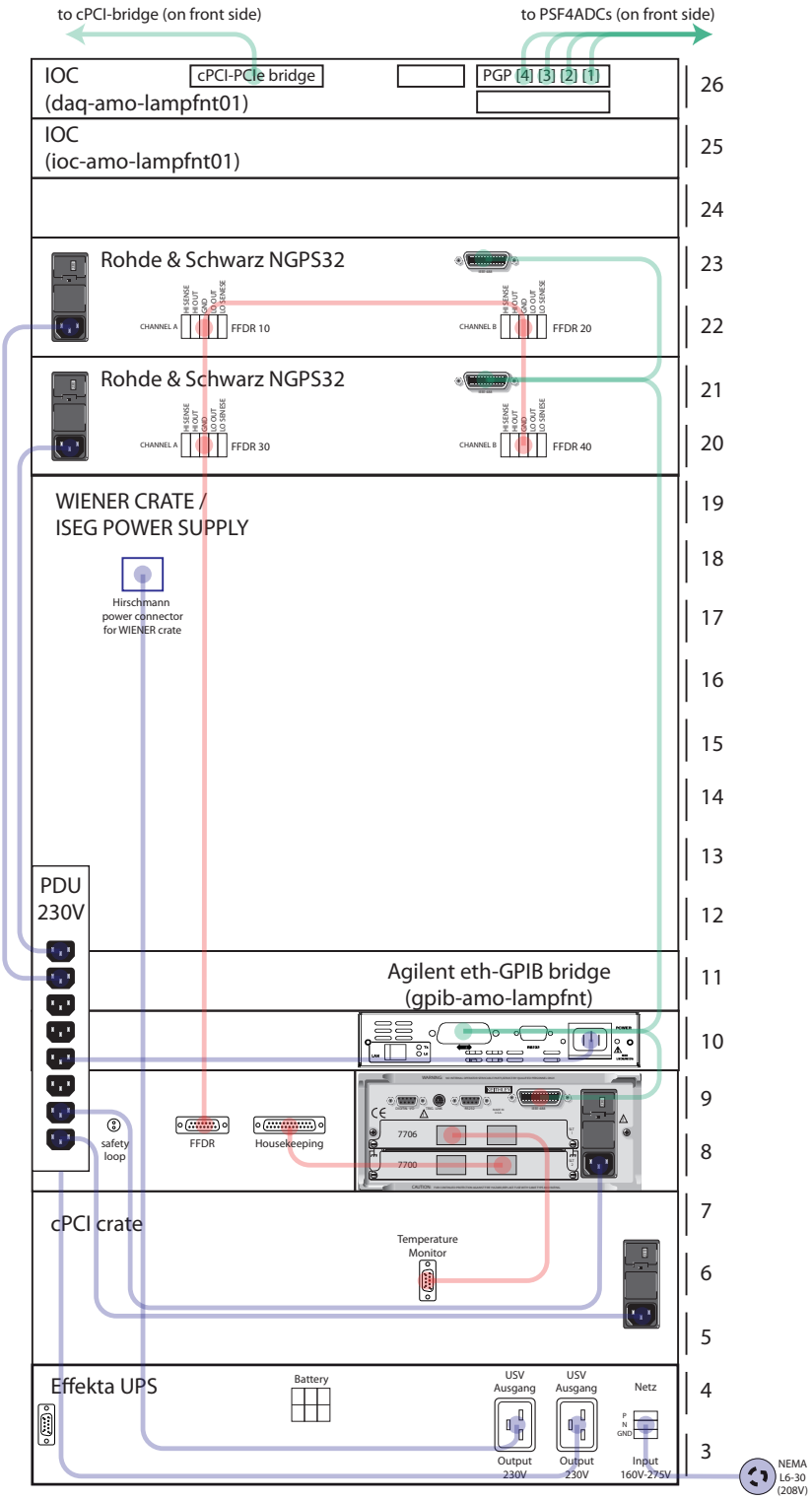


Figure 9: Internal Control Rack connections on rear side. The device positions is counted in rack units (starting bottom) and is shown on the right side. Power cables are shown in blue, GPIB cables in green and custom cables in red. Connection cable from UPS to battery is not shown.

The **WIENER crate** with the ISEG modules has a Hirschmann connector for power supply. A fitting cable with an IEC C19 plug goes directly to the Effekta UPS.

The two **Rohde & Schwarz NGPS32** power supplies generate a total of four voltages for the PNCCD. They are connected to the 230 V PDU with an IEC C13/C14 cable. Communication is done by GPIB cables connected to the Agilent GPIB bridge. Output voltages of the NGPS32 are provided on terminal blocks. They can be unplugged for better access after releasing the screws on the left and right end of the terminal block. Positive output is on `HI OUT`, negative output on `LO OUT`. The terminals are connected to a cable with a DSUB-15 connector leading to the AUX-Connector-Box next to the Keithley. The pin-layout is shown in Table 1. The top Rohde & Schwarz has the GPIB ID 17 and supplies `FFDR_10` and `FFDR_20`. The bottom has the GPIB ID 18 and supplies `FFDR_30` and `FFDR_40`.

rack pos.	NGPS32 terminal	AUX-Con-Box	description
22 (upper)	Ch. A, HI OUT	Pin 9	`10_FFDR+`
22 (upper)	Ch. A, LO OUT	Pin 1	`10_FFDR−`
22 (upper)	Ch. B, HI OUT	Pin 10	`20_FFDR+`
22 (upper)	Ch. B, LO OUT	Pin 2	`20_FFDR−`
20 (lower)	Ch. A, HI OUT	Pin 11	`30_FFDR+`
20 (lower)	Ch. A, LO OUT	Pin 3	`30_FFDR−`
20 (lower)	Ch. B, HI OUT	Pin 12	`40_FFDR+`
20 (lower)	Ch. B, LO OUT	Pin 4	`40_FFDR−`

Table 1: Connections between Rohde & Schwarz NGPS32 power supply terminal blocks and AUX connector box DSUB-15 socket.

4.1.2 Front side internal control rack connections

The front side of the control rack has some internal connection described in this section. The external connections to the mounted data box at the vacuum chamber is explained in section 4.2.

Figure 10: Internal Control Rack connections on front side. The device positions is counted in rack units (starting bottom) and is shown on the right side.

The **WIENER Mpod crate** is controlled by SNMP via copper ethernet. The RJ45 connector is labeled "Ethernet" and is located on the leftmost module (MpodC) in the crate. The IP is determined by DHCP. After the MpodC there are five ISEG modules (from left to right: EMQ F6x2-F, ELQ F6x1-F, EMQ F6x2-F, ELQ F6x1-F, ELQ F6x1-F) for top CCD, top CMX, bottom CCD, bottom CMX and AUX. To distinguish between front (F) and rear (R) detector plane and between top (T) and bottom (B) module, abbreviations, the letters in brackets, are being used, e.g. F-T for front-top. The ISEG module "AUX" is connected to the AUX-Con-Box socket "ISEG AUX IN" with a cable containing REDEL H51 plugs. Optional a Safety-Loop device can be installed in the WIENER crate to shut down its supply voltages immediately, which has to be connected to the corresponding socket on the AUX-Connector box.

In the **cPCI-crate** there are two **dual constant-current sources** for measuring the temperature on the PNCCD chip by the voltage-drop of a p-n-junction. The round LEMO 4-pin sockets of the dual current sources are connected to corresponding connectors of the AUX-Con-Box. The **cPCI-bridge** is connected via a cable with the PCIe-counterpart in *ioc-amo-lampfnt01 / ioc-det-pnccd02*. The four **ADC boards** labeled "PSF4AD" are each connected to the sequencer labeled "SEQ" with short Network-cables as indicated by the red letters in Fig. 12. The digitized output of each ADC is transmitted via four fibers-pairs (labeled PGP 1 to PGP 4) to one PGP card on the rear side of *daq-amo-lampfnt01 / daq-det-pnccd02*.

4.2 Cables between control rack and data box

Electrical connection between the control rack and the top and bottom data box is done by 6 m cables. A two-letter prefix determines the detector plane (“F” for front, “R” for rear) and the module (“T” for top, “B” for bottom).

The data box has five internal connections by round LEMO connectors (see Fig.11). Each connector has a different number of pins or notch-pattern. Same names have to be connected. The data box has several optional monitoring connectors. The mAP-ADC module on the data box provides optional analog detector output as single-ended signals on LEMO 00.250 sockets. Maximal output is ± 5 V, typical output several 100 mV. The signal should be terminated with 50 Ω at the oscilloscope. The mAP-SEQ module has an optional dedicated output “TRIG” to synchronize with an oscilloscope, output level is TTL. These optional signals are useful for monitoring or debugging but are not necessary for normal operation.

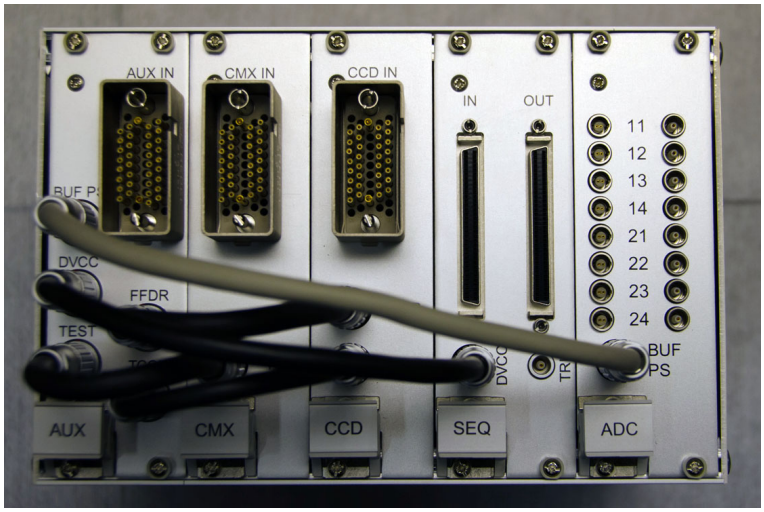


Figure 11: Data box with internal LEMO cable connections applied. From left to right: mAP-AUX, mAP-CMX, mAP-CCD, mAP-SEQ and mAP-ADC.

Power supply is done by three REDEL cables (“AUX”, “CMX” and “CCD” with a two-letter prefix for the location) connected to the correspondingly labeled sockets on the WIENER crate and on the data box. Make sure that every ISEG module is connected with the equally labeled data box module.

The sequencer “SEQ” in the cPCI-crate generates the timing for detector. Synchronizing SEQ with SLAC beamline “Readout”- and “Clear”-Triggers is done by four LEMO 00.250 connectors. The clear trigger should be connected to the top left LEMO and the readout trigger connected to the top right connector. Digital timing information is transmitted with a 68-pin U320-SCSI cable. The long 6 m-cable is connected from the sequencer “SEQ” in the control rack to the “IN” socket of the mAP-SEQ module in the bottom data box. From socket “OUT” the timing is daisy-chained to top data boxes socket “IN”. In the top data box the “OUT” connector stays unconnected and the internal termination must be enabled. The sequencer has four RJ45 connectors to sync the the four ADCs. ADCs from left to right are connected to the sequencer connections starting from bottom to top. There are two LEMO 00.302 connector with small splitter boards for making two LEMO 00.250 connectors.

The differential analog detector signal for one detector module (a half plane) is submitted by 8 cables labeled (location prefix and “11”, “12”, “13”, “14”, “21”, “22”, “23” or “24”). These cables are combined in a common metallic shielding for mechanic and electromagnetic protection. Connector orientation is coded with a notch. On the control rack side the cables have to be connected as shown in Tab. 2. On the detector side connect the eight cables “T-xx” to the correspondingly labeled sockets of the mAP-ADC module in the top data box, and the eight cables “B-xx” analogous in the bottom data box. This information is summarized in Tab. 3, which additionally lists the corresponding locations on the sensors.

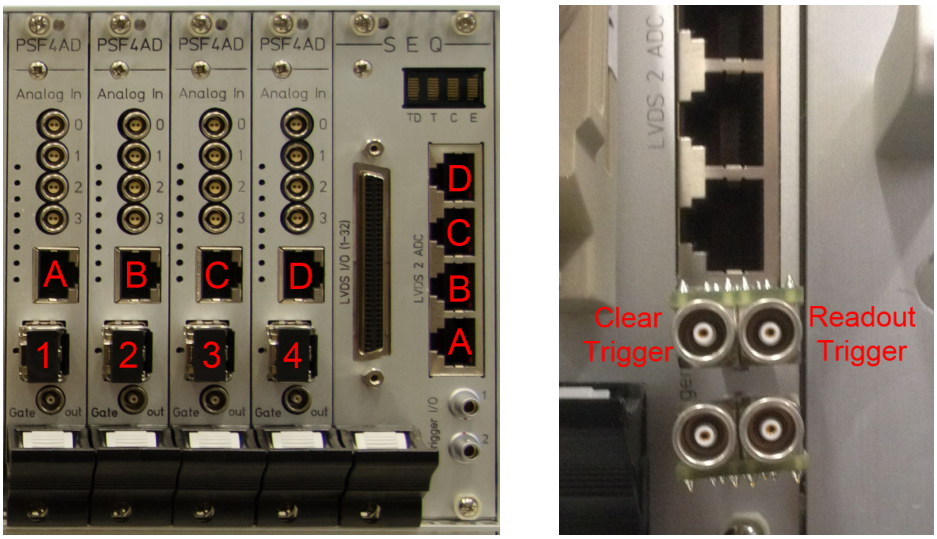


Figure 12: The four ADCs (labeled A, B, C and D) and sequencer on the right. RJ45 sockets with corresponding letters are connected with short patch cables to distribute timing between sequencer and ADCs. The fiber link sockets (labeled 1, 2, 3 and 4) are connected to the PGP card in daq-amo-lampfnt01 / daq-det-pnccd02. On the right picture the inputs for Clear- and Readout-Trigger are shown.

PSF4ADC "A"	PSF4ADC "B"	PSF4ADC "C"	PSF4ADC "D"
B-22 → 0-A	B-13 → 0-B	T-23 → 0-C	T-12 → 0-D
B-21 → 1-A	B-14 → 1-B	T-24 → 1-C	T-11 → 1-D
B-24 → 2-A	B-11 → 2-B	T-21 → 2-C	T-14 → 2-D
B-23 → 3-A	B-12 → 3-B	T-22 → 3-C	T-13 → 3-D

Table 2: Connection matrix for the ADCs and the analog output cables from the data box. The table has the same orientation and labels as the ADCs in Fig. 12. Left side of the arrow shows the cable name (with "T"=top and "B"=bottom) and right side of the arrow defines the ADC socket.

4.2.1 ADCs

There are four ADCs "PSF4AD" in each control rack named A to D from left to right (Fig. 12). Each ADC has four inputs for analog differential signals labeled from 0 to 3. The matrix of connecting the analog cables is shown in Tab. 2 (and Tab. 3).

Quadrant	ADC plug	cable	No. CMX	Quadrant	ADC plug	cable	No. CMX
10	2-D	T-14	14	20	2-C	T-21	21
10	3-D	T-13	13	20	3-C	T-22	22
10	0-D	T-12	12	20	0-C	T-23	23
10	1-D	T-11	11	20	1-C	T-24	24
40	2-A	B-24	44	30	2-B	B-11	31
40	3-A	B-23	43	30	3-B	B-12	32
40	0-A	B-22	42	30	0-B	B-13	33
40	1-A	B-21	41	30	1-B	B-14	34

Table 3: Matrix of CMXs, ADCs and their connecting cables. Here the CMXs are listed according to their physical location on the modules (see also Fig. 7)

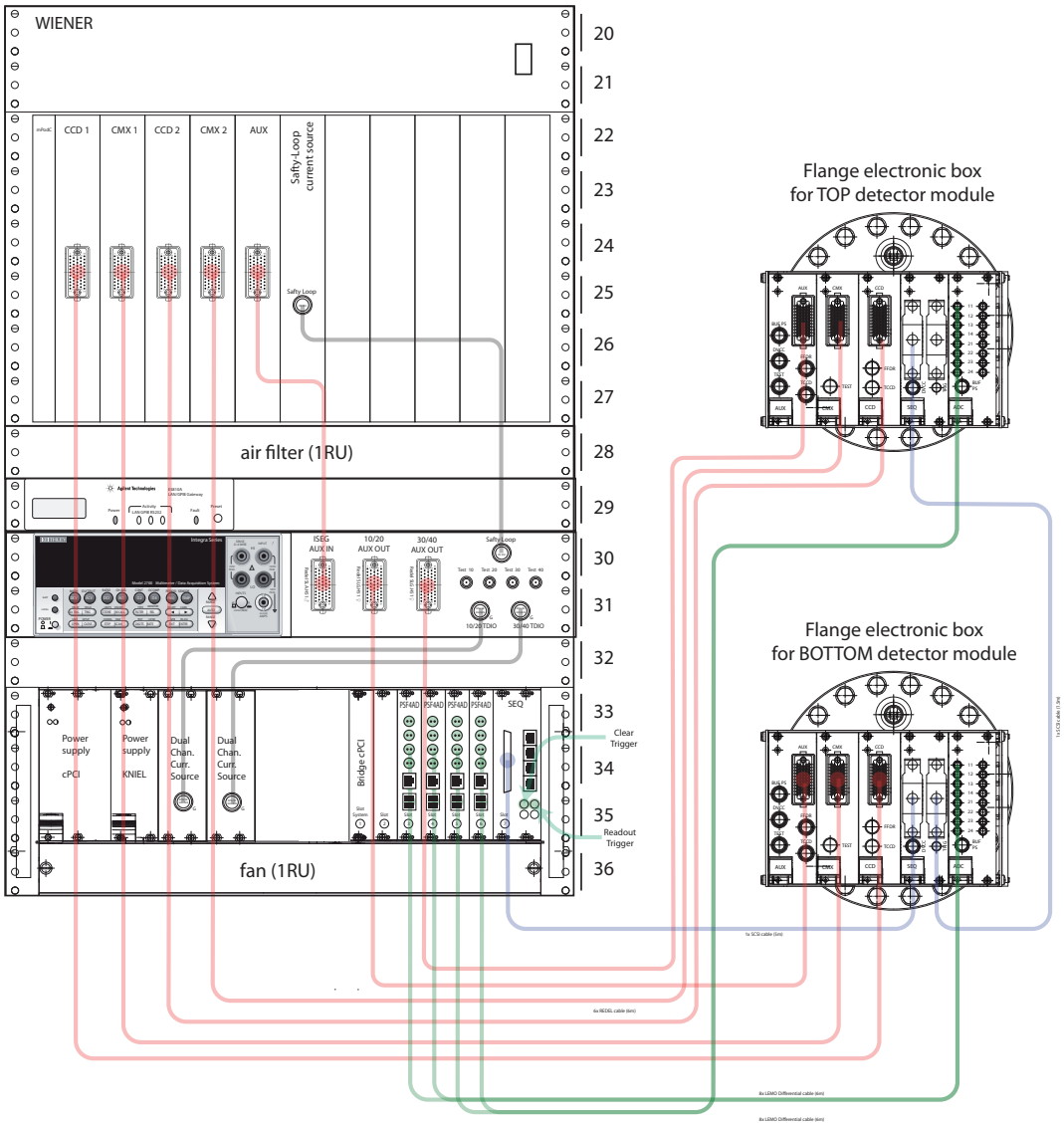


Figure 13: Schematic cable setup between control rack and data boxes at the feedthrough flanges.

4.3 Configuration of data box

The data box is directly connected to the vacuum feedthrough flange and contains five modules: mAP-SEQ for processing digital timing signals from the sequencer of the control rack. mAP-CCD and mAP-CMX are used as power distribution and filter. mAP-ADC contains buffers for the analog output signals. mAP-AUX is a signal distribution module. Configuration is only needed for mAP-SEQ and mAP-CCD. The name mAP originates from the German *"modulare Außen-Platine"* (modular outer PCB).

4.3.1 mAP-SEQ

The sequencer in the control rack provides timing for both the top and bottom detector module. As the modules are daisy chained the signal at the end of the chain has a small delay, which does get compensated by corresponding offsets in the sequencer timing. Additionally the end of the chain has to be terminated. Configuration is done by setting jumpers (see Fig. 14). The proper settings for the top module are listed in Table 4, the bottom module settings are shown in Table 5.

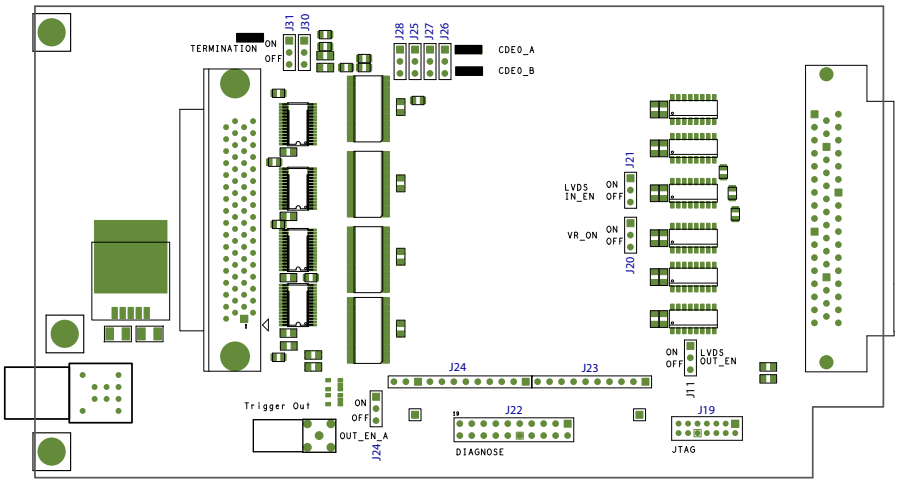


Figure 14: PCB of the mAP-SEQ module.

Jumper	description	"CDE0_A"	"CDE0_B"
J25	"CDE0"	-	set
J26	"CDE0"	-	set
J27	"CDE0"	-	set
J28	"CDE0"	-	set

Jumper	description	ON	OFF
J30	"TERMINATION"	set	-
J31	"TERMINATION"	set	-
J21	"LVDS IN_EN"	default	-
J20	"VR_ON"	default	-
J11	"LVDS_OUT_EN"	default	-
J24	"OUT_EN_A"	default	-

Table 4: Top PNCCD module Jumper settings of board “mAP:SEQ”, here configured to listen to sequencer data “B”. Since this board is at the end of the daisy chain the termination needs to be enabled.

Jumper	description	"CDE0_A"	"CDE0_B"
J25	"CDE0"	set	-
J26	"CDE0"	set	-
J27	"CDE0"	set	-
J28	"CDE0"	set	-

Jumper	description	ON	OFF
J30	"TERMINATION"	-	set
J31	"TERMINATION"	-	set
J21	"LVDS IN_EN"	default	-
J21	"VR_ON"	default	-
J11	"LVDS_OUT_EN"	default	-
J24	"OUT_EN_A"	default	-

Table 5: Bottom PNCCD module Jumper settings of board “mAP:SEQ”, here configured to listen to sequencer data “A”. Since this board is not at the end of the daisy chain the termination needs to be disabled.

Furthermore the mAP-SEQ has a port for diagnostics (J22, J23 and J24) for monitoring the digital timing signals with an oscilloscope, logic analyzer or mixed-signal-scope. The connector J22 is directly compatible with a mixed signal option MSO-250 or MSO-500 from LeCroy with the MSO-3M cable. Connector J19 is for flashing the Xilinx FPGA on the detector module using a standard Xilinx JTAG adapter like “Platform Cable USB II”.

Pin	MSO	description
20		VCC
19	D0	S_OUT
18	D1	RGAT
17	D2	PHI_1
16	D3	PHI_2
15	D4	PHI_3
14	D5	PHI_4
13	D6	PHI_5
12	D7	PHI_6
11	D8	MUX_OUT

Pin	MSO	description
10	D9	TG
9	D10	MUX_CLK
8	D11	MUX_IN
7	D12	S_MODE
6	D13	S_CLK
5	D14	S_IN
4	D15	Diag_Sel_3
3	D16	Diag_Sel_2
2	D17	Diag_Sel_1
1		GND

Table 6: Digital timing signals for diagnostics.

4.3.2 mAP-CCD

The mAP-CCD provides filters for the supply voltages for the CCD. Configuration is done by jumpers (see Fig. 15). The polarity of the reset anode on the CCD (RSTA) can be changed for both halves of the detector separately. Default setup is negative reset anode potential. The pn-junction for measuring the temperature directly on the CCD chip has a Guard-Ring (T_GRD), which can be set to GND potential (default) or to outer guard ring (OGR) potential. If unsure, leave configuration in default state.

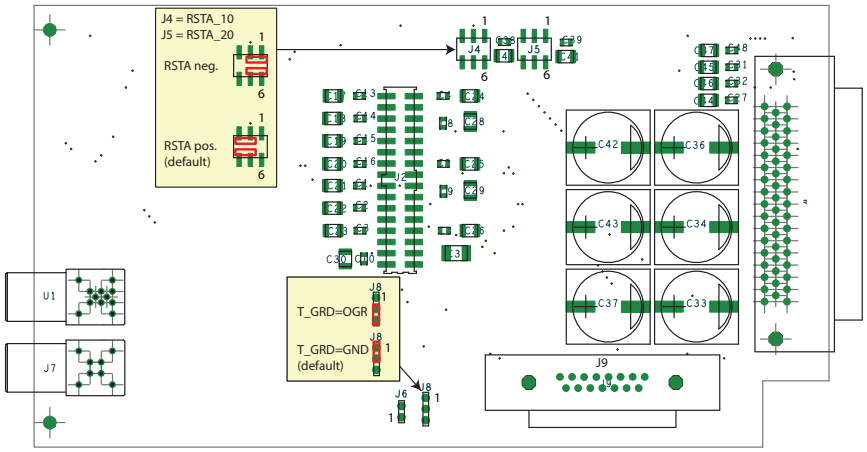


Figure 15: PCB of the mAP-CCD module.

For debugging the shift-register (PHI) and reset-gate (RGAT) potentials generated at the inner PCB of the detector module several monitoring lines (PHI_1_MON to PHI_6_MON and RGAT_MON) are lead through the mAP-CCD to connector J9. An internal 1 kΩ resistor is used to decouple the monitoring lines, therefore do not terminate the analog monitoring lines when connecting them to a scope.

Pin	description
1	CMX analog Ground
2	20_PHI_2_MON
3	20_PHI_3_MON
4	20_PHI_4_MON
5	20_PHI_6_MON
6	10_PHI_3_MON
7	10_RGAT_MON
8	10_PHI_4_MON

Pin	description
9	20_PHI_6_MON
10	20_RGAT_MON
11	20_PHI_5_MON
12	20_PHI_1_MON
13	10_PHI_5_MON
14	10_PHI_2_MON
15	10_PHI_1_MON

Table 7: Analog monitoring signals for shift-registers (PHI) and reset-gate. Do not terminate.

4.3.3 mAP-CMX

The module mAP-CMX is for filtering the CAMEX ASICs supply voltages. There is nothing to configure on this module.

4.3.4 mAP-ADC

The module mAP-ADC is for buffering the differential analog output signal from the CAMEX ASICs. It contains monitoring outputs for single-ended LEMO 00.250 connectors. 6 m cables are supplied for convenience, for viewing a channel on a scope the cable should be terminated with 50 Ω.

5 Software Initialization

Software initialization consists of two main areas: Main control and Timing/DAQ. Section 5.1 explains how to set up *Main control* which is used for temperature control, for turning PNCCDs on or off, and for changing the operating mode. Section 5.2 shows setting up timing sequencer and the data acquisition for the ADCs. This section assumes that the drivers and the control software have been installed. For questions regarding these please consult the corresponding readme files.

5.1 Main control

To start the *main control* window you have to be on one of the console computers (for example *amo-console*, *xcs-console*, *sxr-console*, ...) and be a member of the group *detopr*. In the directory `~detioc` you can start the main control window for the rear PNCCD by the command `./launchScreens.sh`. The usage of the main control window is explained in Section 6.

5.2 DAQ: Timing sequencer and ADCs

The sequencer and the ADCs have to be in sync, they need to get initialized once. For the initialization a (DAQ-)trigger for the sequencer is required. Login on the DAQ computers (`daq-amo-lampfnt01` or `daq-det-pnccd02`) as user `carron`. In directory `~carron/lamp` start `./2_startAdc.sh`. This spawns 4 ADC control windows (see Fig. 24 in Section 6.7). Then start `./2_startSeq.sh` to spawn the sequencer control window and load the standard timing `lamp_std`.

In the *ADC control* windows check the Control register. In the main menu press "R" for *Read Value* and then "V" for *Cntrl*. It should now show: `Last read: Cntrl Reg [ 0x00001400 ]`. If it shows `[ 0x00001000 ]`, the ADCs are not completely initialized, they are in state NOT-READY. In this state data will not yet be sent from ADCs to the DAQ. To complete the initialization process proceed as follows:

1. Stop run / DAQ and shut down
2. Remove PNCCDs from DAQ configuration
3. Shut down both PNCCD processes from the procserv monitor window (Ctrl+X)
4. Start DAQ without PNCCDs
5. For both front and rear PNCCDs:
   (a) Stop Sequencer (press "S" in sequencer control window)
   (b) For each of the 4 ADCs:
      i. Go to Options menu ("ESC" for main menu, then "O" for option menu)
      ii. Do Master Reset (press "M")
      iii. Do Reset Optics (press "R")
      iv. Do Clear Counter (press "K")
   (c) In Sequencer control window: (Re)start Sequencer (press "S")
   (d) For each of the 4 ADCs:
      i. Toggle Enable ADC2TLK (press "F", in enabled state it shows Disable ADC2TLK)
6. At DAQ control: Stop run
7. At procserc monitor window: Restart both PNCCD processes (Ctrl+R)
8. At DAQ control: Partition select -> include PNCCDs
9. At DAQ control: allocate and begin run (with record run disabled)
10. Check for damaged frames/data

It is essential that during step 5d the corresponding sequencer needs to be running continuously with a typical repetition rate. Therefore a repeating trigger is required. “Start DAQ without (the corresponding) PNCCD” is recommended (step 4) to supply this trigger. The DAQ of the corresponding PNCCD should not be taking data during this step, to avoid damaged data frames. After the completion of step 5d the sequencer and ADCs are in the state READY-RUNNING. You may temporarily stop the sequencer here, then sequencer/ADCs are in state READY-STOPPED.

6 Software Usage

6.1 Main control window

The main control window is used to open control windows for power supplies, cooling control and monitoring and general housekeeping data. Figure 16 shows the main control window for the rear PNCCD. The front PNCCD has a very similar control window. The main control window has four areas: *Power*, *Cooling*, *Monitoring* and *Scripts*.

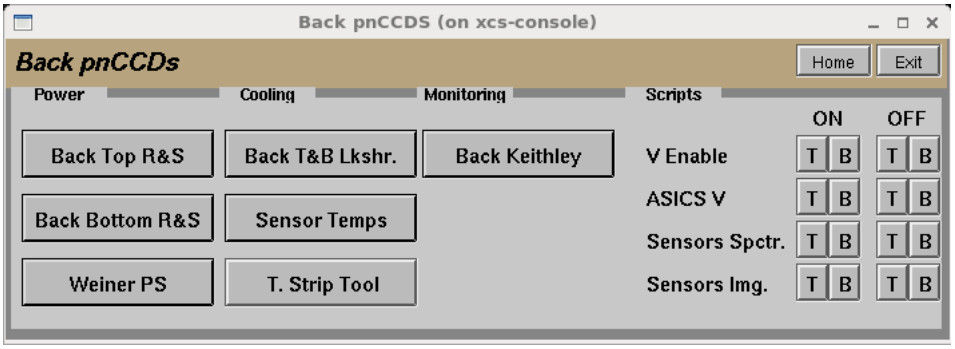


Figure 16: The main control window for rear PNCCDs.

The area *scripts* is used for turning the PNCCD on or off power supplies or change the mode of operation. Buttons labeled **T** control the top detector module and **B** is for the bottom detector module. After clicking on a button you are asked for the password to prevent accidental change of operating state. The order of the steps is described in Section 7 with Figure 25.

The area *Power* is for manual control and monitoring of the supply voltages. Most PNCCD supply voltages are provided by the WIENER power supply. Operation of the WIENER is described in Section 6.3. The FFDR voltage is supplied by the Rohde and Schwarz (Section 6.2).

In the area *Cooling* you can control the Lake Shore temperature controllers (see Section 6.4), monitor the temperatures on the detector module (see Section 6.5) and use the StripTool to visualize the temperature evolution over time.

6.2 Powersupply: Rohde and Schwarz

The FFDR voltage is generated by a single Rohde and Schwarz power supply for each detector module. The window (see Fig. 17) shows the state of the Channel in the button (Channel A on/off). Clicking on the button toggles the state (on/off). The applied voltage is shown next to the button. You can type a new

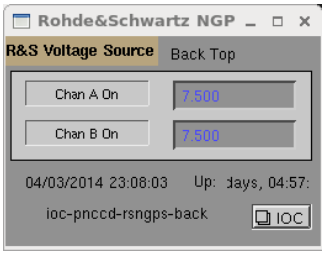


Figure 17: The control window for the Rohde and Schwarz power supply.

voltage and confirm with pressing ENTER. If possible check directly on the display of the R&S whether all voltages are correct and whether the right channels are enabled. This control window only shows the voltages. The currents for FFDR are shown with the Keithley (see Section 6.6).

6.3 Powersupply: Wiener

Most of the PNCCD supply voltages are generated by the WIENER power supply. The control window is shown in Fig. 18. 16 channels are shown at the same time. The button *OTHER MODULES* changes the set of displayed channels. ASICs voltages are on module 0 (top) and module 2 (bottom). CCD voltages are shown on module 1 (top) and module 3 (bottom). Auxiliary voltages are on module 4. The button *STATUS* shows additional status conditions for each channel.

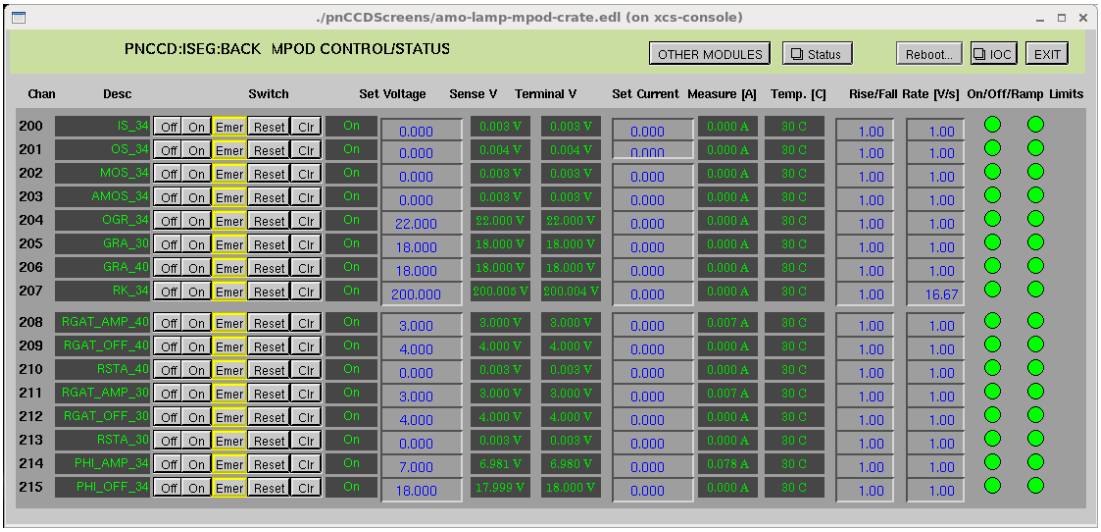


Figure 18: The control window for the Wiener power supply.

Every channel has the following sections: Channel number, channel description, button *Off* (disabling channel), button *On* (enabling channel), button *Emer* (for emergency off), button *Reset* and *Clr* (reset fault conditions), state of channel (on/off), *set voltage*, *sense voltage*, *terminal voltage*, *set current*, *Measure [A]* (measured current), *temperature*, rise/fall rate settings, indicators on on/off/rise state.

The *set voltage* accepts inputs to change the voltage which has to be confirmed by ENTER. It takes some time until the sense voltage reaches the set voltage.

6.4 Cooling: Lake Shore

The detector modules are cooled by a cooling finger. To keep them at a defined temperature heaters are attached near the detector modules. The heating power is controlled by the Lake Shore controller and depends on the temperature of the cooling line.

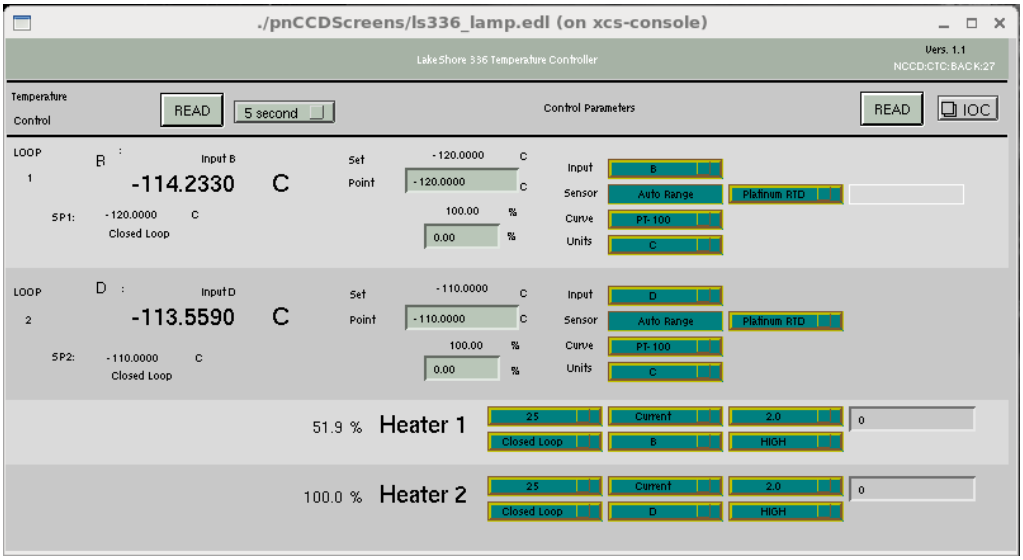


Figure 19: The control window for the Lake Shore Temperature controller.

The control window for the Lake Shore controller is shown in Fig. 19. The setpoint (target) temperature is set in the *Point* field and read back in the *Set* field. The actual measured temperature is shown below the label *Input* while the heating power in percent is displayed below the set point.

6.5 Cooling: Sensor Temperatures

The sensor temperatures window shows the four temperatures of every quadrant on the PNCCD chips (for most central numbers). Next to the PNCCD temperatures are buttons to enable the sensor. In rare cases the noise and offset performance can be improved by disabling the temperature diodes on the PNCCD by turning this buttons to *Off* state. If the temperature diodes are disabled the displayed temperatures are

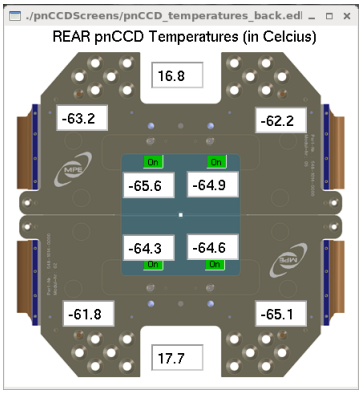


Figure 20: The monitor window for the Temperature sensors on the detector module.

bogus. There are additional temperature sensors on the four read out ceramics. The two values on top and

bottom are the temperature of the inner PCBs. As they are thermally isolated their temperature is much warmer than the cooled PNCCD chip or the read out ceramics.

6.6 Monitoring: Keithley

The Keithley monitors the currents of the FFDR supply (*FFDR10* to *FFDR40*). Additionally it monitors the voltage drop of the PNCCD temperature diodes (top four values, voltage drop is measured in Volt). At room temperature a voltage drop of about 330 mV is normal. A cooled system has a voltage drop of

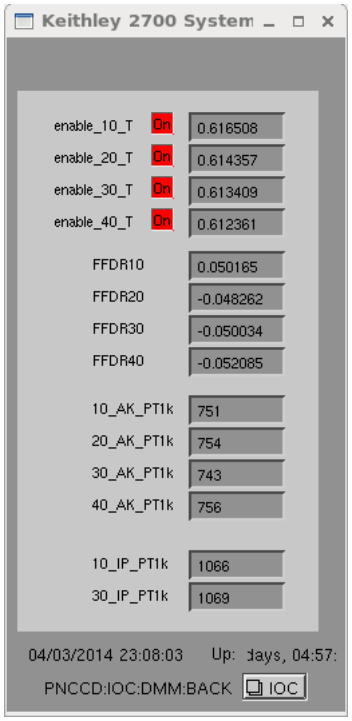


Figure 21: The control window for housekeeping data obtained by the Keithley.

about 550 mV or higher. Each temperature diode can be disabled individually (buttons *enable_10_T* to *enable_40_T*). If no module is connected or the temperature diode is disabled the measured voltage drop is 13.6 V. The calculated temperature is shown in the Sensor Temperatures window (Section 6.5).

The other temperature sensors are PT1000 with a base resistance of 1 kΩ at 0 °C. There are four sensors on the read out ceramics (*10_AK_PT1k* to *40_AK_PT1k*) and two on the inner PCBs (*10_IP_PT1k* and *30_IP_PT1k*).

6.7 Sequencer

The sequencer provides the timing for the PNCCDs. The schematic flow chart of the default timing is shown in Fig. 22.

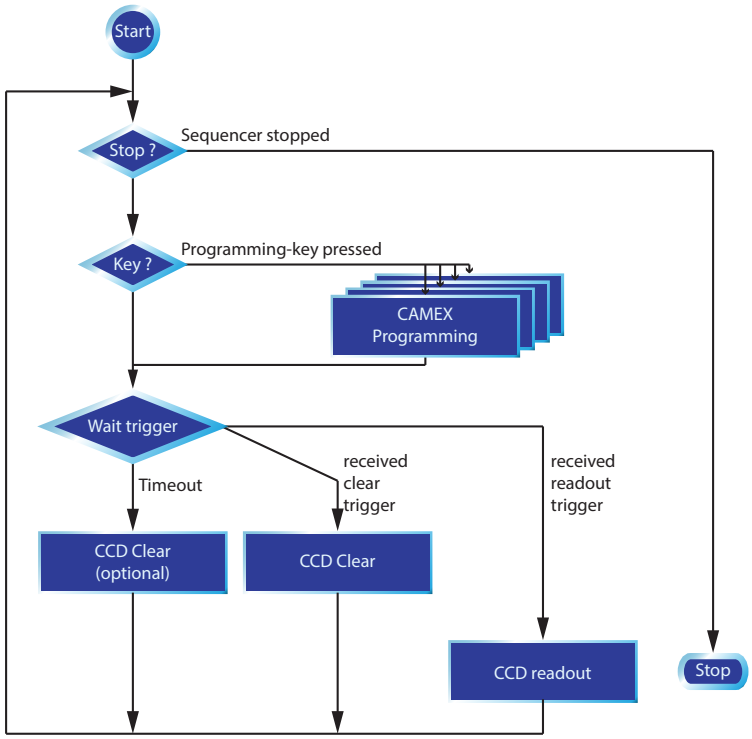


Figure 22: Simplified flow chart of sequencer default timing.

6.7.1 Starting and Stopping

The sequencer can be stopped and started within the sequencer menu. This is necessary if you would like to change a timing plugin. Before doing so it is recommended to stop the DAQ, too. After requesting a stop of the sequencer the sequence will continue until the end of the timing cycle (see Fig. 22). Therefore during readout the current frame will be completed. Only complete frames will be sent to the DAQ. It is not possible to interrupt a frame readout within the sequencer menu. To this respect the sequencer control is saver than ADC control. Do stop the sequencer before making changes on the ADCs (exception: ADC2TLK initialization). During CCD and/or CMX operation, sequencer stop time should be kept to a minimum. After changing the timing plugin select the options “open”, “load” and “start” to continue.

6.7.2 Programming the CAMEX

The sequencer can program the CAMEX. First programming is necessary within the step of powering up the ASICs (see Section 7.2). Reprogramming is possible while ASICs are powered up. It is recommended that the DAQ is not running, since the CAMEX mode (gain!) will be logged during DAQ start only. Programming is done with a single key stroke and is completed within a fraction of a second. The programming sequence starts immediately after the end of the frame readout and will take about $146\,\mu s$. Depending on the timing and the trigger setup one complete frame may get omitted. All four sequencer counters do get increased by one. Depending on the type of timing the programming has to be done once or twice. Possible programming options are listed in Tab. 8.

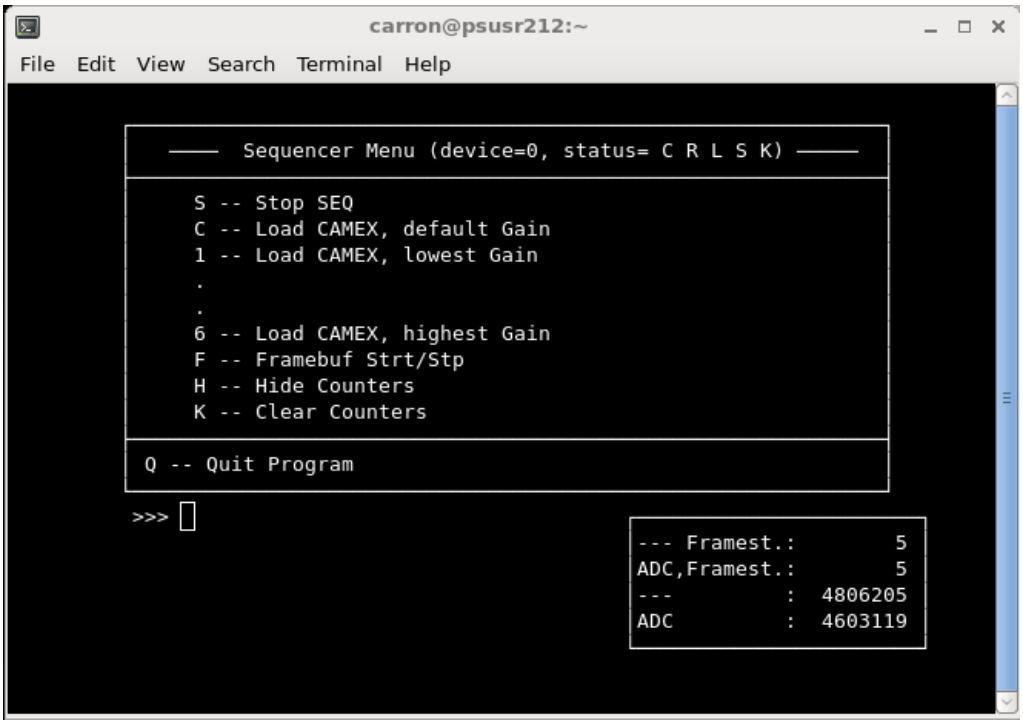


Figure 23: The control window for the timing sequencer.

The PNCCD has a charge handling capacity of $3 \times 10^5\,\mathrm{e}^-$ per pixel in imaging mode. This is about 1100 photons at 1 keV or 140 photons at 8 keV per pixel. For this number of photons no damage to the sensors occurs [**?**]. Exceeding this numbers may result in distorted images due to overflow from one pixel to the next one. Charges start to spread within one row over several channels. At even higher charge rates the distortion also influences several rows. The minimum irradiation level which leads to permanent damage has not been experimentally determined yet. For example high intensity Bragg diffraction peaks from "ice events" may lead to hot pixels which show higher signal offset and higher noise values. Such hot pixels may partially or fully recover within days.

key	relative gain	approx. ADU/keV	max. photons (1 keV) per pixel	Camex Magic	comment
1	1/256	5	1100	0x5ff	lowest gain
2	1/128	10	640	0x5bf	
3	1/64	20	320	0x4ff	
4	1/16	79	80	0x7ff	
5	1/4	316	20	0x6ff	
6	1	1250	5	0x63f	highest gain

Table 8: Sequencer options for programming the CAMEX in various gain settings. When using a non-standard sequencer timing file the options “1” to “6” may correspond to another set of gain values.

6.8 ADCs

Figure 24: The control window for one ADC.

The source code for the ADCs is located in the directory `~carron/lamp/HRL`. Until now no additional documentation is available for the ADCs.

7 Usage

To use the PNCCDs the electronic setup (see Section 4) and the software initialization (see Section 5) have to be completed. A slightly simplified overview of the operating states of the PNCCD camera system is shown in Fig. 25.

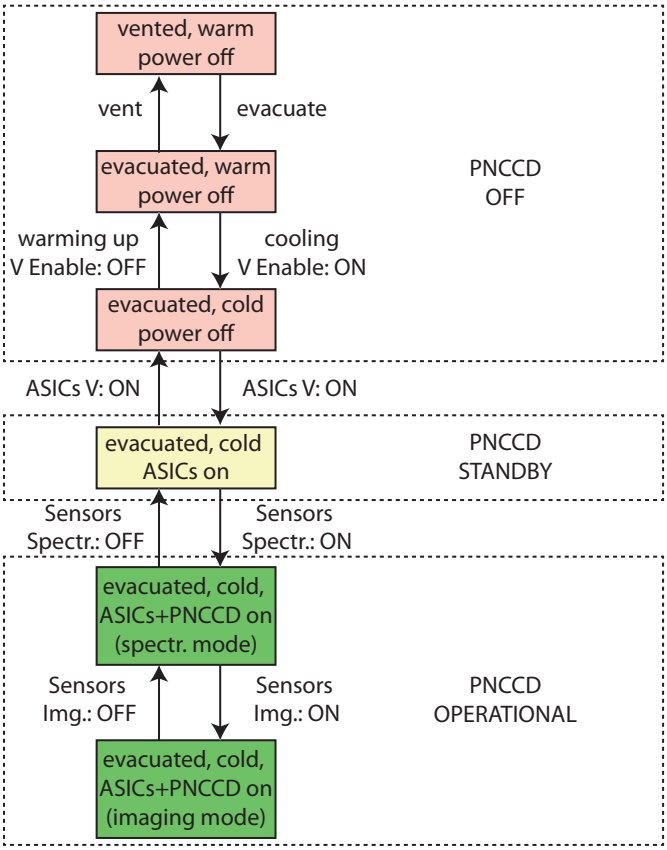


Figure 25: Overview of the states for the PNCCD camera system.

7.1 State: PNCCD OFF

The first step is pumping down until the pressure is sufficiently low ($p < 1 \times 10^5$ mbar), so that condensation ice will not form on cold sensor surfaces. Before the PNCCDs can be operated they need to be cooled down. Starting at room temperature, cooling down takes about 3 hours to reach final operating temperatures of the PNCCDs. Cooling is controlled by the Lake Shore control window (see Section 6.4) and can be monitored at the cooling sensor window (see Section 6.5). Temperature change on the readout ceramics and PNCCDs must not exceed $1\,^{\circ}\mathrm{C\,min}^{-1}$. Adjust the set points on the Lake Shore Temperature controllers accordingly.

7.2 State: STANDBY

When the PNCCD chip reaches a temperature of about $-40\,^{\circ}\mathrm{C}$ the CAMEX ASICs can be turned on. This can be done in the main control window with the button “ASICS V ON” for “T” (top) and “B” (bottom). A password will be asked to prevent accidental change of state. Within the ASIC power up script there will be a message to program the CAMEX ASICs. When the script tells you to do so (`program CMX now!`)

go to the sequencer control window (see Section 6.7). Start the programming of the CAMEX by pressing the key corresponding to the wanted gain ("1" to "6") without "Enter". The programming will start immediately and is completed within a fraction of a second. After programming the CAMEX continue with the script. When the CAMEX script is finished and the sequencer runs the currents should be checked again. Typical currents for are shown in Tab. 9.

The programming of the ASICs is done by the sequencer control window (see Section 6.7). As the ASICs produce about 12 W of heating per focal plane (two detector modules) the temperature curve will have a dip when turning them on. Now the PNCCD is in the STANDBY state. The ASICs are turned on, but all CCD related voltages are still turned off. Typical currents

name	description	standby	typical	maximum
VSS	neg. analog supply	250 mA	360 mA	450 mA
VDD	pos. analog supply	300 mA	430 mA	500 mA
VSST	neg. driver supply	25 mA	60 mA	150 mA
VDDT	pos. driver supply	25 mA	60 mA	150 mA
VSSD	neg. digital supply	5 mA	14 mA	50 mA
VDDD	pos. digital supply	5 mA	17 mA	50 mA
VBST	current source control	0 mA	0 mA	2 mA
VREF	reference for Op-Amps	0 mA	0 mA	2 mA

Table 9: Typical and maximal currents for CAMEX ASICs in typical operation.

7.3 State: PNCCD OPERATIONAL

To get the PNCCDs into the fully operational state the CCD sensor voltages have to be turned on. This is archived in the main control window by pressing "Sensors Spctr. ON" and "T" and "B". Again password protected scripts do the power cycle steps, ending up in a fully operational sensor mode optimized for spectroscopy use. In this spectroscopy mode a minimal spectral line width is archived. A check of the ASIC and PNCCD currents is advised (see Tab. 9 and 10). The gain can be changed in the sequencer control window. For more information on changing the gain settings see Section 6.7.2. It is not recommended to run the PNCCD with enabled sensor unattended for an extended time.

name	description	typical	maximum
IS	inner substrate	0 mA	0 mA
OS	outer substrate	0 mA	0 mA
MOS	MOS register	0 mA	0 mA
AMOS	MOS register at anode	0 mA	0 mA
OGR	outer guard ring	0 mA	0 mA
GRA	guard ring anode	0 mA	0 mA
RK	back contact	0 mA	0 mA
RGAT_AMP	reset gate amplitude	7 mA	15 mA
RGAT_OFF	reset gate offset	0 mA	0 mA
RSTA	reset anode	0 mA	0 mA
PHI_AMP	shift register amplitude	80 mA	300 mA
PHI_OFF	shift register offset	0 mA	0 mA
FFDR	first FET Drain	50 mA	80 mA

Table 10: Typical and maximal currents for CCDs in typical operation.

Apart from the spectroscopic mode the PNCCDs also do have an imaging mode with decreased spectral resolution but with larger charge handling capabilities. When the PNCCD is in spectroscopy mode you can

select “Sensor Img. ON” and press “T” and “B” to start the script changing the voltage settings on the PNCCD. You can not go directly from PNCCD standby mode (only ASICs on) to imaging mode.

The operation temperature of the PNCCD is around $-55\,^{\circ}$C. Thermal load generated by the detector modules depends on the operation mode (standby, spectroscopy or imaging) and on the repetition rate of the read-out and clear triggers.

	set point	PNCCD
PNCCD Front Top	$-120\,^{\circ}$C	$-56\,^{\circ}$C
PNCCD Front Bottom	$-115\,^{\circ}$C	$-56\,^{\circ}$C
PNCCD Rear Top	$-105\,^{\circ}$C	$-54\,^{\circ}$C
PNCCD Rear Bottom	$-85\,^{\circ}$C	$-54\,^{\circ}$C

Table 11: Typical operation temperatures and set points.

7.4 Shutdown procedure

To shut down the PNCCD proceed through the steps in reverse order. Starting from imaging mode, return to spectroscopic mode first by pressing in “Sensors Img. OFF” the buttons “T” and “B”. Adjust the setpoint temperatures either for standby mode or for heating up. Then turn off PNCCD voltages by pressing in “Sensors Spectr. OFF” the buttons “T” and “B”. You have now reached the STANDBY state, with only the ASICs turned on. It offers faster return to operational modes.

To power off the PNCCD the ASICs have to be turned off by “ASICS V OFF” and button “T” and “B”. Without thermal load the modules will quickly cool down. Adjust setpoint of the Lake Shore accordingly. A complete warm up from operational mode to room temperature takes about 3 hours.

Before venting with dry nitrogen make sure the detector module is at room temperature. Even when venting at $10\,^{\circ}$C, chances are that contaminants adhere to the coldest surface which might be the sensor chip on the PNCCDs.

The module can be stored in vacuum for an extended time either at room temperature or at constant temperatures ($-40\,^{\circ}$C to $+30\,^{\circ}$C).

7.5 PNCCD Data processing

The raw data of the PNCCDs have to be post processed. This includes dark frame offset substraction, common mode correction and event recombination [**?**, **?**].

7.6 Troubleshooting

Symptom: A set voltage is set to several volts but the sense voltage stays at 0 V. Although the set voltage has been received by the WIENER crate, ramping up of the channel voltage does not start.

Solution: Manually enter a slightly lower value (e.g. 0.1 V lower) in the set voltage. Wait for 3 seconds. Then enter the original set voltage. Ramping up should begin within 10 seconds.

Symptom: Set voltage can not be reached. For example: Set voltage is 0 V but the sense voltage does not decrease below 0.15 V.

Reason: Some voltages are coupled in the ASICs. It is possible that a different voltage channel which is still turned on prevents the desired channel to reach the set voltage. Then the stalled channel is pulled up by the other channel.

Solution: If unsure ask for help. Look for a voltage which is coupled to the pulled-up channel. Most likely it is a supply voltage in the same logical group. For example a CAMEX supply voltage like VSS or VSSD is not ramping down because it is coupled to VSS, VSST, VSSD or VBST. Slowly reduce remaining voltages by 0.1 V and look for a change in the sense voltage of the pulled-up channel. When a correlation is found, decrease the channel further until the script continues.

Symptom: Current on VSST or VDDT is 100 mA instead of usual 50 mA.

Reason: Output drivers for the analog signal is either on positive or negative limit. Can be due to missing trigger or stopped sequencer.

Solution: Check if sequencer is running and trigger is working. If this does not solve the problem, reprogram the CAMEX.

Symptom: Currents are much higher then usual. Data received from PNCCD is abnormal although there should be no photons hitting the detector.

Solution: Shut down CCD voltages and after that the CMX voltages. Then power up CMX and CCD again.

8 Timing

The LAMP PNCCD camera has a design readout rate of 120 Hz which means one full frame has to be transmitted in 8.33 ms. The full detector plane of 1024 by 1024 pixels is transmitted on 16 channels (11 to 24 and 31 to 44, see Fig. 7). On one channel 128 pixel per row and 512 rows are transmitted. The pixel `MUX_CLK` is 10 MHz, therefore 128 pixels take 12.8 µs. With a gap between two rows of approx 1.5 µs a total transfer of the frame data takes 7.3 ms. This leaves about 1 ms for shifting charges from one row to the next, exposure time and the frame-wise reset (563 µs).

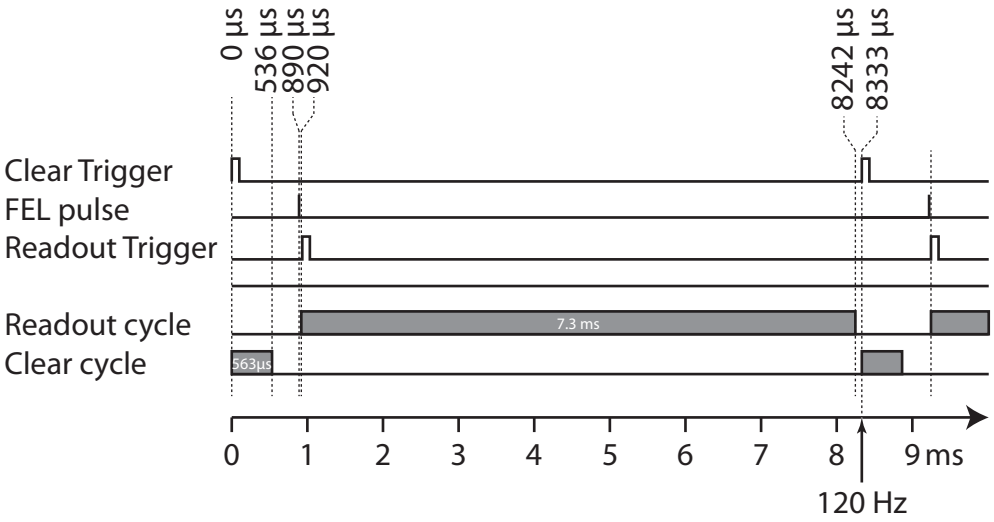


Figure 26: Typical Timing for 120 Hz frame rate without row-wise reset. Clear Trigger and Readout Trigger have a width of 10 µs to 100 µs.

The clear trigger and the readout trigger are supplied by EVR. The clear trigger starts the frame wise clear cycle. The FEL has to be between the end of the frame clear and the readout trigger. The readout trigger starts the following processes: Charge shifting to next row, reading out 128 pixels per row, row-wise reset (optional) and reading out 512 rows. In Figure 27 one complete frame is shown with highlighted regions for the frame-wise reset and the full frame readout cycle.

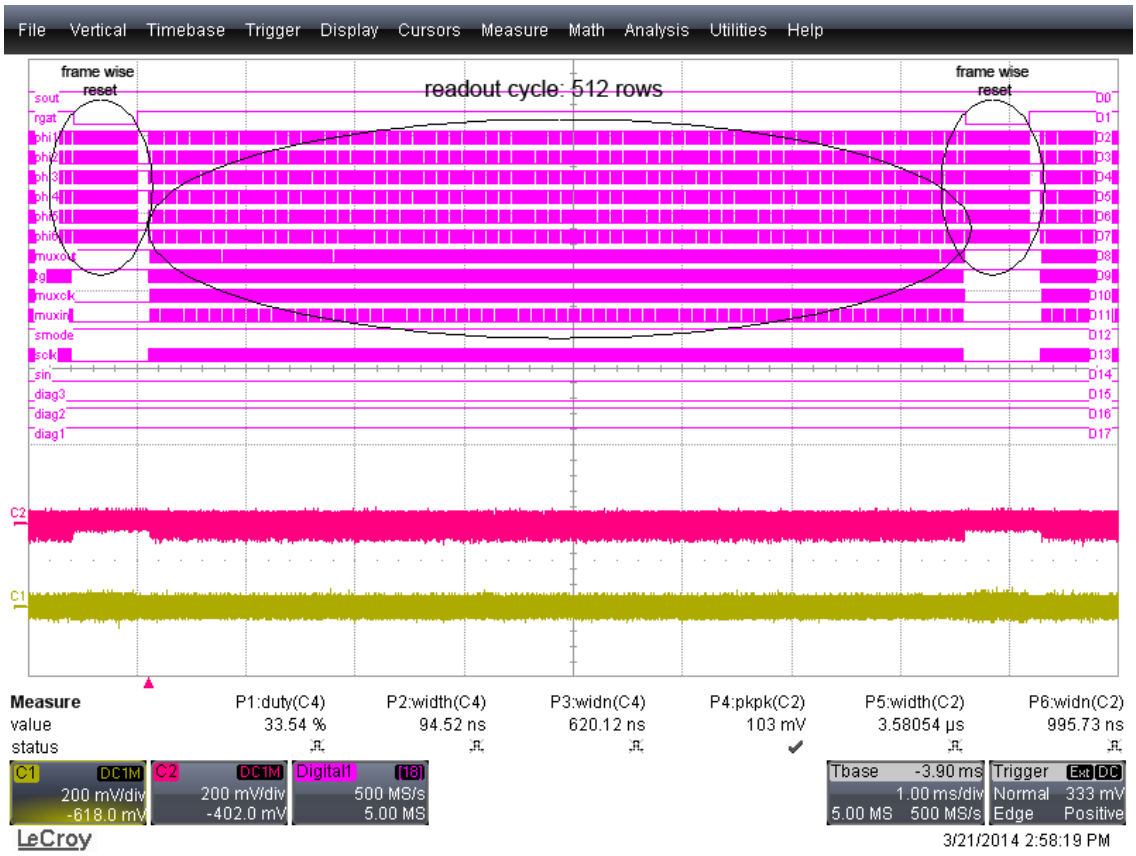


Figure 27: Oscilloscope screenshot for a 120 Hz timing. The full frame is visualized. Analog Signal C1 is the test pulse input (no testpulses are activated here) and C2 is the analog output of one CAMEX.

Figure 28 shows three rows inside the frame. A testpulse of about 100 mV is injected. When using testpulses make sure that the timing is compatible with test pulses (usually the .seq and .inc file names contain "TP" in their names). The test pulse has to be aligned in time to have a maximal signal in the analog output of the CAMEX. There are two different types of CAMEX used which differ in the test signal routing. Type PJD type is used in detector module 02 and 05 and features three bits (0x1c00) on CamexMagic to select every third channel to be connected to the test input. The Type OJD is used at detector modules 01, 06, 07 and 08 and features a 128 bit maxtrix which selects every channel individually (but all three bits 0x1c00 of CamexMagic have to be set). Therefore test pulse timings for OJD and PJD differ in the implementation of the test pulse settings.

Detector	position	CMX type
Module 02	FB	PJD
Module 05	FT	PJD
Module 06	RT	OJD
Module 07	RB	OJD
Module 01	spare	OJD
Module 08	spare	OJD

Table 12: Summary of the used CAMEX types and their location in the experiment.

The MUX_IN signal starts the multiplexing of the pixel data (MUX_OUT goes low) in respect to the clock signal MUX_CLK which is usually 5 MHz. But since both, rising and falling edges are used, every 100 ns a new data point is being multiplexed. When the multiplexing of the current row has finished, the signal MUX_OUT goes to high. While (pre-)processing the signal from the second row internally in the CAMEX with correlated double sampling, the processed signals from the first row are being multiplexed to the output of the CAMEX. These signals stay stored in the sample-and-hold buffers until the multiplexing for the first row has been finished. For this reason the first readout block in a frame has no MUX_CLK. Additionally the shift registers (PHI_1 to PHI_6) are used to shift charges on the PNCCD one row towards the readout nodes. In Figure 26 the row-wise reset has been activated which adds a 500 ns pulse send to the reset gate (RGAT) after processing a row.

For diagnostic purposes the three lines DIAG_1 to DIAG_3 select diagnostic outputs of one of the 8 CAMEXes on one module. This affects the CAMEX outputs MUX_OUT, TG (checksum output) and S_OUT (programming data output). The last is only relevant when the CAMEX is programmed (e. g. to a new gain) while S_MODE is set to low level.

Figure 28: Oscilloscope screenshot taken during the readout of three CCD rows. An injected testpulse (channel C1) is monitored on the analog CAMEX output (channel C2). No row-wise reset is used.

Figure 29: Oscilloscope screenshot taken during readout of one row with testpulses and with row-wise reset.

The timing is contained in two files: `lamp_std.seq` and `lamp_std.inc` located at the directory `~carron/lamp/SEQ-New/projects/LAMP`. The `.seq` should not be edited as `.inc` sets all the parameter values. Do not change the original `lamp_std.*` but use them as template to create new `.inc` and `.seq`. A timing has to be compiled with `./seqcc pathto/lamp_new.seq` in the directory `~carron/lamp/SEQ-New/bin`.

9 Appendix

9.1 EPICS PV

PV name	Pos.	unit	description
AMO:LMP:DMM:08:FR:10_T	FT	V	diode on CCD
AMO:LMP:DMM:08:FR:20_T	FT	V	diode on CCD
AMO:LMP:DMM:08:FR:30_T	FB	V	diode on CCD
AMO:LMP:DMM:08:FR:40_T	FB	V	diode on CCD
AMO:LMP:DMM:08:FR:10_AK_PT1k	FT	Ω	PT1000 on readout ceramic
AMO:LMP:DMM:08:FR:20_AK_PT1k	FT	Ω	PT1000 on readout ceramic
AMO:LMP:DMM:08:FR:30_AK_PT1k	FB	Ω	PT1000 on readout ceramic
AMO:LMP:DMM:08:FR:40_AK_PT1k	FB	Ω	PT1000 on readout ceramic
AMO:LMP:DMM:08:FR:10_IP_PT1k	FT	Ω	PT1000 on PCB
AMO:LMP:DMM:08:FR:30_IP_PT1k	FB	Ω	PT1000 on PCB

Table 13: Temperatures readouts on the PNCCD, the readout ceramics and the in-vacuum PCB. PV names are for the front detector plane. For rear detector plane exchange :FR: with :BK: in PV name.

PV name	Pos.	unit	description
AMO:LMP:DMM:08:FR:enable_10_T	FB	bool	Enable 30_T
AMO:LMP:DMM:08:FR:enable_20_T	FB	bool	Enable 40_T
AMO:LMP:DMM:08:FR:enable_30_T	FB	bool	Enable 10_T
AMO:LMP:DMM:08:FR:enable_40_T	FB	bool	Enable 20_T
AMO:LMP:DMM:08:FR:swap_polarity	FB	bool	invert diodes polarity

Table 14: Switches to enable/disable PNCCD internal temperature diodes. In LAMP the default mode is to set invert polarity to TRUE.

The swap_polarity variable defines the polarity for the pn-junction measuring the temperature. The default value is 1. If the polarity is wrong or the channel is not enabled (enable_?0_T) or the module is not connected the readout will be 13.6 V.

9.2 PNCCD voltages

PV name	Pos.	Ch.	description
AMO:LAMP:ISEG:FRONT:IS_12	10+20	001	inner substrate
AMO:LAMP:ISEG:FRONT:IS_34	30+40	201	inner substrate
AMO:LAMP:ISEG:FRONT:OS_12	10+20	002	outer substrate
AMO:LAMP:ISEG:FRONT:OS_34	30+40	202	outer substrate
AMO:LAMP:ISEG:FRONT:MOS_12	10+20	003	shift register separation potential
AMO:LAMP:ISEG:FRONT:MOS_34	30+40	203	shift register separation potential
AMO:LAMP:ISEG:FRONT:AMOS_12	10+20	004	shift reg. sep. pot. near readout
AMO:LAMP:ISEG:FRONT:AMOS_34	30+40	204	shift reg. sep. pot. near readout
AMO:LAMP:ISEG:FRONT:OGR_12	10+20	005	outer guard ring
AMO:LAMP:ISEG:FRONT:OGR_34	30+40	205	outer guard ring
AMO:LAMP:ISEG:FRONT:GRA_10	10	006	guard ring anode
AMO:LAMP:ISEG:FRONT:GRA_20	20	206	guard ring anode
AMO:LAMP:ISEG:FRONT:GRA_30	30	007	guard ring anode
AMO:LAMP:ISEG:FRONT:GRA_40	40	207	guard ring anode
AMO:LAMP:ISEG:FRONT:RK_12	10+20	008	back contact HV
AMO:LAMP:ISEG:FRONT:RK_34	30+40	208	back contact HV
AMO:LAMP:ISEG:FRONT:PHI_AMP_12	10+20	015	shift register phi amplitude
AMO:LAMP:ISEG:FRONT:PHI_AMP_34	30+40	215	shift register phi amplitude
AMO:LAMP:ISEG:FRONT:PHI_OFF_12	10+20	016	shift register phi offset
AMO:LAMP:ISEG:FRONT:PHI_OFF_34	30+40	216	shift register phi offset
AMO:LAMP:ISEG:FRONT:RGAT_AMP_10	10	012	reset gate amplitude
AMO:LAMP:ISEG:FRONT:RGAT_AMP_20	20	009	reset gate amplitude
AMO:LAMP:ISEG:FRONT:RGAT_AMP_30	30	212	reset gate amplitude
AMO:LAMP:ISEG:FRONT:RGAT_AMP_40	40	209	reset gate amplitude
AMO:LAMP:ISEG:FRONT:RGAT_OFF_10	10	013	reset gate offset
AMO:LAMP:ISEG:FRONT:RGAT_OFF_20	20	010	reset gate offset
AMO:LAMP:ISEG:FRONT:RGAT_OFF_30	30	213	reset gate offset
AMO:LAMP:ISEG:FRONT:RGAT_OFF_40	40	210	reset gate offset
AMO:LAMP:ISEG:FRONT:RSTA_10	10	014	reset anode potential
AMO:LAMP:ISEG:FRONT:RSTA_20	20	011	reset anode potential
AMO:LAMP:ISEG:FRONT:RSTA_30	30	214	reset anode potential
AMO:LAMP:ISEG:FRONT:RSTA_40	40	211	reset anode potential
AMO:LMP:PSL:22:VSetA	10	A	first FET Drain (FFDR10)
AMO:LMP:PSL:22:VSetB	20	B	first FET Drain (FFDR20)
AMO:LMP:PSL:20:VSetA	30	A	first FET Drain (FFDR30)
AMO:LMP:PSL:20:VSetB	40	B	first FET Drain (FFDR40)

Table 15: PNCCD supply voltages for front detector modules with corresponding channel numbers for the WIENER power supply. For rear detector modules exchange :FRONT: by :BACK: in the PV name.

PV name	Pos.	Ch.	description
AMO:LAMP:ISEG:FRONT:VSS_10	10	101	neg. analog supply
AMO:LAMP:ISEG:FRONT:VSS_20	20	116	neg. analog supply
AMO:LAMP:ISEG:FRONT:VSS_30	30	301	neg. analog supply
AMO:LAMP:ISEG:FRONT:VSS_40	40	316	neg. analog supply
AMO:LAMP:ISEG:FRONT:VDD_10	10	102	pos. analog supply
AMO:LAMP:ISEG:FRONT:VDD_20	20	115	pos. analog supply
AMO:LAMP:ISEG:FRONT:VDD_30	30	302	pos. analog supply
AMO:LAMP:ISEG:FRONT:VDD_40	40	315	pos. analog supply
AMO:LAMP:ISEG:FRONT:VSST_10	10	103	neg. driver supply
AMO:LAMP:ISEG:FRONT:VSST_20	20	114	neg. driver supply
AMO:LAMP:ISEG:FRONT:VSST_30	30	303	neg. driver supply
AMO:LAMP:ISEG:FRONT:VSST_40	40	314	neg. driver supply
AMO:LAMP:ISEG:FRONT:VDDT_10	10	104	pos. driver supply
AMO:LAMP:ISEG:FRONT:VDDT_20	20	113	pos. driver supply
AMO:LAMP:ISEG:FRONT:VDDT_30	30	304	pos. driver supply
AMO:LAMP:ISEG:FRONT:VDDT_40	40	313	pos. driver supply
AMO:LAMP:ISEG:FRONT:VSSD_10	10	105	neg. digital supply
AMO:LAMP:ISEG:FRONT:VSSD_20	20	112	neg. digital supply
AMO:LAMP:ISEG:FRONT:VSSD_30	30	305	neg. digital supply
AMO:LAMP:ISEG:FRONT:VSSD_40	40	312	neg. digital supply
AMO:LAMP:ISEG:FRONT:VDDD_10	10	106	pos. digital supply
AMO:LAMP:ISEG:FRONT:VDDD_20	20	111	pos. digital supply
AMO:LAMP:ISEG:FRONT:VDDD_30	30	306	pos. digital supply
AMO:LAMP:ISEG:FRONT:VDDD_40	40	311	pos. digital supply
AMO:LAMP:ISEG:FRONT:VDDD_10	10	106	pos. digital supply
AMO:LAMP:ISEG:FRONT:VDDD_20	20	111	pos. digital supply
AMO:LAMP:ISEG:FRONT:VDDD_30	30	306	pos. digital supply
AMO:LAMP:ISEG:FRONT:VDDD_40	40	311	pos. digital supply
AMO:LAMP:ISEG:FRONT:VBST_10	10	103	curret source adjustment
AMO:LAMP:ISEG:FRONT:VBST_20	20	110	curret source adjustment
AMO:LAMP:ISEG:FRONT:VBST_30	30	307	curret source adjustment
AMO:LAMP:ISEG:FRONT:VBST_40	40	310	curret source adjustment
AMO:LAMP:ISEG:FRONT:VREF_10	10	103	curret source adjustment
AMO:LAMP:ISEG:FRONT:VREF_20	20	110	curret source adjustment
AMO:LAMP:ISEG:FRONT:VREF_30	30	307	curret source adjustment
AMO:LAMP:ISEG:FRONT:VREF_40	40	310	curret source adjustment
AMO:LAMP:ISEG:FRONT:VSSS_10	10	103	input current load support
AMO:LAMP:ISEG:FRONT:VSSS_20	20	110	input current load support
AMO:LAMP:ISEG:FRONT:VSSS_30	30	307	input current load support
AMO:LAMP:ISEG:FRONT:VSSS_40	40	310	input current load support

Table 16: CAMEX ASIC supply voltages for front detector modules with corresponding channel numbers for the WIENER power supply. For rear detector modules exchange :FRONT: by :BACK: in the PV name.

PV name	Pos.	Ch.	description
AMO:LAMP:ISEG:FRONT:P5V_IP_BUF_12	10+20	401	pos. buffer, vacuum PCB
AMO:LAMP:ISEG:FRONT:P5V_IP_BUF_34	30+40	409	pos. buffer, vacuum PCB
AMO:LAMP:ISEG:FRONT:N5V_IP_BUF_12	10+20	402	neg. buffer, vacuum PCB
AMO:LAMP:ISEG:FRONT:N5V_IP_BUF_34	30+40	410	neg. buffer, vacuum PCB
AMO:LAMP:ISEG:FRONT:P5V_ADC_BUF_12	10+20	403	pos. buffer, mAP
AMO:LAMP:ISEG:FRONT:P5V_ADC_BUF_34	30+40	411	pos. buffer, mAP
AMO:LAMP:ISEG:FRONT:N5V_ADC_BUF_12	10+20	404	neg. buffer, mAP
AMO:LAMP:ISEG:FRONT:N5V_ADC_BUF_34	30+40	412	neg. buffer, mAP

Table 17: Auxiliary supply voltages for front detector modules with corresponding channel numbers for the WIENER power supply. For rear detector modules exchange :FRONT: by :BACK: in the PV name.

9.3 Cables

9.3.1 Analog signal cables (LEMO)

The analog signal cables are 6 m long shielded Twinax cables from *TEMP-FLEX Cables Inc.* which can be ordered at Mousers (order no 100TX-08). It is 32 AWG and has a differential impedance of 100 Ω. On both sides there are LEMO FGG.00.302.CLAD22 connectors.

first connector	cable	second connector
LEMO pin 1	twinax cable 1a	LEMO pin 1
LEMO pin 2	twinax cable 1b	LEMO pin 2
LEMO shield	twinax shield	LEMO shield

Table 18: Analog signal cable pinout

9.3.2 Power supply cables (REDEL)

The main power cables do all have the same pin and cable mapping. reftab:redel There are long cables (6 m) for connections between control rack and data box and short cables (1 m) for interconnection in the rack. Each cable has got a female and a male REDEL connector. The male connector made by LEMO (SAG.H51) has 34 crimp contacts for normal voltage pins (ERA.05.403.ZLL1) and 2 crimp contacts for the safety loop (EGG.3B.665.ZZM). The crimp contacts are individually protected by heatshrink tubes (GMA.30.010.ST). The common shield of the cable is only connected to the shield of the SAG.H51 (male) connector. The cable shielding is not connected on the SAA.H51 (female) side. On the SAA.H51 side there are 34 crimp contacts (FFA.05.403.ZLA1) plus 2 crimp contacts (FGG.2B.565.ZZC). Again, every crimp contact is secured by a heatshrink tube (GMA.30.010.ST).

The cable is 18x2xAWG26 and is manufactured by Helektra (www.helektra.de), type 2LVCC-CY, order number 1108776. The cable contains 18 pairs of twisted cables. Each twisted pair (e.g. cable 1a and 1b) is used for a corresponding pair of power supply contacts (e.g. CH0 and CH0 Return).

There is an assembly tube for the guide pins (DCT.91.551.0LA) and an extraction tool for the high voltage pins (DCF.91.133.5LT).

connector power supply side REDEL SAG.H51 (male)				connector data side REDEL SAA.H51 (female)		
pin	function	crimp contact	cable	pin	function	crimp contact
2	CH0	ERA.05.403.ZLL1	<– 1a –>	2	CH0	FFA.05.403.ZLA1
3	CH1	ERA.05.403.ZLL1	<– 2a –>	3	CH1	FFA.05.403.ZLA1
4	CH2	ERA.05.403.ZLL1	<– 3a –>	4	CH2	FFA.05.403.ZLA1
5	CH3	ERA.05.403.ZLL1	<– 4a –>	5	CH3	FFA.05.403.ZLA1
6	CH4	ERA.05.403.ZLL1	<– 5a –>	6	CH4	FFA.05.403.ZLA1
7	CH5	ERA.05.403.ZLL1	<– 6a –>	7	CH5	FFA.05.403.ZLA1
8	CH6	ERA.05.403.ZLL1	<– 7a –>	8	CH6	FFA.05.403.ZLA1
9	CH7	ERA.05.403.ZLL1	<– 8a –>	9	CH7	FFA.05.403.ZLA1
10	spare 1	ERA.05.403.ZLL1	<– 18a –>	10	spare 1	FFA.05.403.ZLA1
13	CH0 RTN	ERA.05.403.ZLL1	<– 1b –>	13	CH0 RTN	FFA.05.403.ZLA1
14	CH1 RTN	ERA.05.403.ZLL1	<– 2b –>	14	CH1 RTN	FFA.05.403.ZLA1
15	CH2 RTN	ERA.05.403.ZLL1	<– 3b –>	15	CH2 RTN	FFA.05.403.ZLA1
16	CH3 RTN	ERA.05.403.ZLL1	<– 4b –>	16	CH3 RTN	FFA.05.403.ZLA1
17	CH4 RTN	ERA.05.403.ZLL1	<– 5b –>	17	CH4 RTN	FFA.05.403.ZLA1
18	CH5 RTN	ERA.05.403.ZLL1	<– 6b –>	18	CH5 RTN	FFA.05.403.ZLA1
19	CH6 RTN	ERA.05.403.ZLL1	<– 7b –>	19	CH6 RTN	FFA.05.403.ZLA1
20	CH7 RTN	ERA.05.403.ZLL1	<– 8b –>	20	CH7 RTN	FFA.05.403.ZLA1
21	spare 2	ERA.05.403.ZLL1	<– 18b –>	21	spare 2	FFA.05.403.ZLA1
22	SL 1	EGG.3B.665.ZZM	<– 9a –>	22	SL 1	FGG.2B.565.ZZC
30	SL 2	EGG.3B.665.ZZM	<– 9b –>	30	SL 2	FGG.2B.565.ZZC
32	CH15	ERA.05.403.ZLL1	<– 10a –>	32	CH15	FFA.05.403.ZLA1
33	CH14	ERA.05.403.ZLL1	<– 11a –>	33	CH14	FFA.05.403.ZLA1
34	CH13	ERA.05.403.ZLL1	<– 12a –>	34	CH13	FFA.05.403.ZLA1
35	CH12	ERA.05.403.ZLL1	<– 13a –>	35	CH12	FFA.05.403.ZLA1
36	CH11	ERA.05.403.ZLL1	<– 14a –>	36	CH11	FFA.05.403.ZLA1
37	CH10	ERA.05.403.ZLL1	<– 15a –>	37	CH10	FFA.05.403.ZLA1
38	CH9	ERA.05.403.ZLL1	<– 16a –>	38	CH9	FFA.05.403.ZLA1
39	CH8	ERA.05.403.ZLL1	<– 17a –>	39	CH8	FFA.05.403.ZLA1
43	CH15 RET	ERA.05.403.ZLL1	<– 10b –>	43	CH15 RET	FFA.05.403.ZLA1
44	CH14 RET	ERA.05.403.ZLL1	<– 11b –>	44	CH14 RET	FFA.05.403.ZLA1
45	CH13 RET	ERA.05.403.ZLL1	<– 12b –>	45	CH13 RET	FFA.05.403.ZLA1
46	CH12 RET	ERA.05.403.ZLL1	<– 13b –>	46	CH12 RET	FFA.05.403.ZLA1
47	CH11 RET	ERA.05.403.ZLL1	<– 14b –>	47	CH11 RET	FFA.05.403.ZLA1
48	CH10 RET	ERA.05.403.ZLL1	<– 15b –>	48	CH10 RET	FFA.05.403.ZLA1
49	CH9 RET	ERA.05.403.ZLL1	<– 16b –>	49	CH9 RET	FFA.05.403.ZLA1
50	CH8 RET	ERA.05.403.ZLL1	<– 17b –>	50	CH8 RET	FFA.05.403.ZLA1
	shield		cable shield			

Table 19: REDEL cable pinout