HPS SVT Review, November 5, 2013

SVT Data Acquisition

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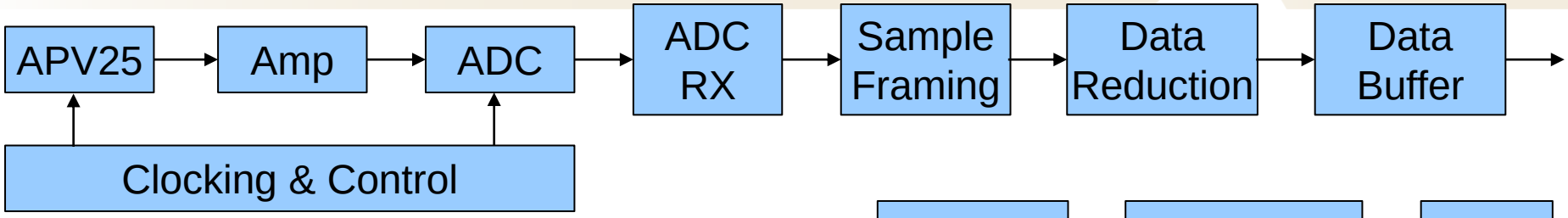
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

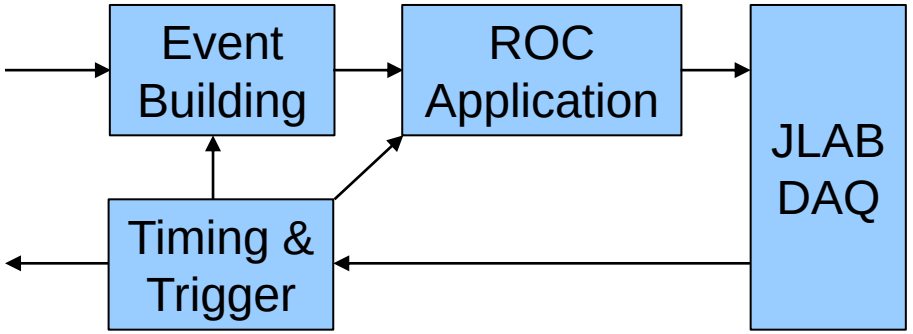
Overview

- Generic SVT data flow
- HPS Test beam DAQ
  - Major components
  - Lessons learned
- HPS requirements
- HPS DAQ configuration
- New work required for HPS
- Integration testing strategy
- Effort
- Schedule
- Budget

SVT Data Flow

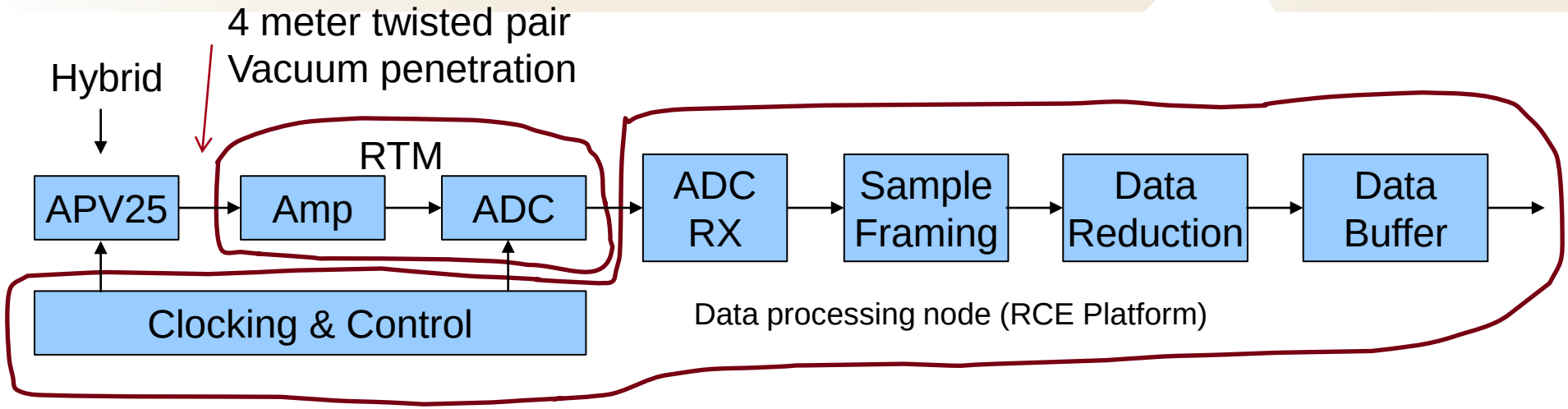


- APV25 support
  - Amplifier for current to voltage conversation
  - Scale to ADC input range of +/- 1V
- Clocking and control
  - APV25 configuration and monitoring
  - ADC clocking and sample phase control
- ADC RX
  - Convert ADC serial data to parallel samples
- Sample framing
  - Initial ADC data processing
  - Sync detect
  - Framing and reorganization of samples
- Data reduction
  - Firmware based edge detect
  - Baseline subtraction
  - Threshold compare
- Data buffer
  - Memory for storing N events

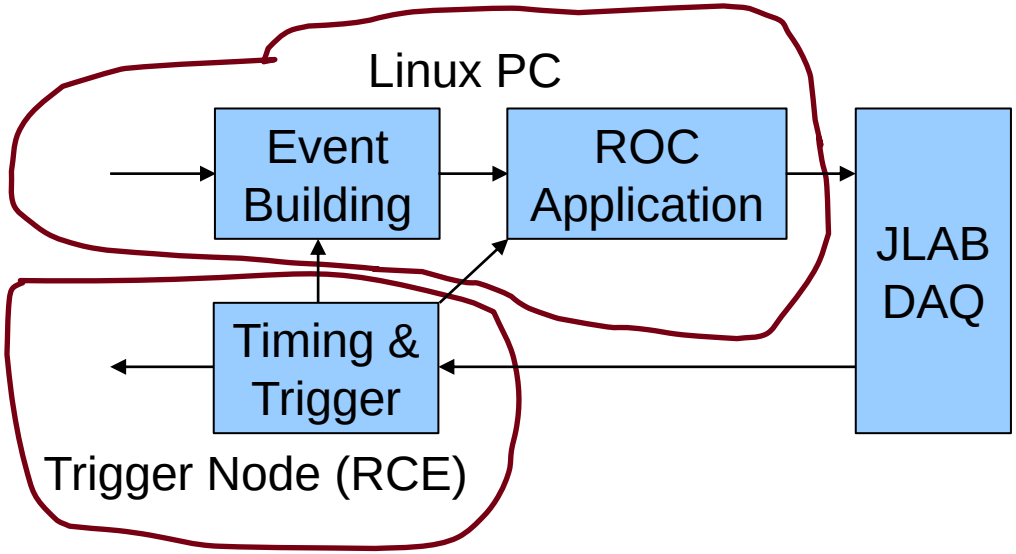


- Event Building
  - Combine event data from multiple sources
  - Add trigger/timing information
  - Combine multiple events into large blocks
- Timing and trigger
  - Receive timing and trigger data from JLAB
  - Distribute to front ends
- ROC application
  - State control
  - Ethernet communication to JLAB DAQ
  - Event record passing

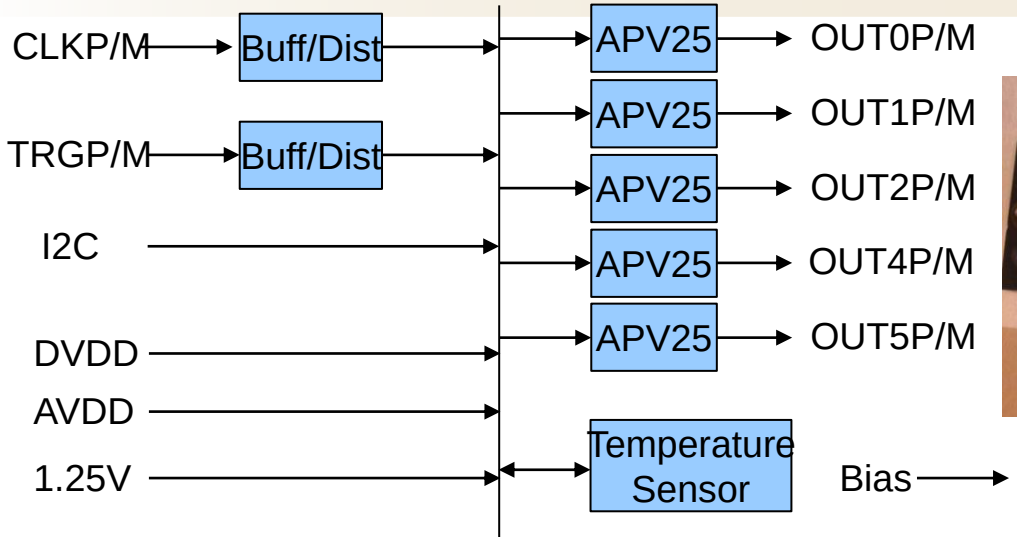
HPS Test SVT Data Acquisition

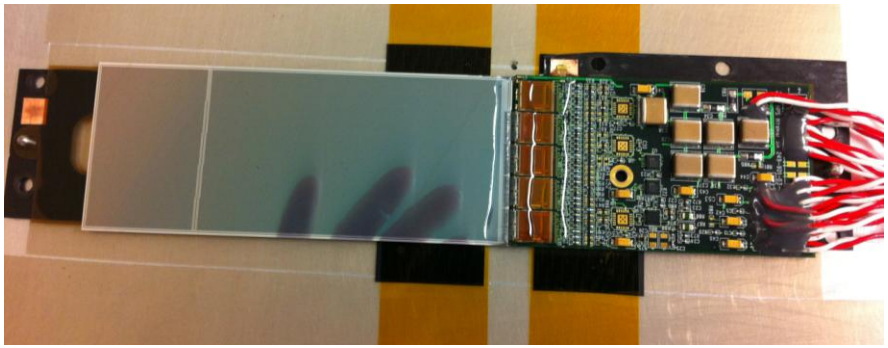


- Internal chamber electronics
  - APV25 mounted on hybrid
- RCE Platform
  - Dual ATCA blades
  - Analog RTMs (rear transition module)
  - 7 data processing nodes
  - 1 trigger processing node
- External Linux PC
  - ROC application
  - Standard Ethernet NIC for configuration traffic
  - Custom Ethernet NIC for low latency data
- Large vacuum penetration count
  - Fragile connections
  - Impedance mismatches
- RCE platform close to chamber



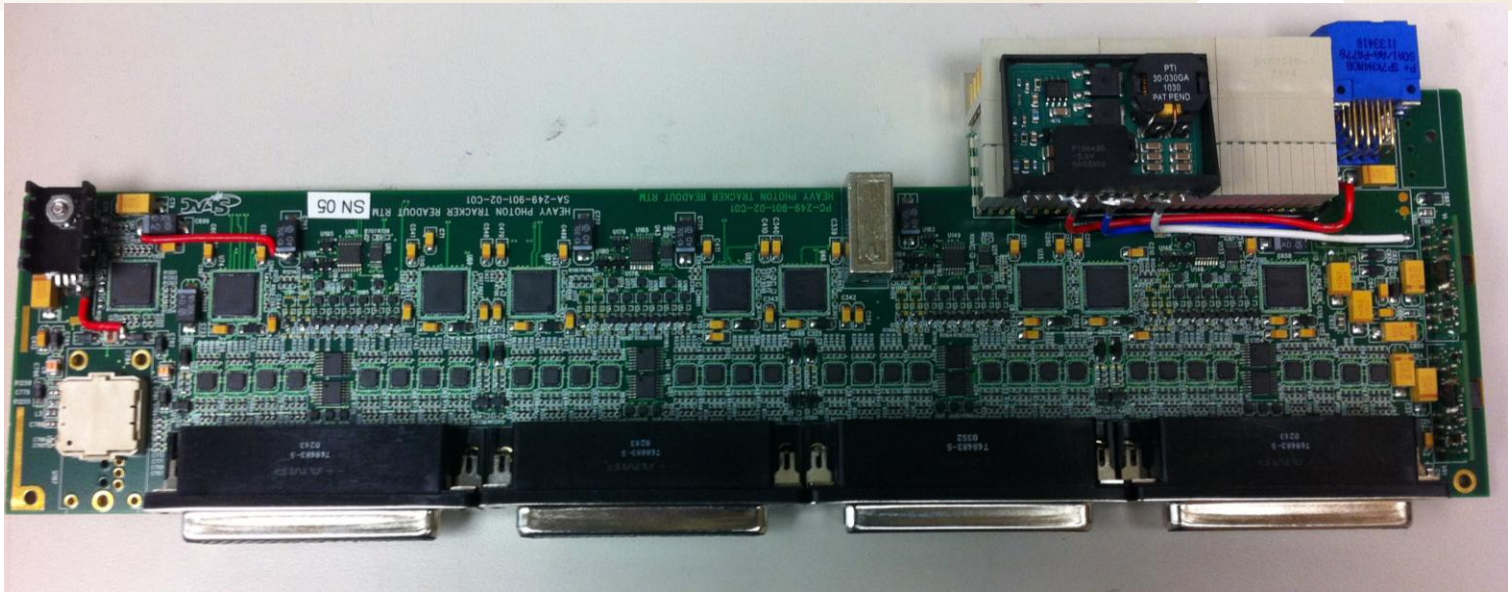
SVT Hybrid





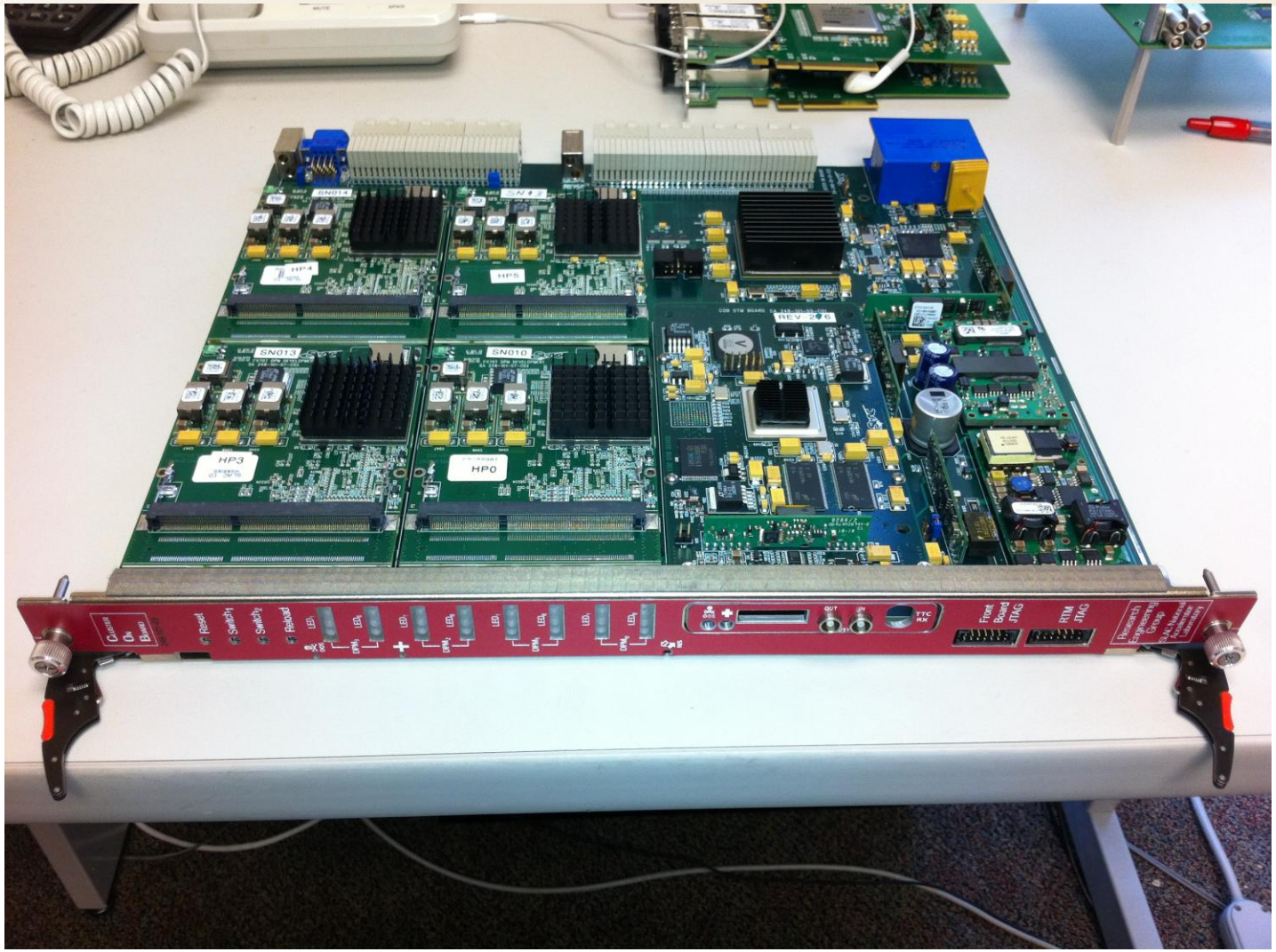
- Incoming clock & trigger buffered, 2 loads per output (2.5V supply)
- I2C bus for APV25 configuration & temperature sensor readout
- Power inputs distributed to all parts
- Bias routed directly to wire bond pads with local bypassing
- Existing hybrid had loading options to allow AP25 outputs to be buffered
  - We determined this was not required
- Existing hybrid connects through twisted pair cables and DB25 connector
  - Defined by short schedule
  - Problematic for bias voltages above 500V

SVT HPS Test RTM



- HPS Test
  - 60 Channels of buffer and ADC
  - Power sourced from “dirty” ATCA distributed voltages
  - Option for JLAB trigger interface (disables 15 ADC channels)
  - First spin board with power reworks
  - DB50 connectors to interface to twisted pair signals from vacuum chamber

RCE Platform GEN2 COB



HPS Test Issues

- Reflections discovered in long run cables with vacuum flange
  - FPGA based FIR added to design
  - Downstream reflections on clock and trigger may cause stability issues
- Clock & trigger skews discovered in long run cables
  - ADC sample adjustment applied per FPGA instead of per hybrid
  - Hybrids on the same FPGA did not necessary want the same ADC phase adjustment
  - ADC sample phase adjustment did not cover full clock cycle (edge +7nS)
- Occasional noisy hybrids and lost sync during runs
  - Once per hour level problem
  - Possibly cause is cable reflections on clock & trigger lines
  - Possibly cause is noise pickup on long cables causing clock & trigger glitches
  - Longer duration system testing required
- ATCA power supply failure
  - Most likely due to radiation
- APV25 trigger rate limited to 43Khz (theoretical fixed rate trigger)
  - Limit is due to enforced dead time during APV25 readout
  - Trigger serialized with readout
  - FPGA firmware did not support APV25 burst capabilities
- Event building & ROC limitations
  - Linux PC based ROC was rate limited
  - Max data rate of ~16Khz at 1 event per APV per trigger (test mode data)
  - Limited by supported buffer depth (8 events)
  - ROC application did not support event bundling
  - Limited by Ethernet latency and bandwidth

Commissioning Issues

Requirements for HPS

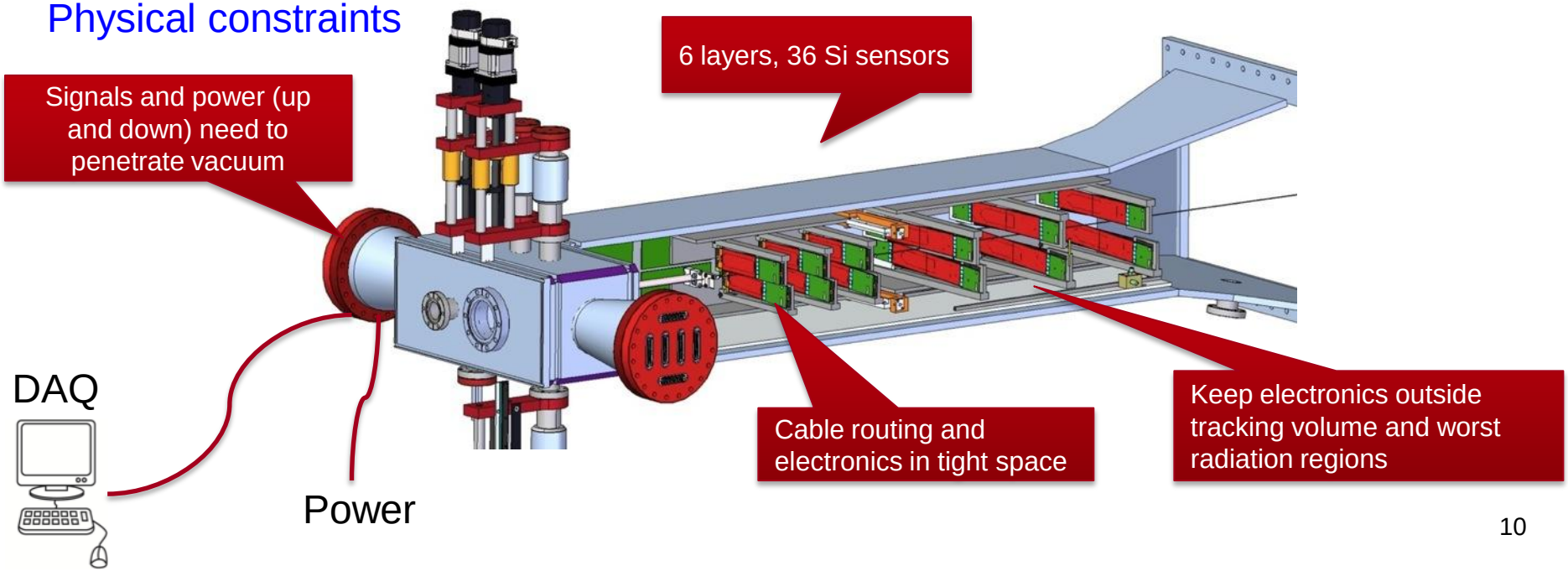
Basic requirements for the SVT DAQ

- Continuous 40Mhz readout of 23'040 channels
- Triggered readout of up to 50Khz
- Low noise (S/N>20 to achieve high spatial resolution)
- Facilitate hit time reconstruction ~2ns
- High bandwidth: up to 100MB/s

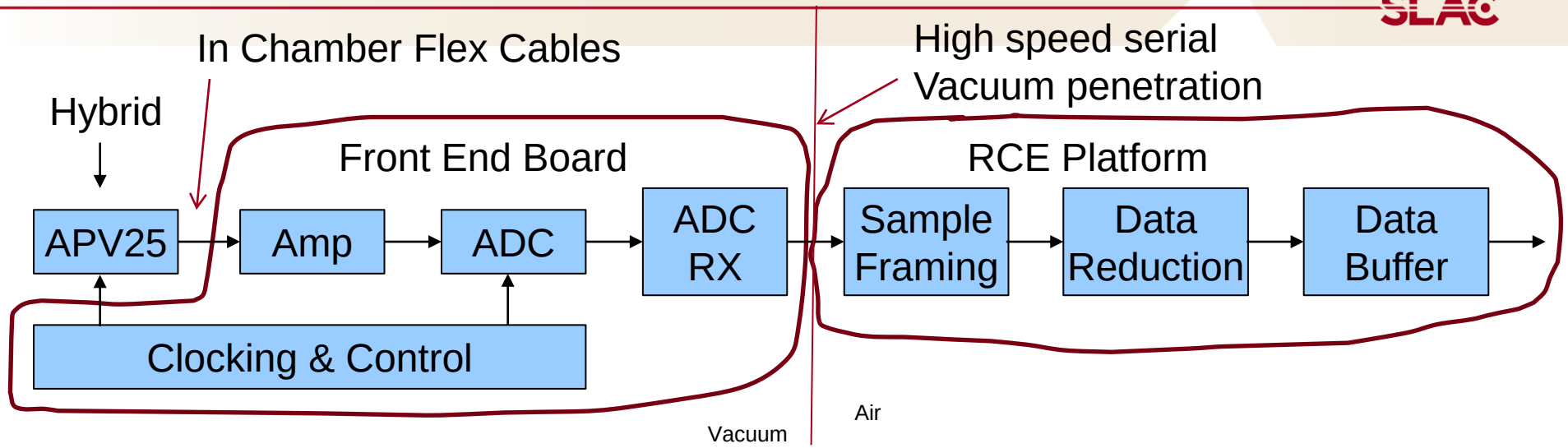
Additional requirements

- 16 more hybrids to support additional layers
  - 40% increase in signal and power density & data bandwidth

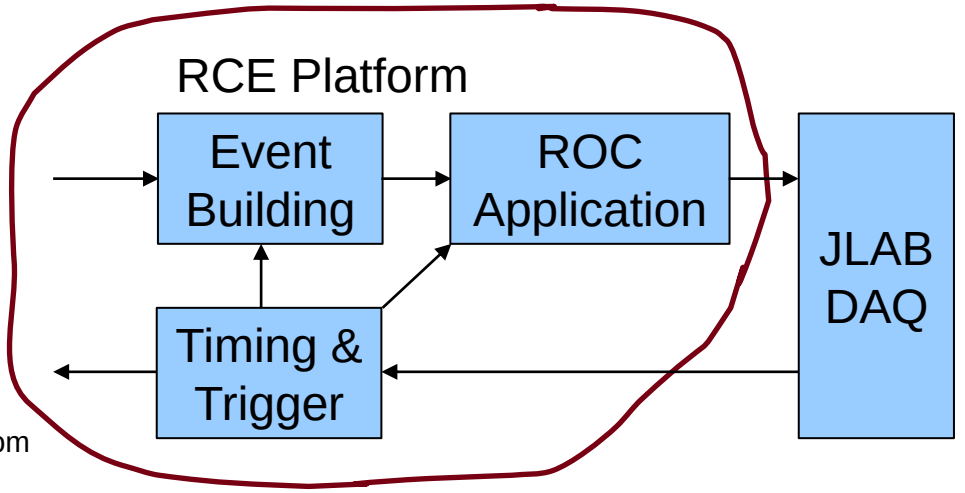
Physical constraints



SVT Data Acquisition For HPS



- Create new in vacuum front end board
  - Shortens distance between APV25 and ADC
  - APV25 signals & power transported over impedance controlled flex cables
  - Local power conversion for hybrids
  - Send ADC samples over high speed serial link to RCE platform
  - Minimal firmware features (avoid updates)
- Convert from electrical to optical at vacuum flange
  - Allows longer distance transmission of high speed lines outside of vacuum chamber (Move ATCA crate away from the beam)
  - Optimizes flange space for signal and power
- Move event builder and ROC to RCE platform
  - Increase size of event blocks (reduce per event overhead)



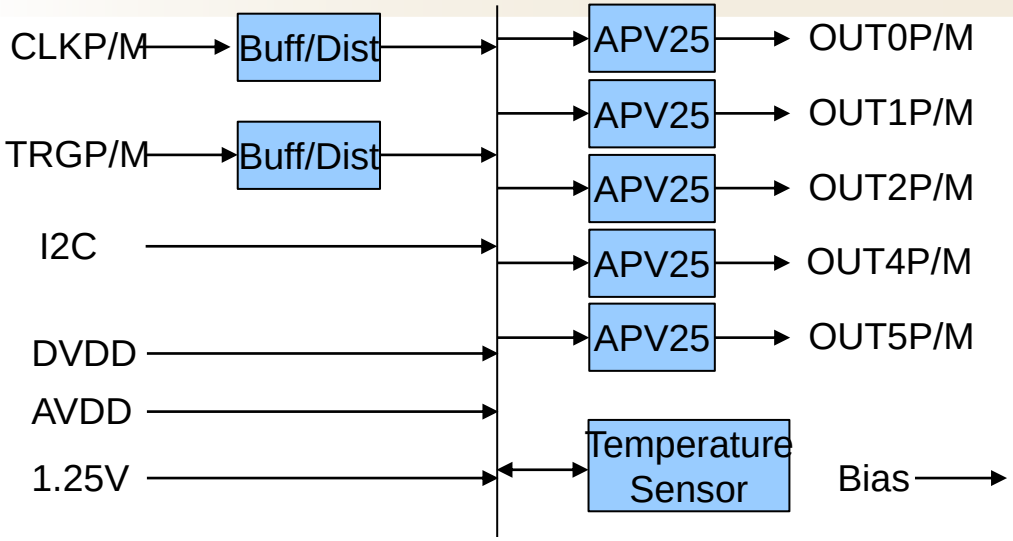
Power Distribution Changes

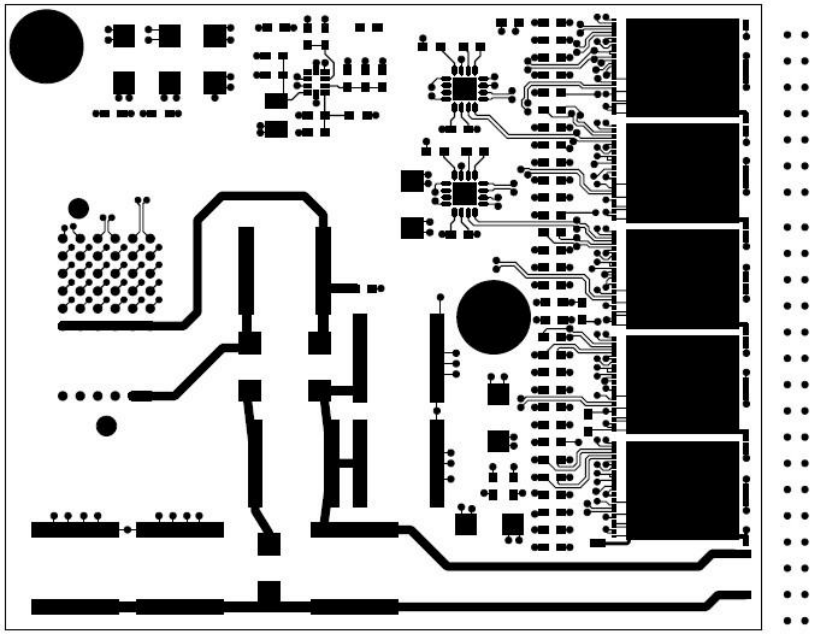
- HPS Test provided all power from external supplies
  - Per hybrid:
    - DVDD: 2.5V (no sense)
    - AVDD: 2.5V (with sense)
    - V125: 1.25V (with sense)
    - Bias: 190V (no sense)
- HPS will distribute power at front end card
  - Per front end card
    - DVDD: 5-7V
    - AVDD: +/- 5-7V
    - 4 channels of detector Bias: 190V (design for up to 1KV)
  - Front end card provides hybrid power control & monitoring
    - Bridge to epics controls through DAQ
    - Per hybrid power on/off control
    - Per hybrid low voltage current monitoring
    - Bias control & monitoring done at supplies (direct link to epics)

New Hardware For HPS

- Layer 4-6 Hybrid Boards
  - Required to support additional tracker layers
  - Low risk changes to existing hybrid schematics
- Front end board
  - Required to minimize in chamber cabling and shorten cable lengths
  - Analog portion uses existing RTM schematic blocks
  - Uses Xilinx Kintex-7 FPGA
  - Power conversion and distribution for hybrid boards based on existing designs
  - High speed digital serial outputs use miniSAS cables tested for LSST project
- Vacuum flex cables
  - Required to simplify in vacuum cabling
  - SLAC has experience with flex cables of this nature
- Vacuum flange board
  - Required to optimize vacuum flange feed through density
  - New development at SLAC being targeted towards multiple projects
  - Based on LSST R&D but custom board for HPS project
- Gen 3 RCE Platform
  - RCE components purchased from DAQ R&D
  - 1 simple custom RTM mezzanine board for HPS (timing & trigger interface)

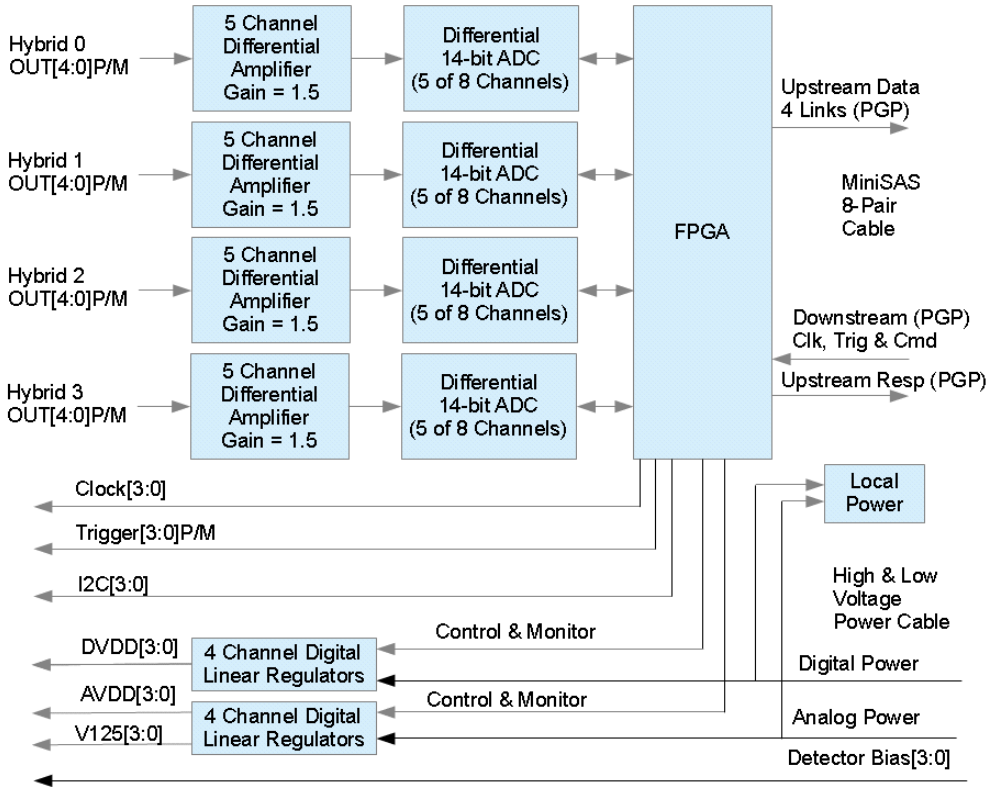
New SVT Hybrid





- Existing Hybrids for layers 1-3
  - Bias voltages routed to separate connector
    - Testing on existing twisted pair shows we can operate at 1KV
  - Interface board to connect DB25 signals to flex cable
    - Short path from hybrid to flex cable
    - Flex cable design has not yet started
      - Still some outstanding interface questions
- New Layer 4-6 Hybrid Boards
  - Required to support additional tracker layers
  - Remove unused components to shrink board size
  - Schematic and layout complete
    - System review last week
    - Some minor changes related to GND and signals returns
    - Expect to release board within the week

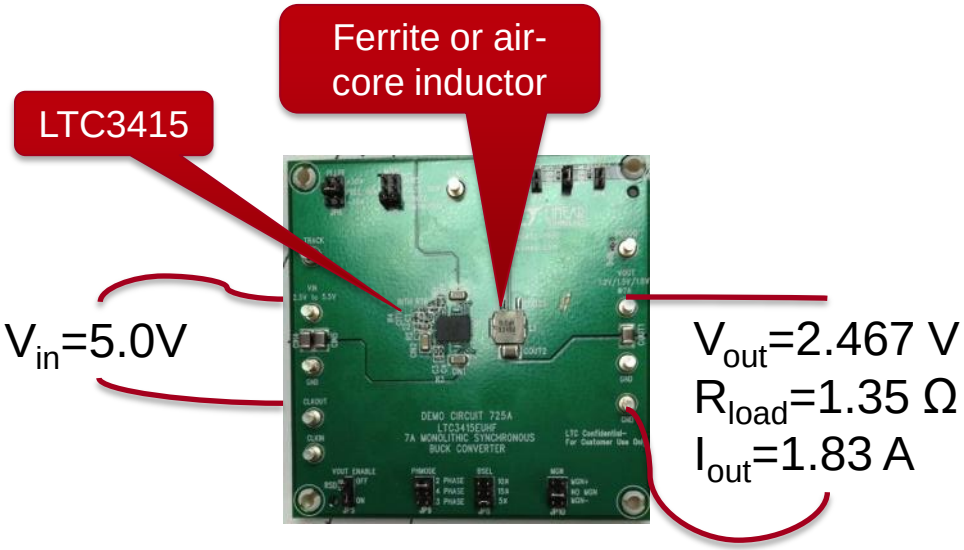
New Front End Board

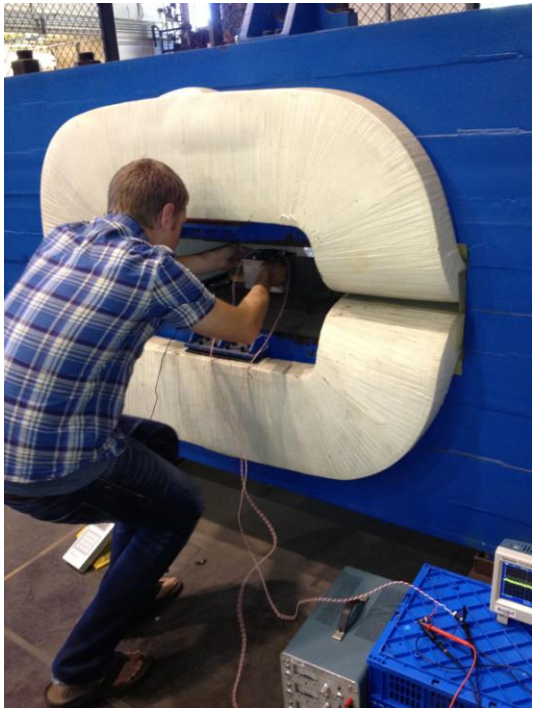


- New front end board supports up to 4 hybrids
  - 6 for layers 4-6, 3 top, 3 bottom (4 hybrid each)
  - 4 for layers 1-3, 2 top, 2 bottom (3 hybrids each)
- Schematic complete, waiting for layout

Magnetic Field & Vacuum Testing

- Concern with specific front end board components in a magnetic field
  - Metal encased oscillators
  - Solid core inductors used in modular switching supplies
- Front end board addresses these issues
  - Non-metal cased oscillators have been sourced
  - Air core inductor based switching supply has been designed and tested
- All components have been vacuum tested

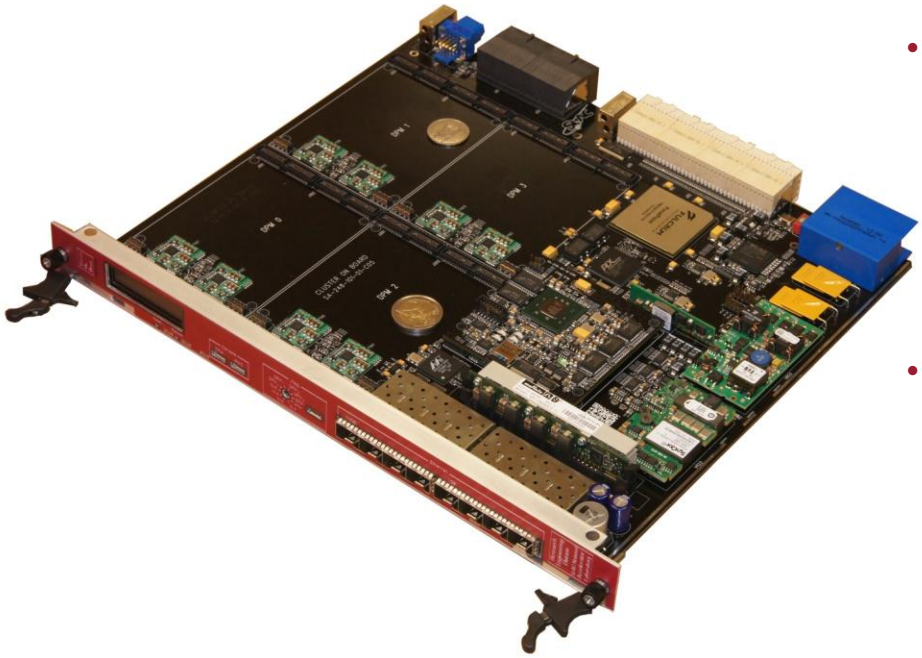


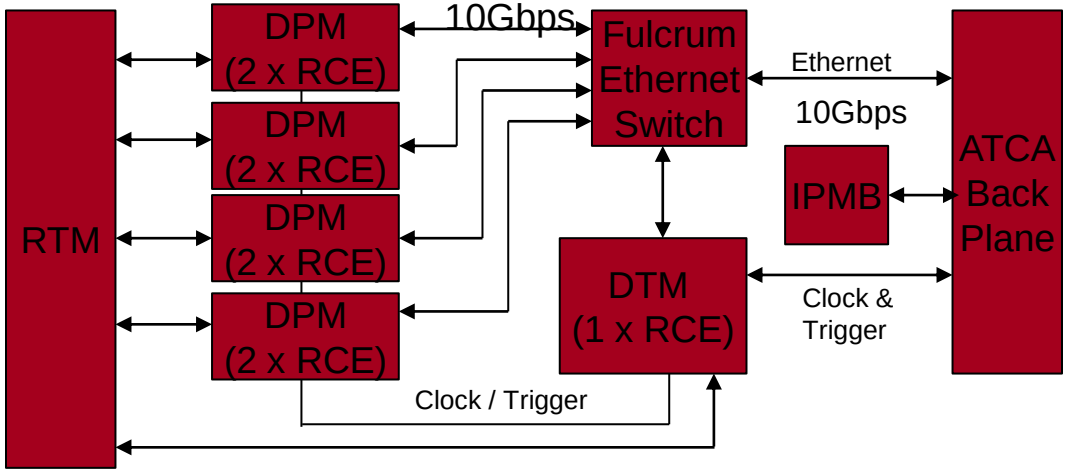


Flex Cables & Flange Boards

- Flex Cables
  - Connectors at hybrid and front end board have been selected
  - Exact mechanical form factors yet to be determined
  - Schematics are very simple
- Flange Boards
  - Two separate types are required, power and signal
  - Flange board for signal penetration is complete, waiting for layout
    - 1 board to support 3 front end boards
    - 4 flange boards mounted in 6” flange
    - All active components are socketed
      - Power supplies
      - Optical modules
  - Flange board for power has not yet been designed
    - Need to pick internal and external power connectors
    - Bias power connectors may be a challenge

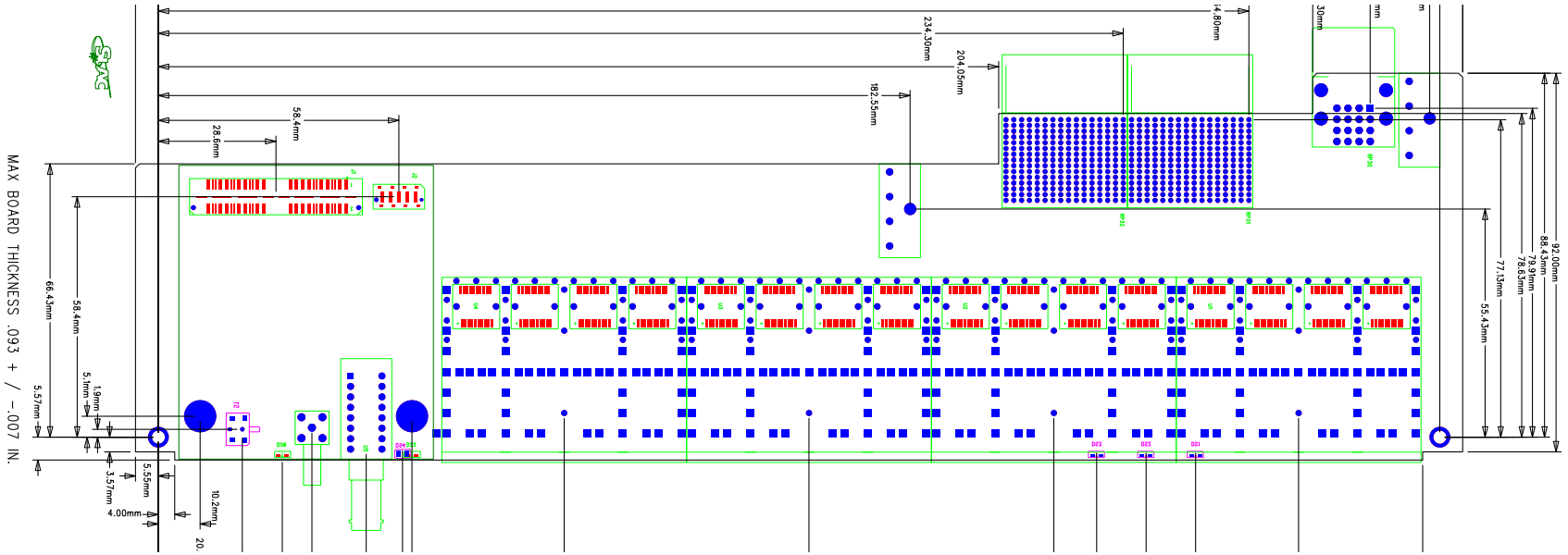
SLAC GEN3 RCE Platform





- Developed by SLAC under generic DAQ R&D program (Huffer, Haller, Herbst)
  - Core software and firmware with hooks for experiment specific software and firmware
  - Strong internal support for base platform as well as assistance with custom development
- COB (Cluster On Board)
  - Carries 1 DTM (Data Transport Module)
    - Single RCE for switch management & timing distribution
  - Carries 4 DPM (Data processing module) daughter boards
    - Each DPM supports 2 RCE (Reconfigurable Cluster Element)
      - RCE is Xilinx ZYNQ based FPGA with embedded ARM processor
      - Provides data processing firmware and software
      - High rate DAQ engine targeted towards > 100Khz trigger rates
      - Supports RTEMs & Linux

SLAC GEN3 RCE Platform

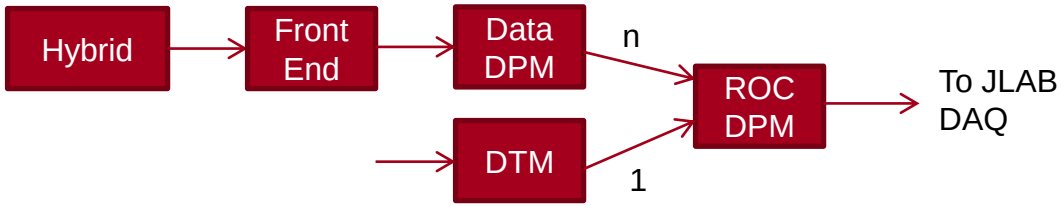


- Standard SLAC RTM
  - 12 bi-directional channels per RCE
  - Will use Fiber patch panel to interface to flange boards
- RCE/RTM Status
  - Rev1 COB, DTMs & DPMs tested
  - Rev1 DPMs had memory problems due to manufacturing defects
  - Rev 2 DPMs in house last week, manufacturing problems resolved
  - Rev2 COBs arrive this week (minor fixes and updated clock distribution)
  - Rev2 DTMs next month (minor fixes)
  - RTM due by end of the year
- HPS RTM Mezzanine Card
  - Due by end of the year

New Firmware For HPS

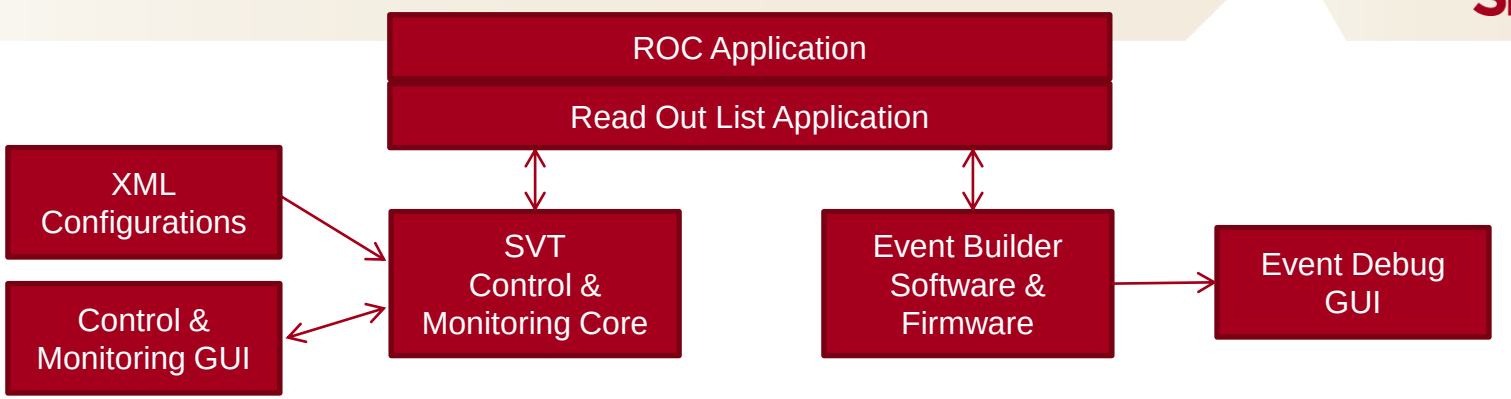
- Front end board firmware
  - Reuse configuration and ADC interface firmware blocks
  - Create Kintex-7 PGP2 GTP interface firmware (completed)
  - Reuse major PGP2 blocks (data transport, register read/write)
  - New I2C controller for improved stability (completed)
  - New register address interconnect (completed)
  - Improved ADC sample phase control (full clock cycle granularity) (completed)
  - Low risk firmware effort
  - Need simplified standalone version (Ethernet) for Hybrid testing
- Data processing firmware (RCE Platform)
  - Reuse major blocks (filter, sample packing, data reduction)
  - Add support for burst triggers in APV25
  - Add firmware support software event blocking & buffering
  - Low risk firmware effort
- Trigger firmware (RCE Platform)
  - Integrated official JLAB TI firmware
  - Modifications for new timing/trigger distribution structure
  - Low risk firmware effort

New SVT Data Flow



- RCE platform is fully configurable
  - 2 COB operating an independent units
    - 10 data RCEs and 2 ROC RCEs
    - 1 front end per RCE
    - 2 DTM RCEs for trigger interface
- Data RCE processes raw ADC data
  - Event builds data at full trigger rate (50Khz)
  - Packs events into blocks defined by buffer size
    - Estimate 32 – 40 events per block
    - Blocks are then forwarded to ROC DPM over Ethernet
  - May be able to run Linux but RTEMS will have better performance
- ROC RCE accepts event blocks from data RCE nodes and trigger RCE node (DTM)
  - Operates at lower rate of trigger rate / block size (~1 – 2 Khz)
  - Arm Linux

New SVT DAQ Software



- Readout List Application
  - Front end specific code developed by SLAC
  - Shared memory interface to control and data modules
  - Interface to JLAB
    - New version with minimal library requirements provided by JLAB (Sergey)
- SVT Control & Monitoring Core Software
  - Interface to data processing RCEs, front end boards & APV25s
  - Configurations pulled from XML files
  - Local control & monitoring GUI
  - Slave to ROC and readout out list applications during run
  - Based on existing generic DAQ software
  - Minor changes from test run version
- Event builder software
  - Interface to event building firmware layer
  - Hooks for SVT specific debug display
  - Handoff to read out list application
- Slow Controls
  - Provides bridge between front end board control and EPICs
  - Required for hybrid power supply control and monitoring
  - Thermal feedback

Integration Testing Strategy

- Phase 1: SLAC only software on ROC platform
  - Test data generators in firmware on each DPM
  - Trigger signal and data generators in firmware on DTM
  - Local readout list application without JLAB interface
  - Look for rate bottlenecks
- Phase 2: Add real JLAB trigger interface
  - Verify we can receive trigger information from JLAB at rate
- Phase 3: Add CODA and JLAB ROC application
  - Verify trigger rate holds up when transferring data to CODA event builder
  - Verify alignment of trigger data
  - Send as test platform to JLAB for testing against their system
- Phase 4: Add real hybrids
  - Start connecting real hybrids and SVT as modules become available

Summary of SVT DAQ

SVT DAQ for HPS based on HPS Test DAQ

- Repackaging of test run components
- Some new hardware
- Bulk of development in DAQ software

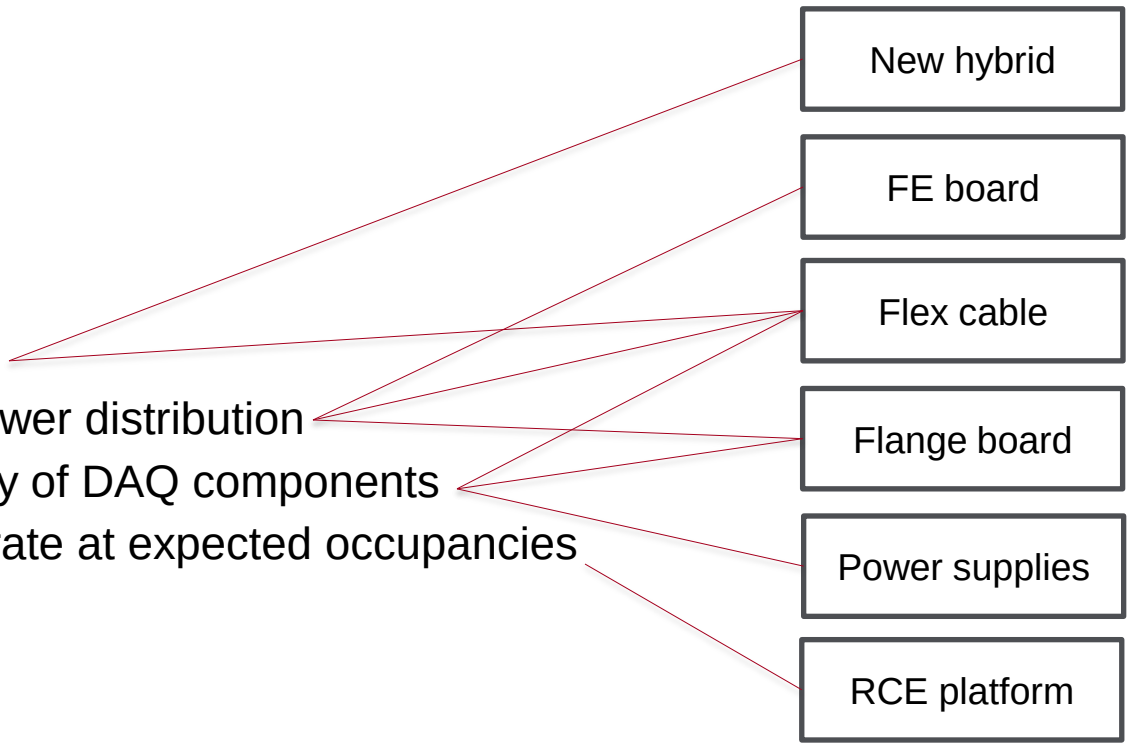
Upgrades driven by

- Mitigate test run issues
- Support additional 16 hybrids
- Improve performance

Key features

- Support for new Layer 4-6
- In chamber digitization and power distribution
- Improved stability and flexibility of DAQ components
- Performance: 50kHz readout rate at expected occupancies

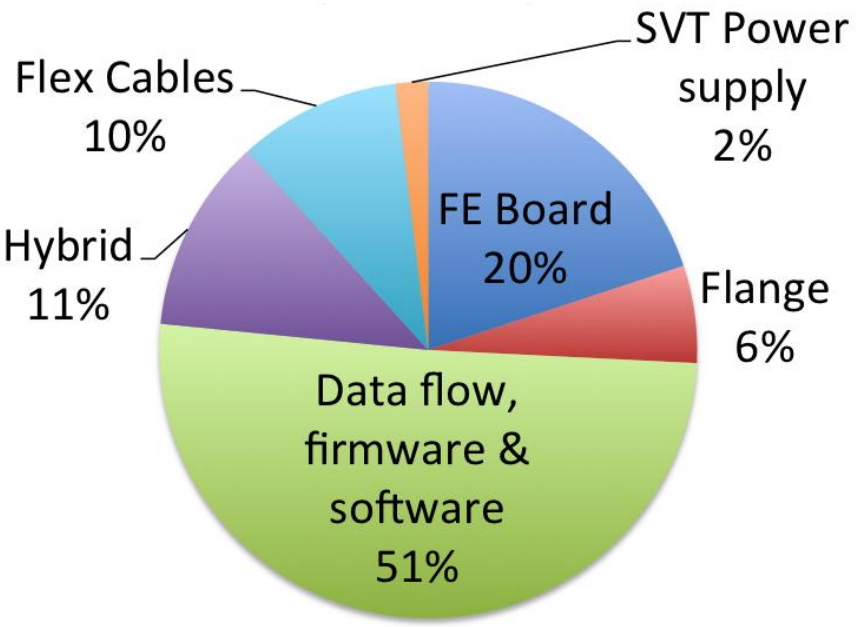
Upgrade project components



Effort Comparison

- HPS Test
  - Manpower
    - 1 FTE part time for 10 months
      - Ryan Herbst
  - R&D
    - Lots of new things to learn
      - APV25 operation
      - JLAB DAQ software and JLAB trigger hardware

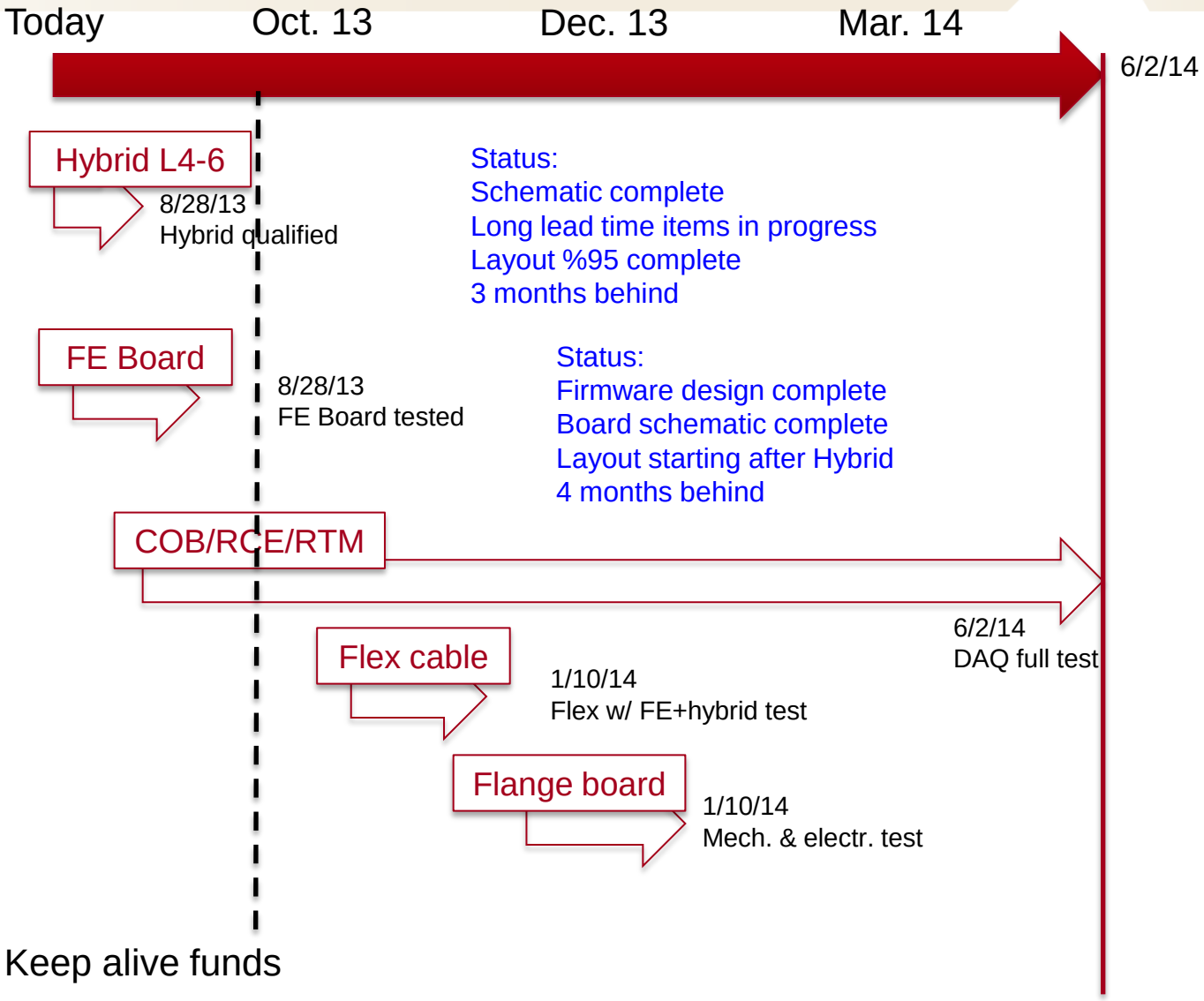
- HPS
  - Manpower
    - 2 FTEs for 18 months
      - Ben Reese (full time)
      - Ryan Herbst (part time)
    - Layout and technician support
      - Tung Phan (layout)
      - Lupe Salgado (e-shop)
    - Additional software support from physicists
      - Sho Uemura
      - Per Hansson
      - Omar Moreno
  - R&D
    - Already familiar with all major hardware components
      - New hardware leveraged from SLAC DAQ R&D
    - Familiar with JLAB DAQ software & JLAB trigger interface
    - Repackaging of existing hardware and firmware
    - Bulk of effort in embedded ROC & event builder software



Total cost: 340k$
Ave. 26% contingency

Started with keep alive funds

Project Overview

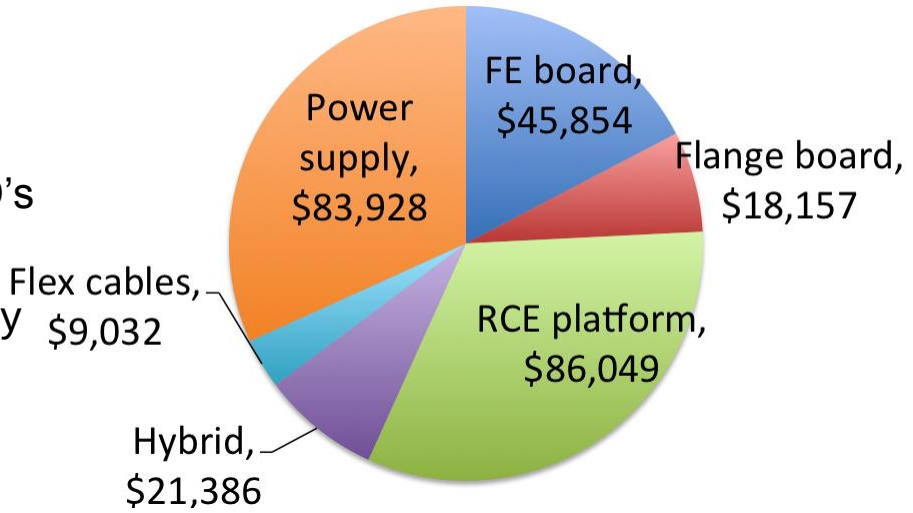


Project Budget

- BOM costs spread relatively evenly across sub-project
  - Total contingency of 33%

- High cost items has low risk
  - Power supplies are standard Wiener MPOD's
  - RCE platform components in prototype or production stage (expected Aug., need by by Nov.)
  - RCE platform purchased from SLAC DAQ group

- Keep alive funds used to keep early sub-projects on schedule
  - Long lead-time items purchased (APV25 chips for hybrids)



Total 264k$
(w/o contingency & OH)