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SVT Data Acquisition

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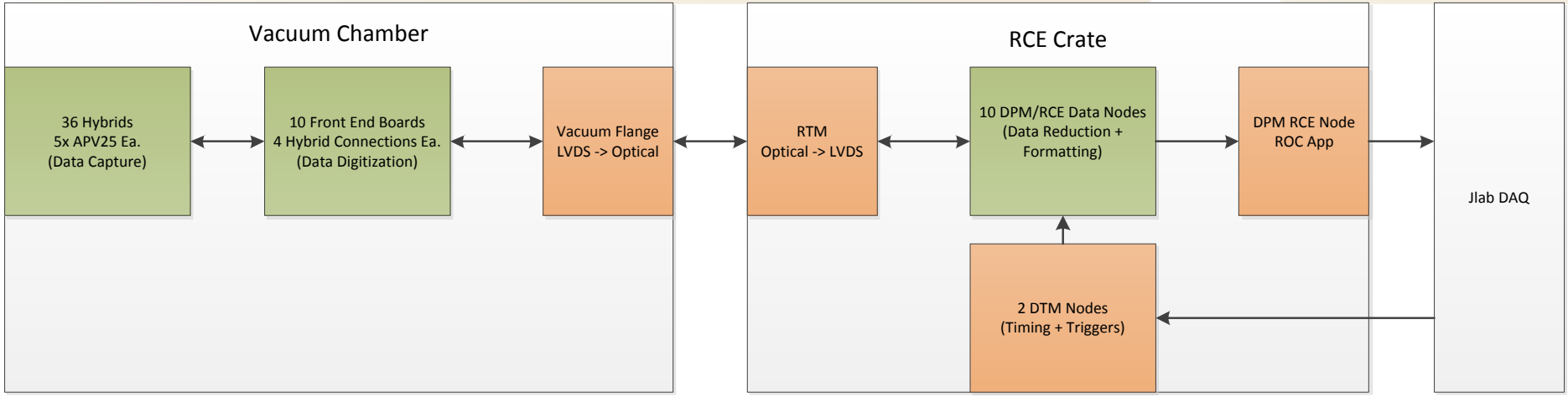
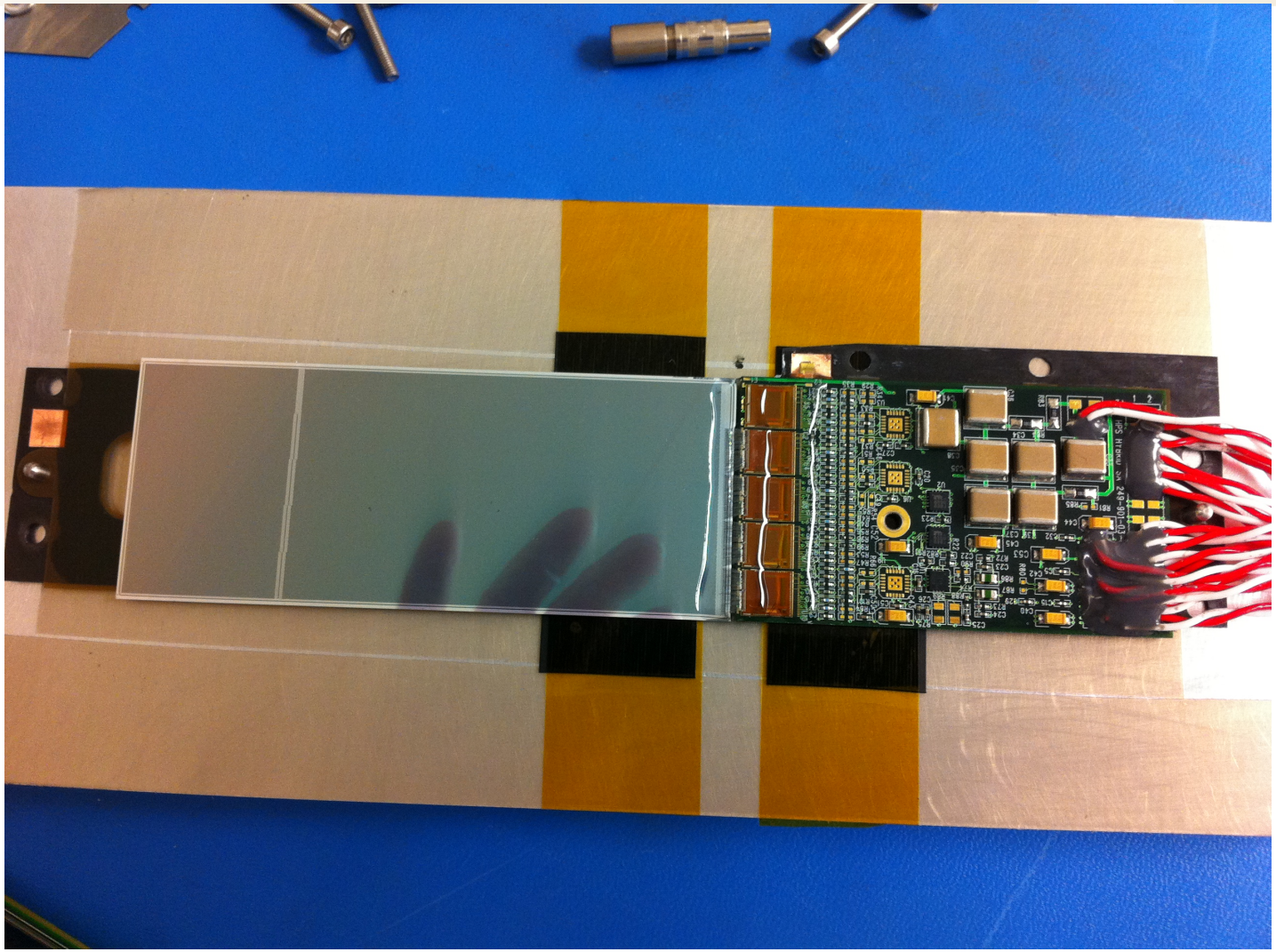
SVT Data Acquisition For 2014 Run

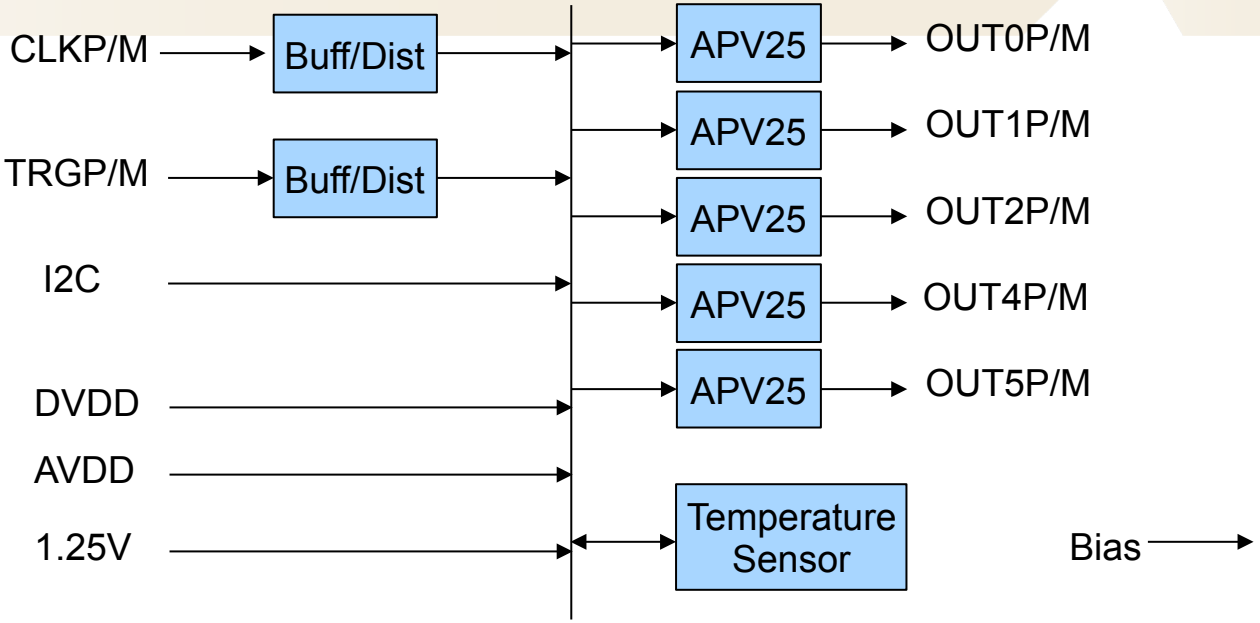


- New Hybrid boards in layers 4-6
- New Front End Boards for digitization
- Convert from electrical to optical at vacuum flange
  - Allows longer distance transmission of high speed lines outside of vacuum chamber
  - Optimizes flange space for signal and power
- Convert back to electrical at ATCA crate RTM
  - Simplified RTM does only LVDS<->Optical conversion
- Data processing done in DPM/RCE Nodes
  - New hardware
  - New firmware features
- DTM Node gets clock and triggers from JLab DAQ and distributes to RCE Nodes
- ROC app also runs on DPM/RCE Node

Hybrid Overview

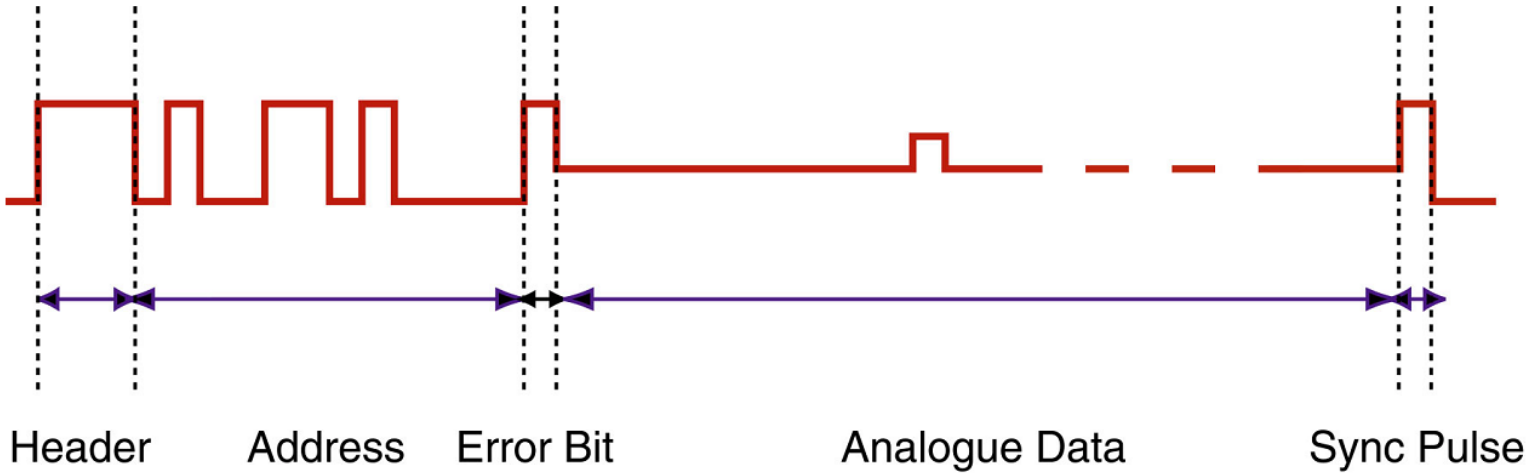


SVT Hybrid



- Incoming clock & trigger buffered, 2 loads per output (2.5V supply)
- I2C bus for APV25 configuration & temperature sensor readout
- Power inputs distributed to all parts
- Bias routed directly to wire bond pads with local bypassing
- New Layer 4-6 Hybrid Boards
  - Required to support additional tracker layers
  - Remove unused components to shrink board size
  - Low risk changes

APV25 Configuration & Readout



- Configuration:
  - “Multi-peak” mode – 3 Samples / channel / trigger
  - 1 DAQ trigger = 2 APV triggers = 6 Samples / channel / trigger
- Readout
  - Sync pulse every 35 cycles – establishes connection
  - 12 Sample digital header
  - 128 analog channel samples
  - 31 entry output buffer -> Can “stack” up to 5 DAQ triggers

Front End Board – Intro

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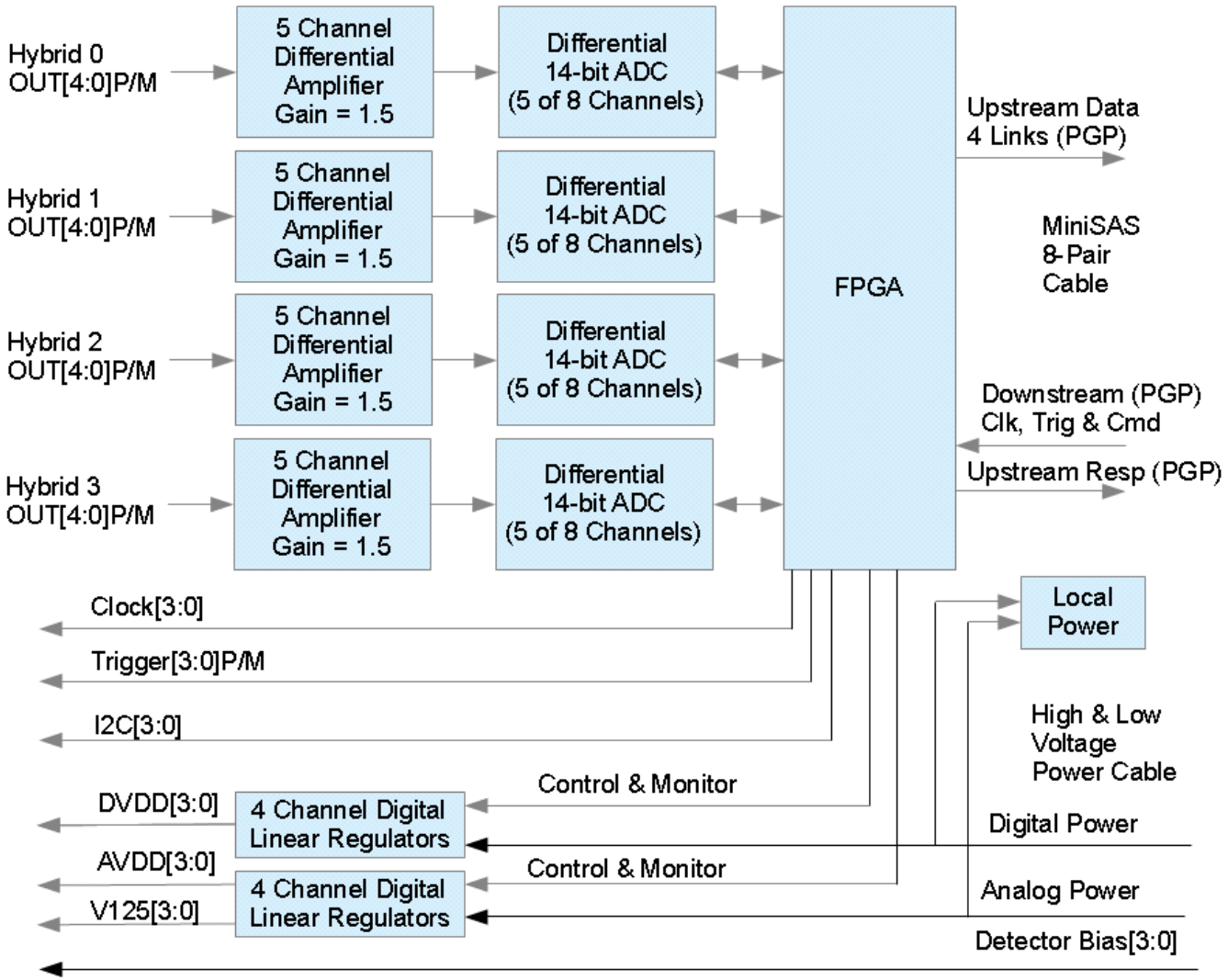
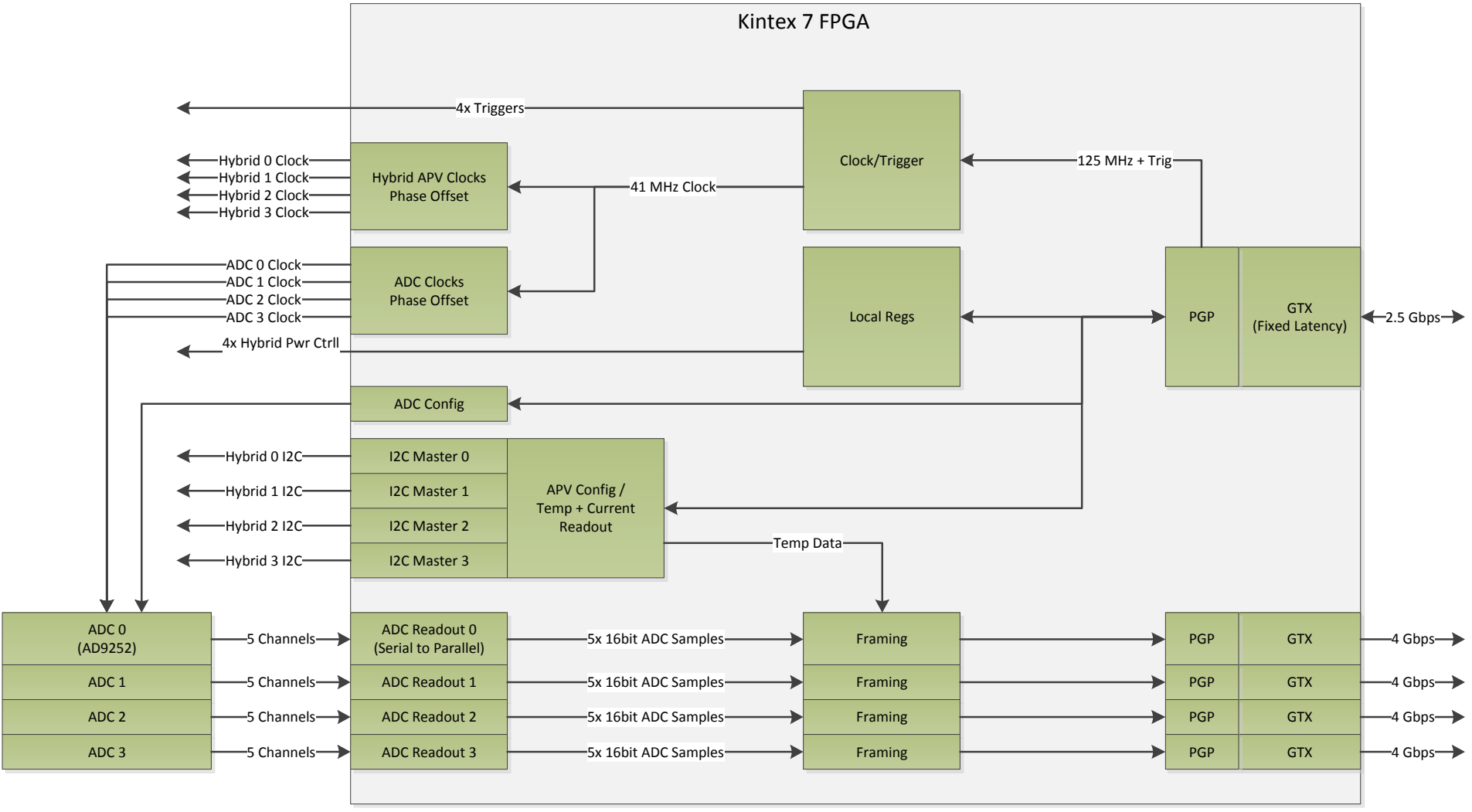
- Purpose:
  - Digitize APV25 outputs
  - Shorten distance between APV25 and ADC
  - APV25 signals & power transported over impedance controlled flex cables
  - Local power conversion, control and monitoring for hybrids
  - Send ADC samples on high speed PGP links to RCE crate
  - Control configuration of APV25 and ADC chips (I2C, SPI)

- Based on Xilinx Kintex 7 FPGA
- 4 Hybrids per Front End Board in back layers
- 3 Hybrids per Front End Board in front layers
- 10 boards total

Front End Board



Front End Board – Firmware



Front End Board – Special Features

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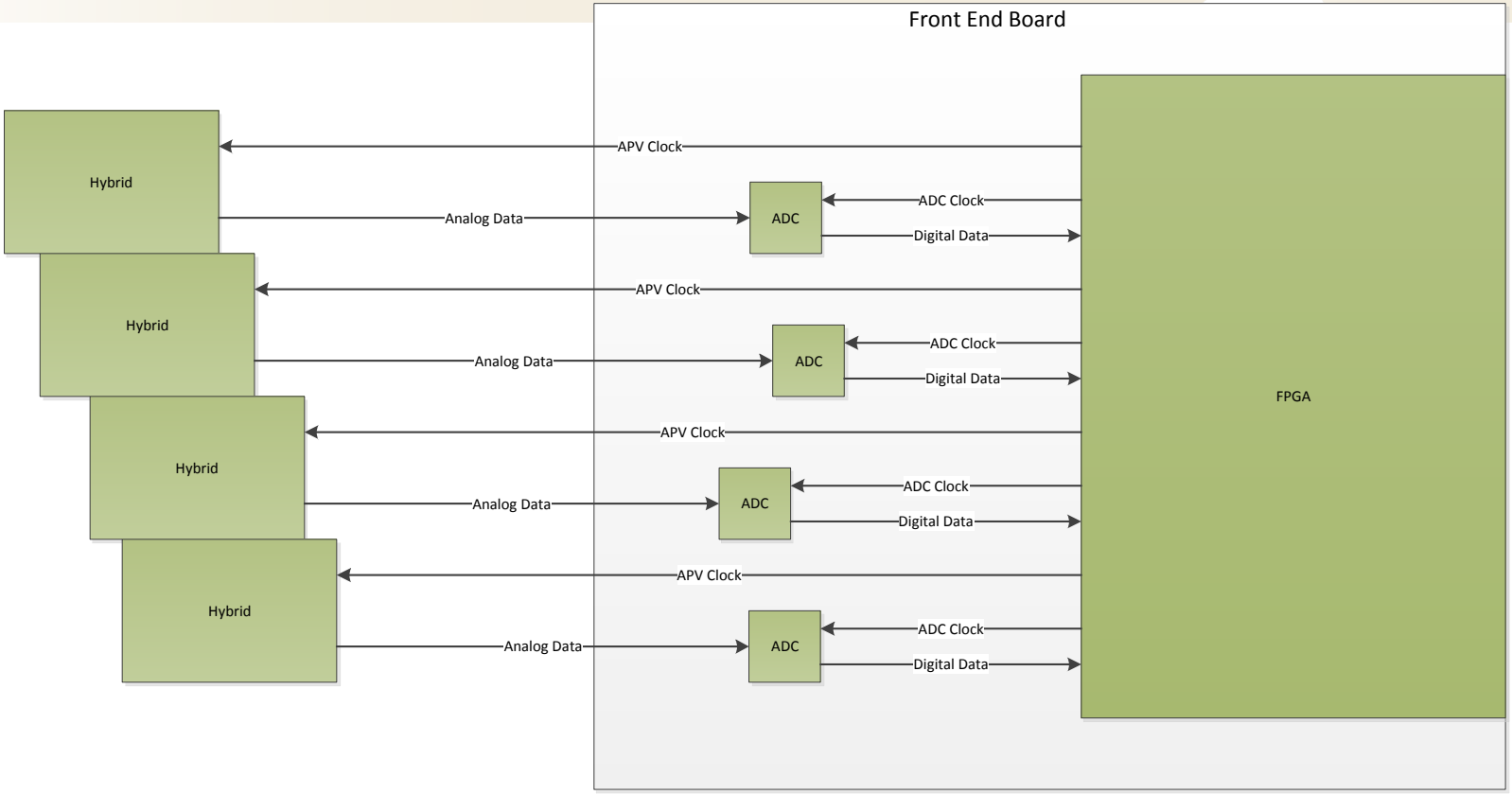
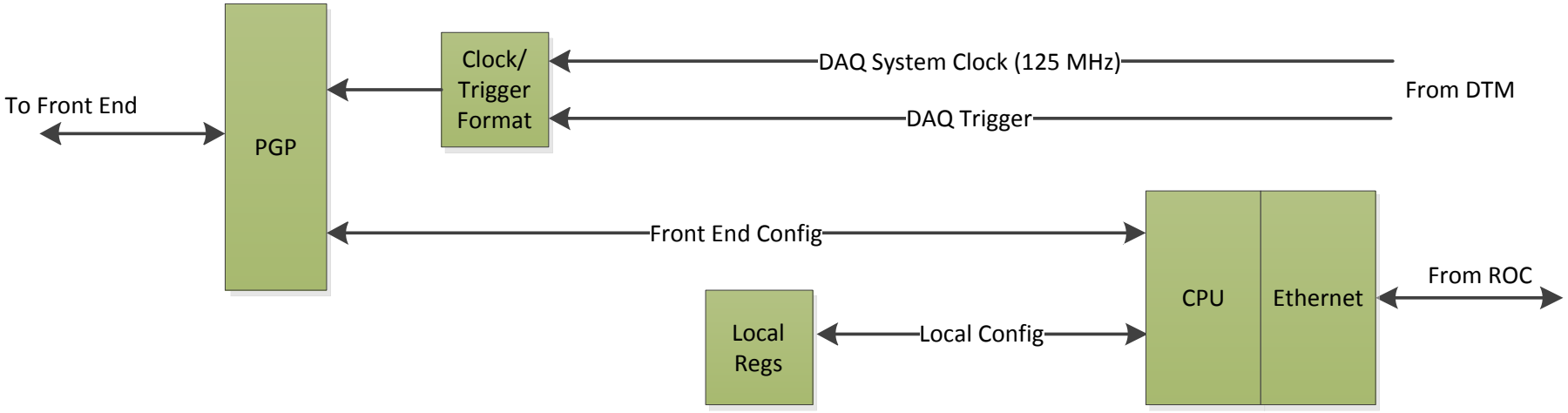
- Clock and Trigger over PGP
  - Create 41 MHz APV clock that is in phase across all FE boards
  - Reduces number of wires through vacuum flange
- Control Power to each Hybrid
- Separate I2C Bus for each attached Hybrid
  - APV Configuration
  - Current + Temp monitoring for each hybrid
  - Temp data inserted into ADC data streams
- Fine phase adjustment of each Hybrid and ADC clock
- Digitized ADC data sent to RCE unmodified
  - All processing happens in RCE crate

Front End Board Firmware – APV/ADC Clock Phase Adjustment



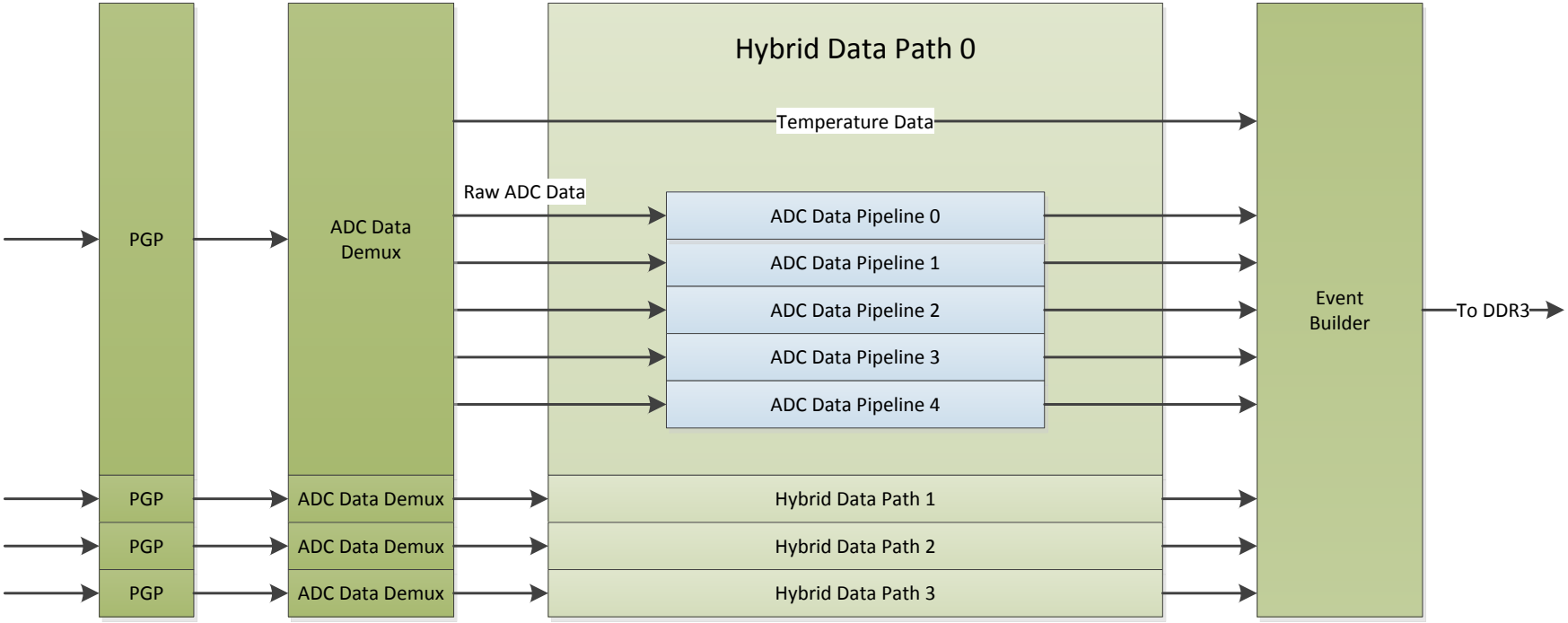
- Compensates for skew due to cable length
  - Every FPGA->Hybrid->ADC->FPGA clock loop different
- In test run could only be applied per FPGA, full range not covered
- Now can phase shift each clock in 150 ps increments over 360º range using Kintex 7 Clock Manager (MMCM)

RCE Data Node Firmware – Clock/Trigger/Config



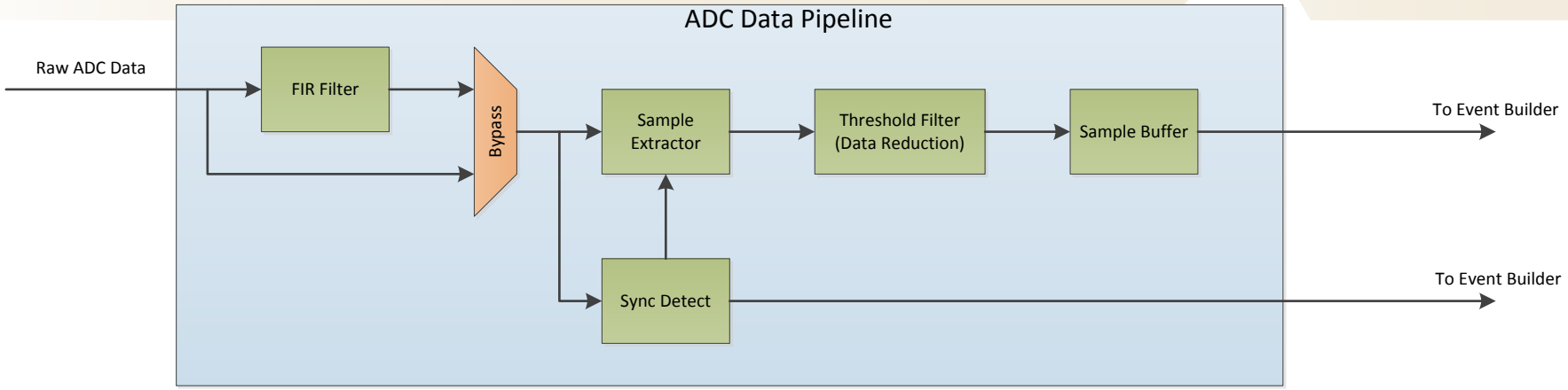
- Each RCE node controls and receives data from 1 Front End board.
  - Or maybe 2.
- Receive local and Front End config from ROC app.
- Pass Front End config down PGP link.
- Pass clock and triggers down PGP link.

RCE Node Firmware – Data Path



- ADC data demuxed from PGP links and sent to data pipelines
- 20 pipelines per RCE node (4 Hybrids x 5 ADC's ea)
- Pipelines process and reduce raw ADC data from each hybrid.
- Event Builder gathers processed and reduced data and writes to DDR3
- Software takes it from there and sends it to ROC app

RCE Node Firmware – Data Pipeline



- FIR Filter
  - Last minute addition in Test Run
  - Filters reflections due to long analog cable runs
  - Shorter analog runs in new setup
  - Filter may not be needed
- Sync Detect
  - Continuously looks for sync pulse from APV25
- Sample Extractor
  - Each trigger produces 6 readout frames from APV25 – Header + 128 channels
  - Processes APV25 frames and groups samples by channel number
- Threshold Filter
  - Threshold compare with per channel constants - three samples over threshold
  - Slope detect: sample 4 > sample 3 or sample 3 > sample 2
- Sample Buffer
  - Stores data to be gathered by Event Builder

- Stacked Triggers
  - APV25 can handle bursts of up to 5 triggers
  - APV Test Run firmware could only handle 1 trigger at a time
  - New firmware will handle trigger bursts

RCE Node Firmware – RAM Bandwidth

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- With no data reduction @ 50 kHz trigger rate:
  - 4 Hybrids – 16.4 Gbps RAM bandwidth needed
  - 3 Hybrids – 12.3 Gbps
  - Zynq platform only supports up to 10 Gbps RAM bandwidth
  - Oversubscribed!?!
- Reality:
  - Low occupancy (<20%) means that most data gets filtered.
  - Can buffer 5 triggers of data in FPGA BRAM to handle bursts.
  - Unlikely to be an issue.
  - Will account for possibility of dropped data just in case.
- Worst case:
  - Can scale up number of RCE Data nodes
  - Less Hybrid data pipelines per RCE node
- No data reduction in calibration mode
  - Will control calibration trigger rate to stay below bandwidth limit.

Current Status

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- New Layer 4-6 Hybrids
  - Schematic capture done
- Front End Board
  - Schematic capture just started
  - New firmware components under development
    - PGP clock recovery and triggering – ongoing
      - Proven on Virtex 5, adapting to 7 Series
    - ADC/APV clock phase delay – done
    - I2C Master – done
  - Other firmware blocks reused from Test Run
- RCE Platform
  - COB – Testing now
  - DTM – Testing now
  - DPM – Will arrive next week