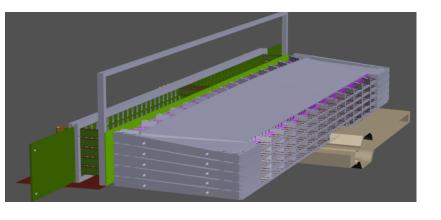
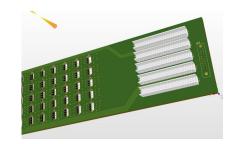
Ecal Mother Boards

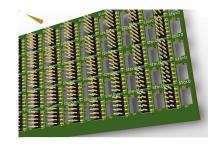
1

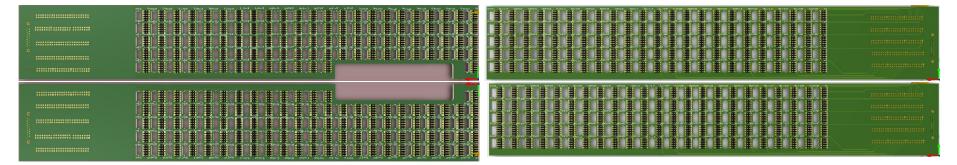
Fabio Pratolongo INFN-GE Italy



ECal Motherboard

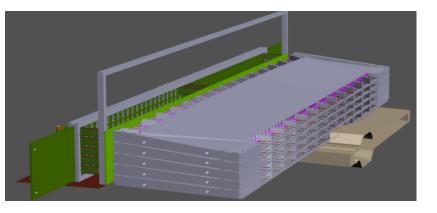




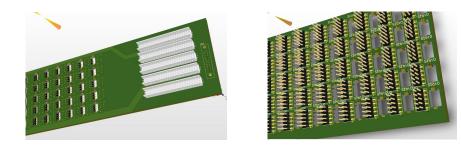


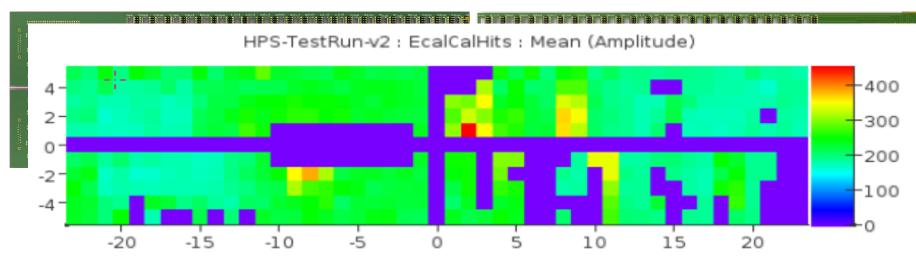
*MB connect preamplifiers and HV from the ECal to crates

*MB extend on Left/Right sides out the vessel to host signal and HV connectors



ECal Motherboard

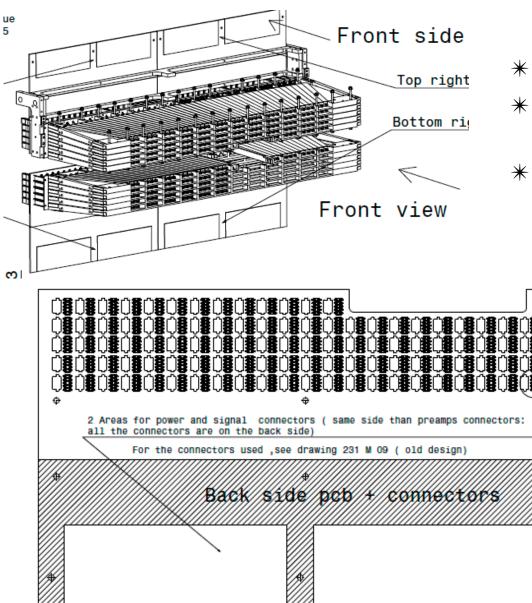




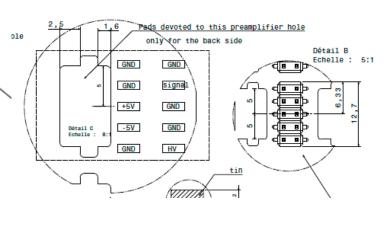
Noise issues with many channels of the motherboards related to design (different trace lengths) and manufacturing

- st New simplified design, keeping the trace length as short as possible
- st Short vertical motherboards with connectors (power and signal) on top/bottom
- * Design solutions taken from IC / FT-CAL experience (IPN-Orsay and INFN-Genova design)

ECal Motherboard Mechanical design



- * Mechanical design: IPN-Orsay
- * Final design after iterations between Genova, Orsay and JLab
- * Mechanics defined: 4 MB (TL, TR, BL, BR)



4

HPS Motherboard Electronic Design

Electrical design: INFN-GE Electronic Service

Design coordinated with JLab (to reuse existing parts: cables, connectors ...)

First step (ORCAD) finished

Last step (ALEGRO) just started

- 4 PCB (115, 115, 106, 106 channels each)
- E.g.:TOP LEFT board (115 chs)
 - •115 SMD connectors (AMP 10 pin, same as used in FT-Cal) for preamps very similar to old MB (pin slightly smaller),
 - 15 TE signal connectors from 16 pin each, same as old MB
 - 2 HV connectors (15 pin) DSUB 750V, 5A, different from old MB for easier routing.
 - I LV connectors (6 pin).
- Same HV grouping (as old MB)
- Same 3M signal signal cable

PCB:

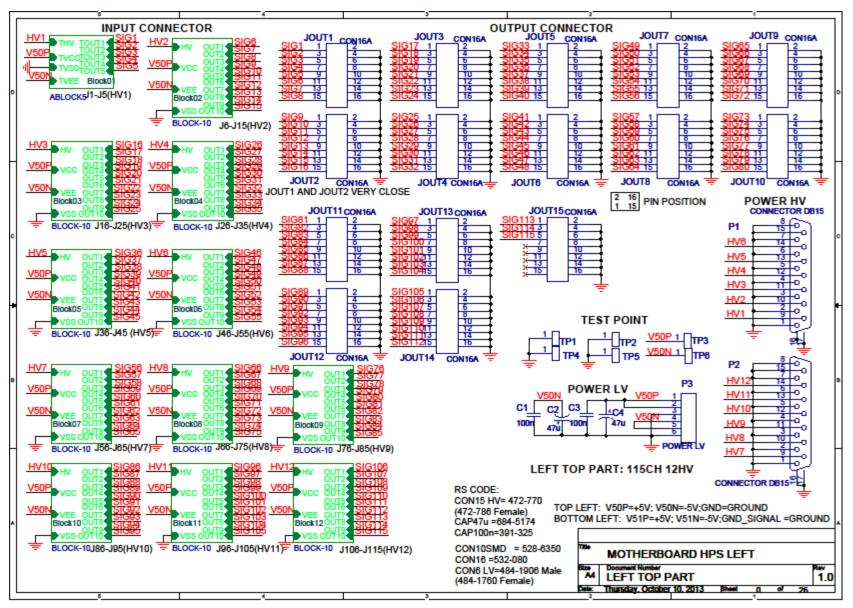
10 layers

3 signals + 1 HV + 1 fan-out + 5 GND

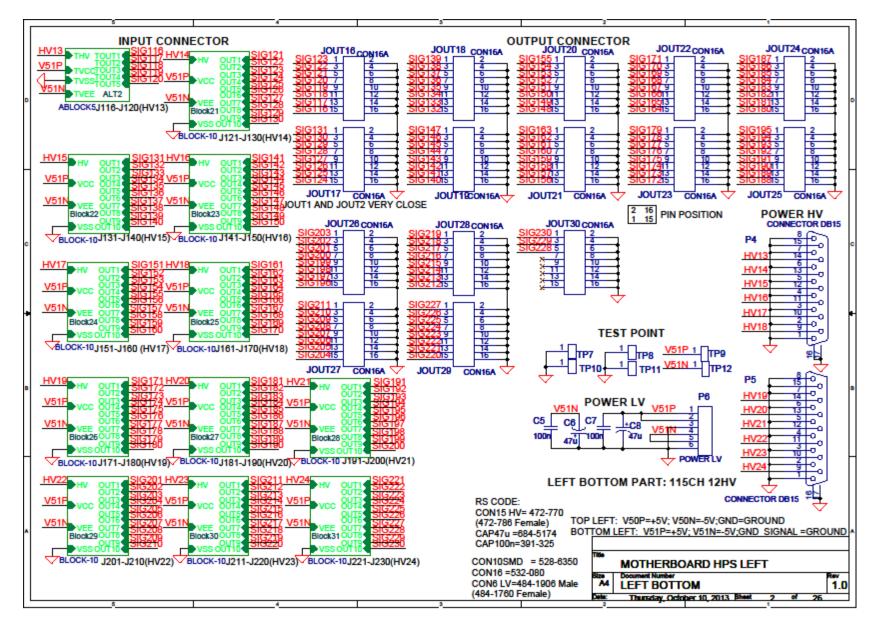
Layout specifications:

I I 5 signal traces with 50 Ohms impedance.Signal: 0.2 mm line width and 0.2 mm min. spacing.HV: 0.6 mm line width and 0.9 mm min. spacing.Ground ring between two signals as FT-Cal project.

LEFT TOP Design (115 channels)



LEFT BOTTOM Design (115 channels)



HV Grouping

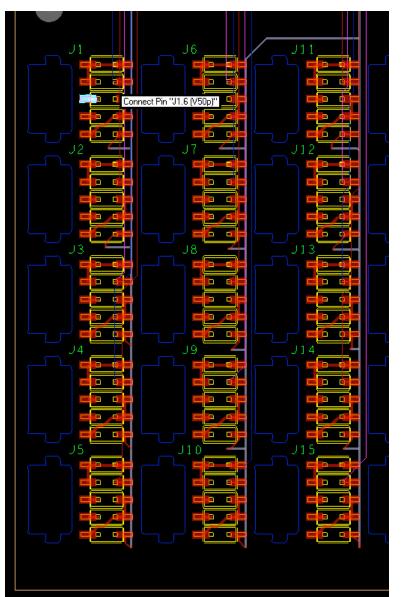
J3 HV1	J8 HV2	J11 HV2 J12 HV2 J13 HV2 J14 HV2	J18 HV3	J23 HV3	J28 HV4	J31 HV4 J32 HV4 J33 HV4 J34 HV4	J38 HV5	J43 HV5	J48 HV6	J53 HV6	J58 HV7	J61 HV7 J62 HV7 J63 HV7	JS8 HW8	J71 HV8 J72 HV8 J73 HV8 J74 HV8	J78 HV9	J83 HV9	J88 HV10	J91 HV10 J92 HV10 J93 HV10		J101 HV11 J102 HV11 J103 HV11 J104 HV11	J106 HV12 J107 HV12 J108 HV12 J109 HV12	J112 HV12 J113 HV12
J5 HV1	J10 HV2	J15 HV2	J20 HV3	J25 HV3	J30 HV4	J35 HV4	J40 HV5	J45 HV5	J50 HV6				J70 HV8	J75 HV8	J80 HV9					J105 HV11	J110 HV12	
NEW TOP AFT (the same as previus project)																						
J1 HV1 J2 HV1 J3 HV1 J4 HV1 J5 HV1	J9 HV2		J19 HV3	J23 HV3 J24 HV3		J33 HV4 J34 HV4	J36 HV5 J37 HV5 J38 HV5 J39 HV5 J40 HV5	142 HV5 43 HV5 J44 HV5	J48 HV6 J47 HV6 J48 HV6 J49 HV6 J50 HV6	J52 HV6 J53 HV6 J54 HV6	J57 HV7 J58 HV7 J59 HV7	J63 HV7 J64 HV7	J67 HV8 J68 HV8 J69 HV8	J71 HV8 J72 HV8 J73 HV8 J74 HV8 J75 HV8	J78 HV9 J79 HV9	J81 HV9 J82 HV9 J83 HV9 J84 HV9 J85 HV9	J86 HV10 J87 HV10 J88 HV10 J89 HV10 J90 HV10	J91 HV10 J92 HV10 J93 HV10 J94 HV10 J95 HV10	J96 HV11 J97 HV11 J98 HV11 J99 HV11 J100 HV11	J101 HV11 J102 HV11 J103 HV11 J104 HV11 J105 HV11	J106 HV12 J107 HV12 J108 HV12 J109 HV12 J110 HV12	J112 HV12 J113 HV12 J114 HV12
									OLD TOP					06 input co	nnectors 1	2 HV nets	HV25 to HV	/36				
									8 groups o	of 10, 2 grou	ups of 9, 1 g	roup of 6 ar	nd 1 group o	of 2								
J3 HV25 J4 HV25	J8 HV25 J9 HV25	J12 HV26	J17 HV26 J18 HV26 J19 HV26	J23 HV27 J24 HV27		J34 HV28	J39 HV28	J44 HV29	J47 HV29 J48 HV29 J49 HV29	J52 HV30 J53 HV30 J54 HV30	J56 HV30 J57 HV30 J58 HV30 J59 HV30 J60 HV30	J62 HV31 J63 HV31 J64 HV31	J66 HV31 J67 HV31 J68 HV31 J69 HV31	J70 HV32 J71 HV32 J72 HV32 J73 HV32	J74 HV32 J75 HV32 J76 HV32 J77 HV32	J78 HV32 J79 HV33 J80 HV33 J81 HV33	J82 HV36 J83 HV33 J84 HV34 J85 HV34	J86 HV36 J87 HV33 J88 HV34 J89 HV35	J90 HV36 J91 HV33 J92 HV34 J93 HV35	J94 HV36 J95 HV33 J96 HV34 J97 HV34	J100 HV33 J101 HV33	J102 HV36 J103 HV36 J104 HV36 J105 HV36 J106 HV36
NEW TOP RIGHT (a vertile bit different) 6 groups of 10, a group of 11, 1 group of 8, 1 group of 6 and 1 group of 3																						
J3 HV25	J8 HV25 J9 HV25	J11 HV26 J12 HV26 J13 HV26 J14 HV26 J15 HV26	J18 HV26 J19 HV26	J22 HV27 J23 HV27 J24 HV27	J28 HV27	J34 HV28	J38 HV28 J39 HV28	J43 HV29	J47 HV29 J48 HV29 J49 HV29	J52 HV30 J53 HV30 J54 HV30	J56 HV30 J57 HV30 J58 HV30 J59 HV30	J62 HV31 J63 HV31 J64 HV31	J68 HV31	J70 HV32 J71 HV32 J72 HV32 J73 HV32	J75 HV32 J76 HV32	J79 HV33 J80 HV33	J84 HV33	J88 HV34	J90 HV35 J91 HV35 J92 HV35 J93 HV35	J94 HV36 J95 HV36 J96 HV35 J97 HV35	J98 HV36 J99 HV36 J100 HV36 J101 HV36	

- Old: hits-load well distributed
- New: simple trace routing
- We are working to find a compromise

LEFT TOP Routing (preliminary)

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Routing Zoom on 3 columns



HPS Motherboard WorkPlan

- Mechanical Specifications with Orsay
 - Design of LEFT TOP and LEFT BOTTOM boards
 - Layout routing of LEFT TOP and LEFT BOTTOM boards in progress
 - Design of RIGHT TOP and RIGHT BOTTOM boards with the correct HV grouping
 November
 - Layout routing of RIGHT TOP and RIGHT BOTTOM boards.
 December
 - Board Productions and Assembly (with the same company serving the FT-Cal).
 12k euro
 January 2014
 - Test on Electrical connections and Full crosstalk test with FT-Cal crystals
 3k euro
 February 2014

Done!

Done!