SVT Testing Update

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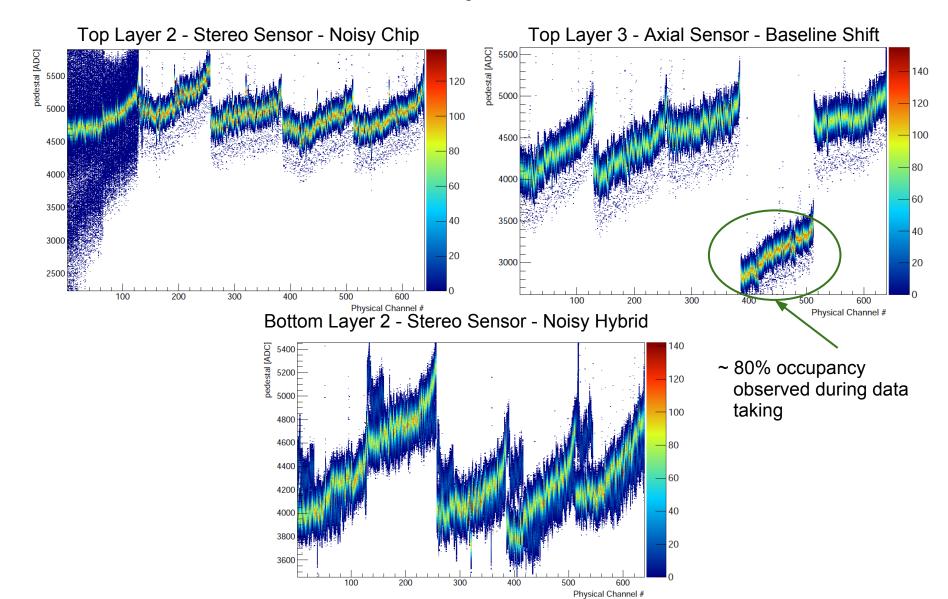
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August 9, 2013 Heavy Photon Search DAQ Meeting

Sensors With Issues During Test Run

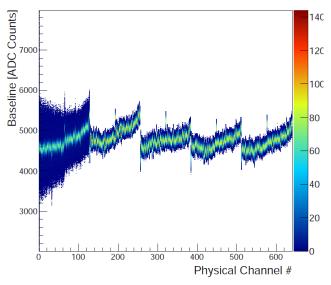
Three sensors were found to have issues during the test run



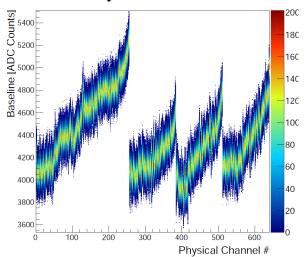
Revisiting the Sensors

Only the noisy chip on the top layer has been reproducible

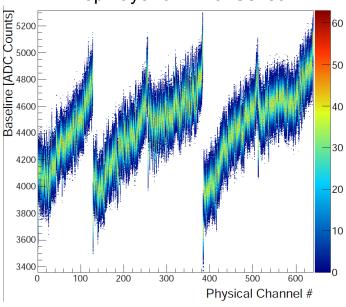
Top Layer 2 - Stereo Sensor - Noisy Chip



Bottom Layer 2 - Stereo Sensor



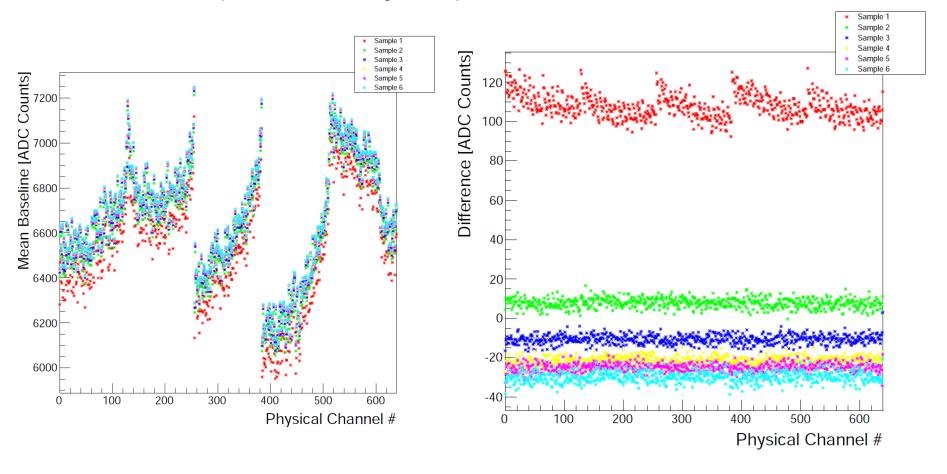
Top Layer 3 - Axial Sensor



- Was the baseline shift caused by a misconfigured chip we didn't catch?
- Was the noisy sensor caused by faulty grounding, the "black box" or a faulty DPM?

Sample to Sample Shifts

- Baseline sample 1 of FPGA 5, Hybrid 1 in the current setup has an abnormally large shift as compared to the other samples
 - Typical shifts are observed to range from 10-20 ADC counts
- The behavior is present when testing both top and bottom SVT volumes



Sample to Sample Shifts

- The shifts are causing tails to show up in the pedestal distributions
- Individual samples are as expected
- Noise looks fine but the Shaper signal shape is a bit strange and has a lower amplitude than expected

