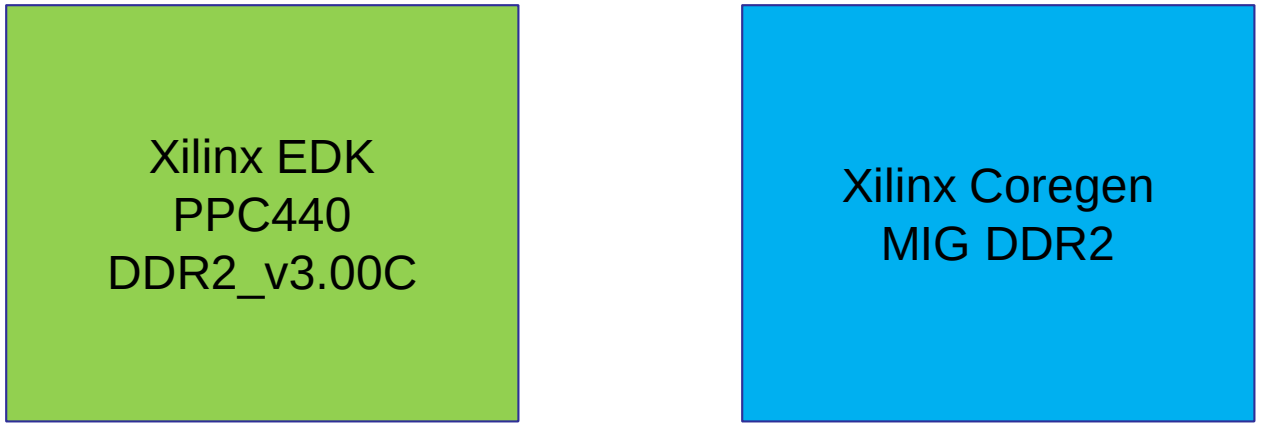
DDR2 vs DDR3

- Only minor differences
  - Lower signal voltage – 1.5V vs 1.8V
  - Different mode registers
  - Different initialization procedure

Xilinx DDR Controllers

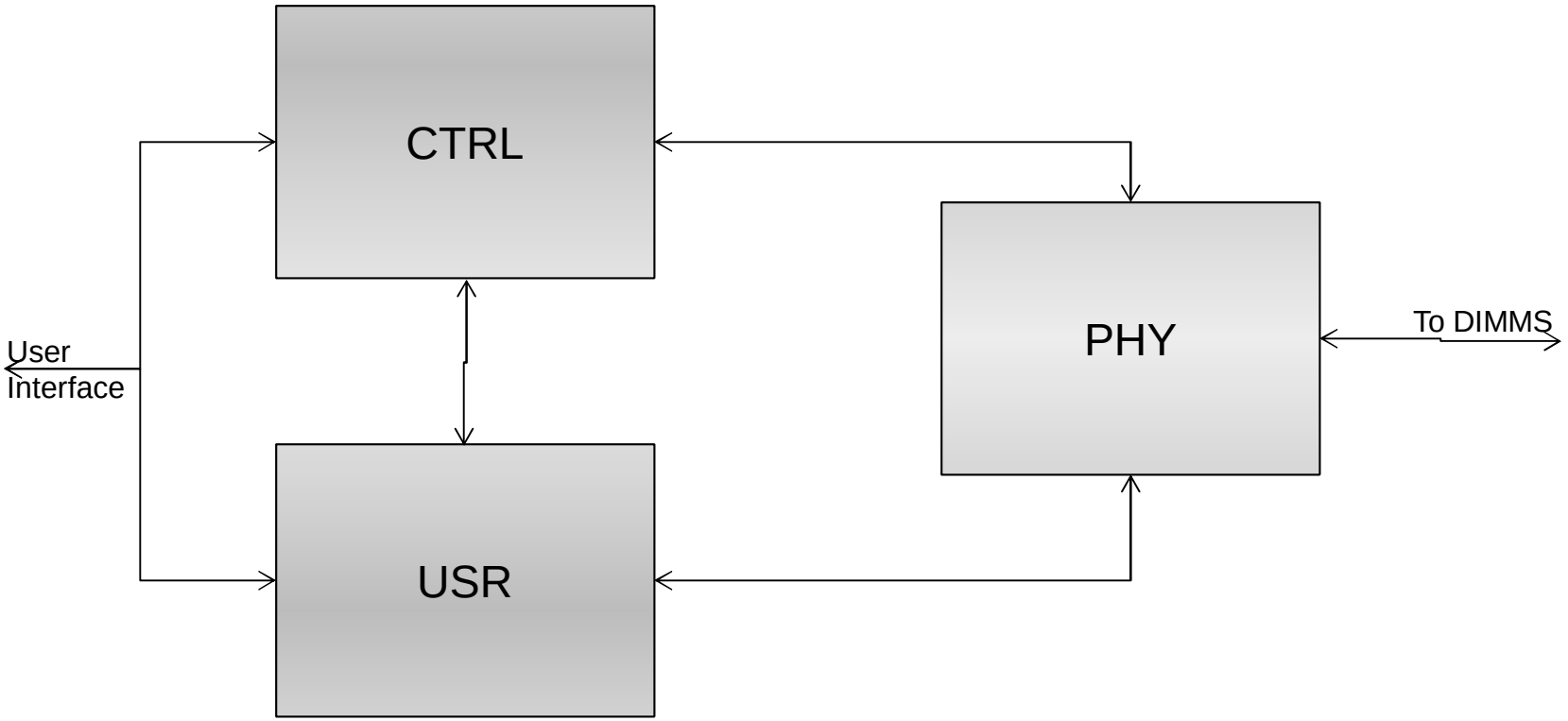
Two base DDR controllers



Both have support for DDR3 already baked in.

Enabled through Verilog parameters.

DDR Controller Structure



USR
- FIFOs for Data
- Read data alignment

CTRL
- Autorefresh
- Memory commands
- Address generation
- Bank management
- RAS, CAS, WE, CS

PHY
- IO Primatives
- Initialization
- Read timing calibration
- All DDR3 specific stuff here

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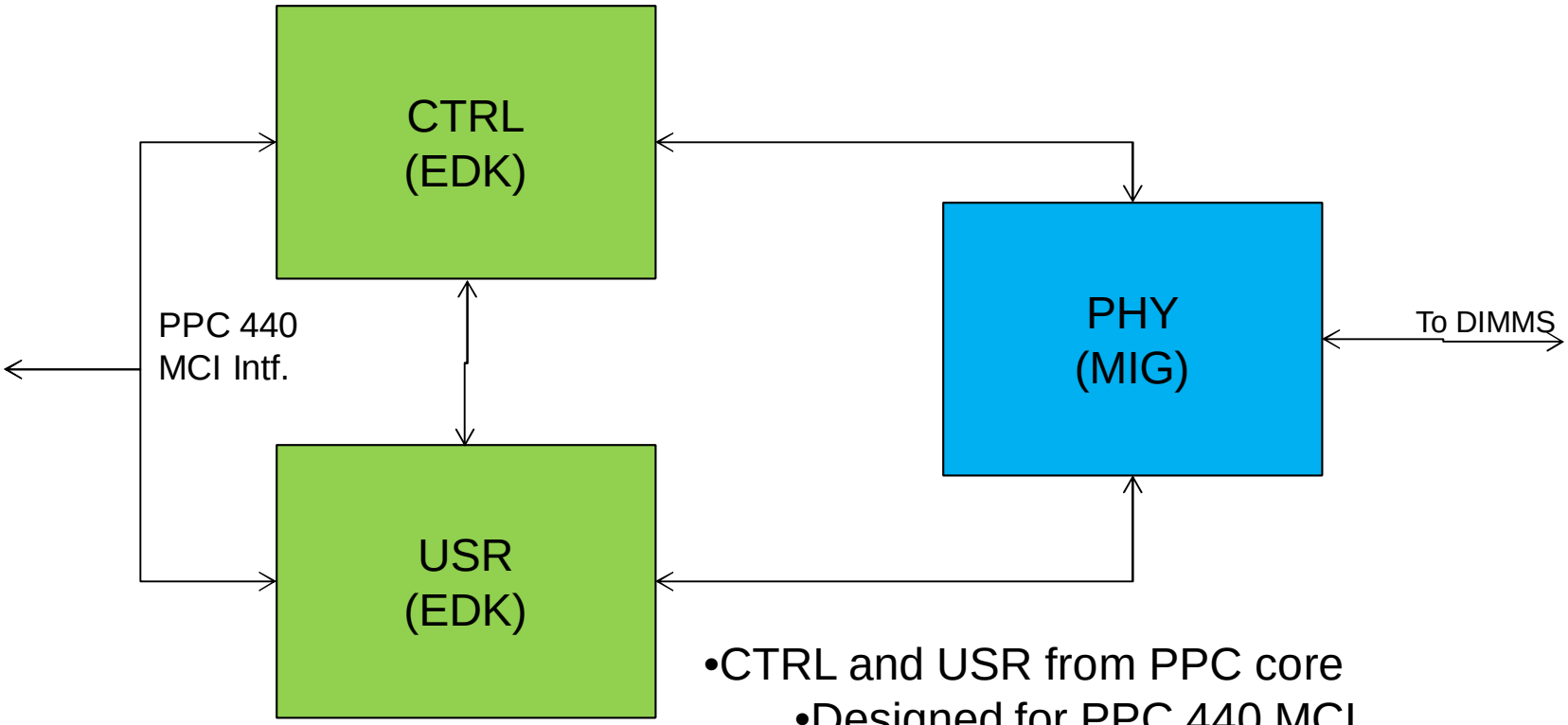
COB DPM DDR3 Controller



- CTRL and USR from PPC core
  - Designed for PPC 440 MCI
  - CTRL slightly modified to support 2T timing

- PHY from MIG
  - Newer, better calibration procedure
  - IDDR instead of ISERDES in Read data path
  - Drop in replacement for PPC 440 PHY

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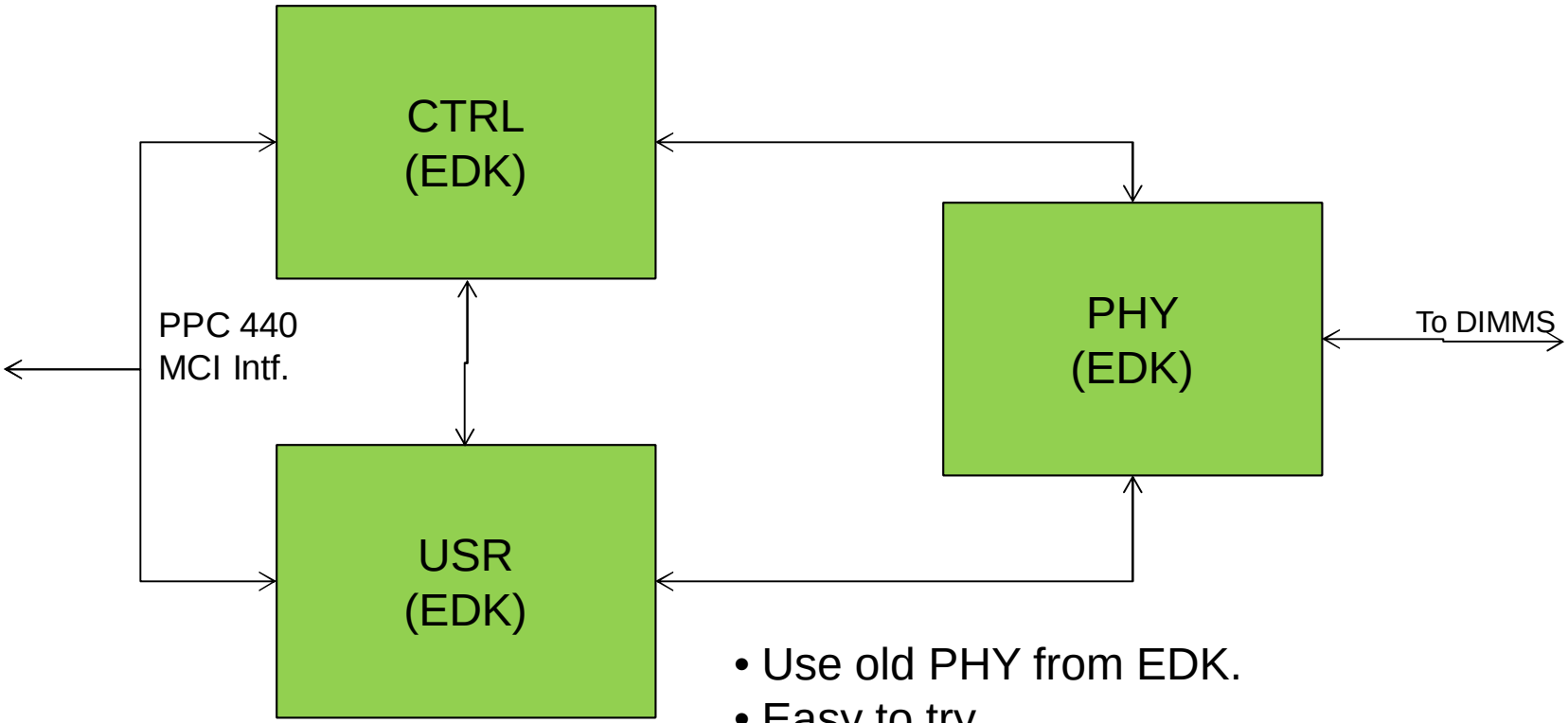
Issues

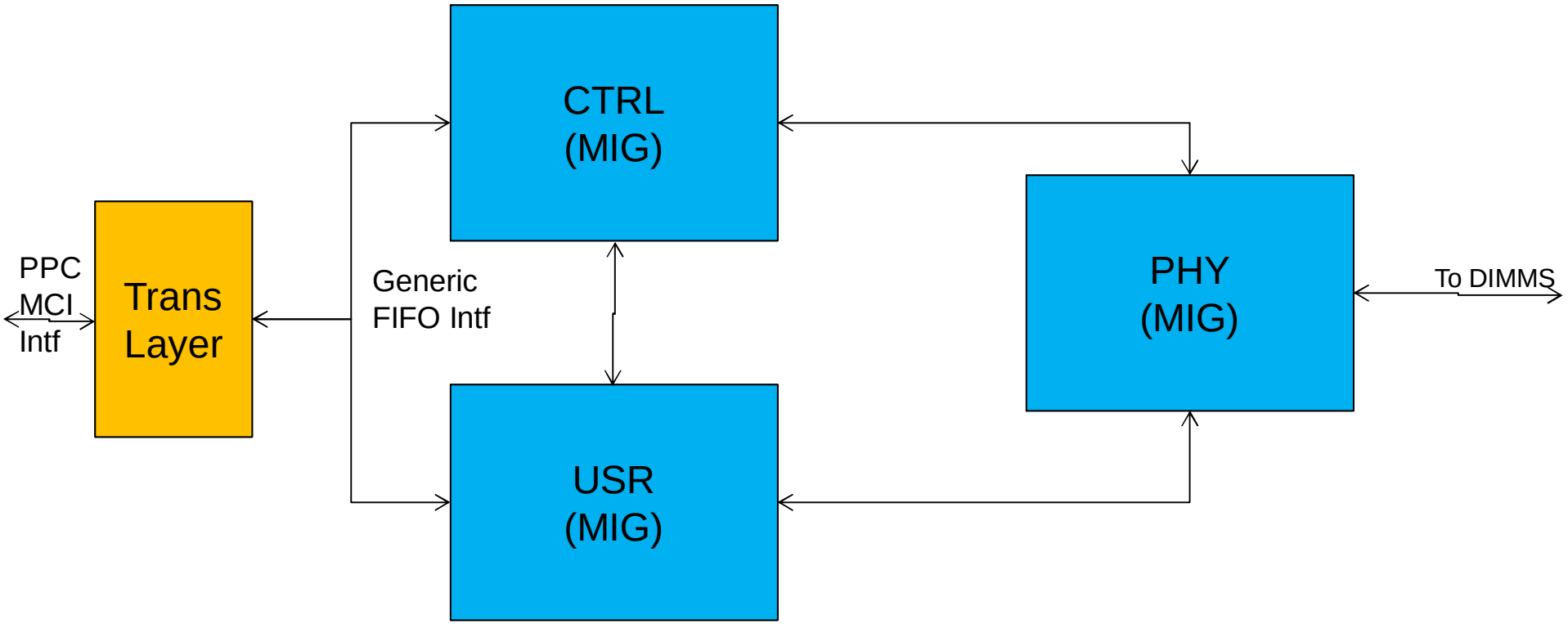
- Bank management
  - Can’t be disabled
- Timing
  - Narrowly met at 312 MHz
- Code quality
  - Ctrl.v is a house of cards.
  - Many unused signals.

Option: All EDK



- Use old PHY from EDK.
- Easy to try.

Option: All MIG + Translation



- Might not be easy to implement
- Would be less efficient
  - More resources
  - Higher latency
- Would rule out MIG PHY as source of issues if it worked

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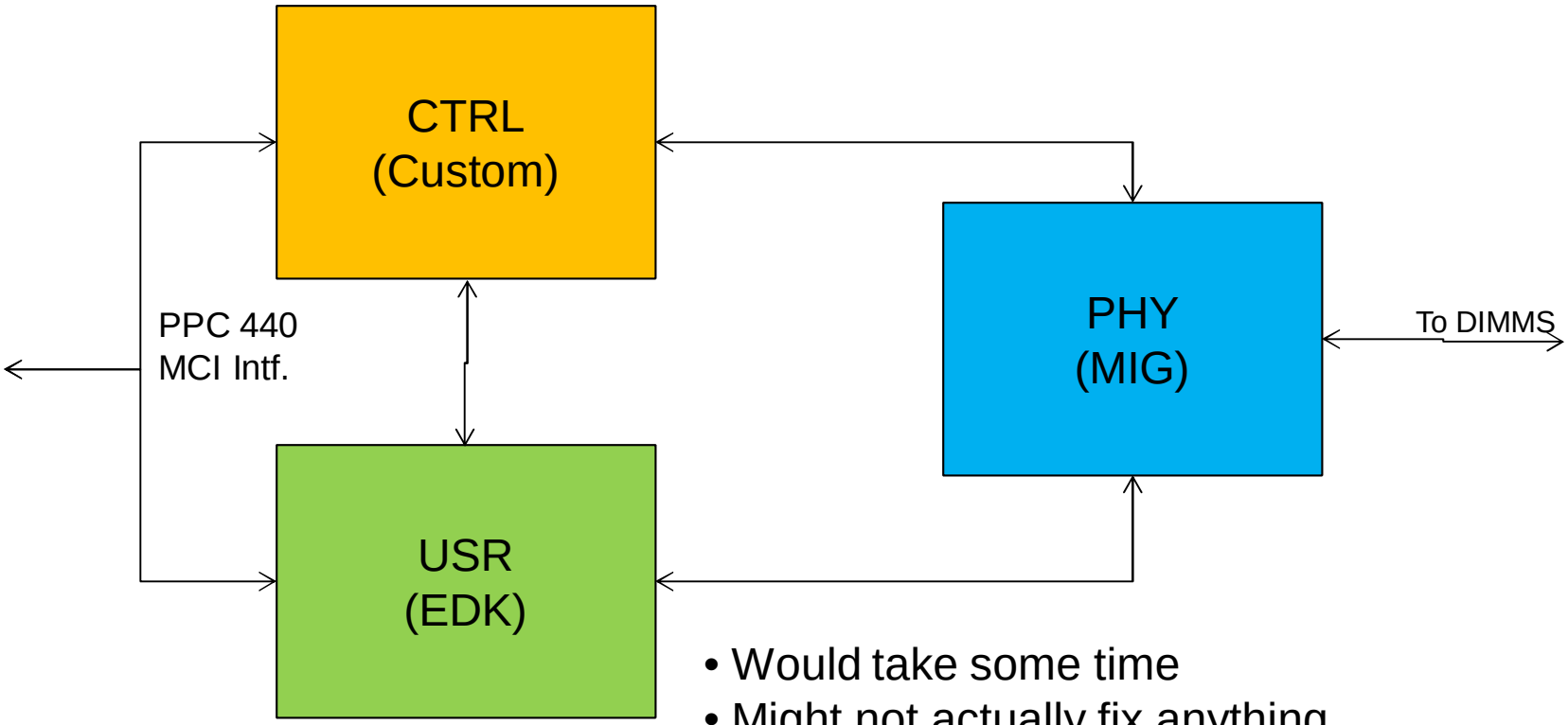
Option: Rewrite CTRL



- Would take some time
- Might not actually fix anything.