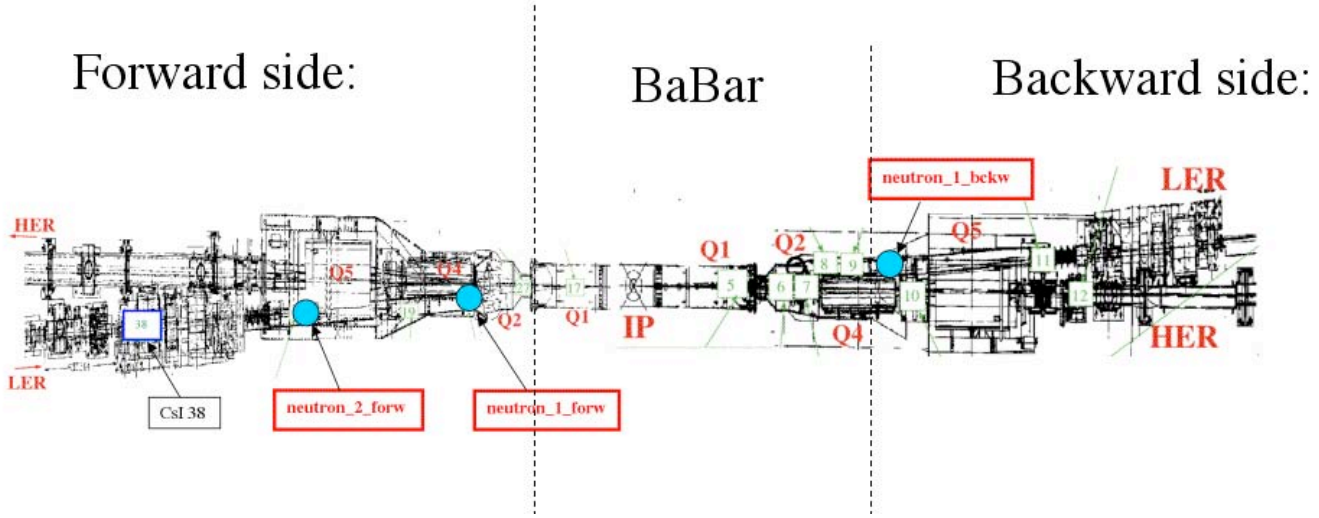
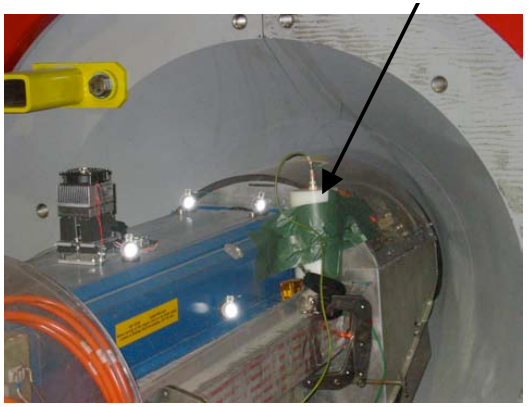
BaBar/HPS Neutron Background

Pelle, Jerry, Ben, Ryan

Babar Experience

- Neutron source from radiative Bhabha scattering striking flange
- Confidence from low neutron rate with HER or LER only in ring
- No residual activity
- Three neutron detectors installed



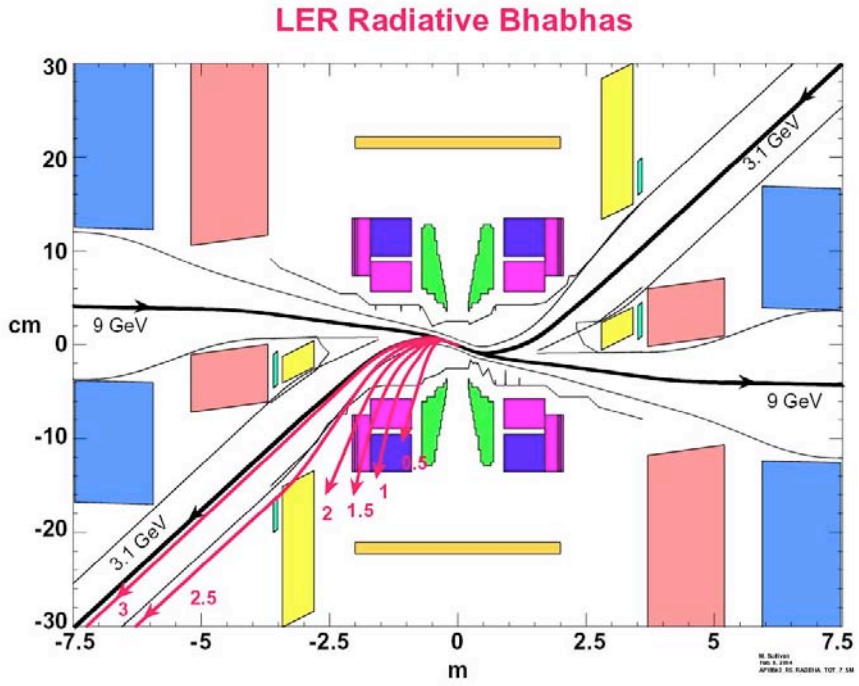


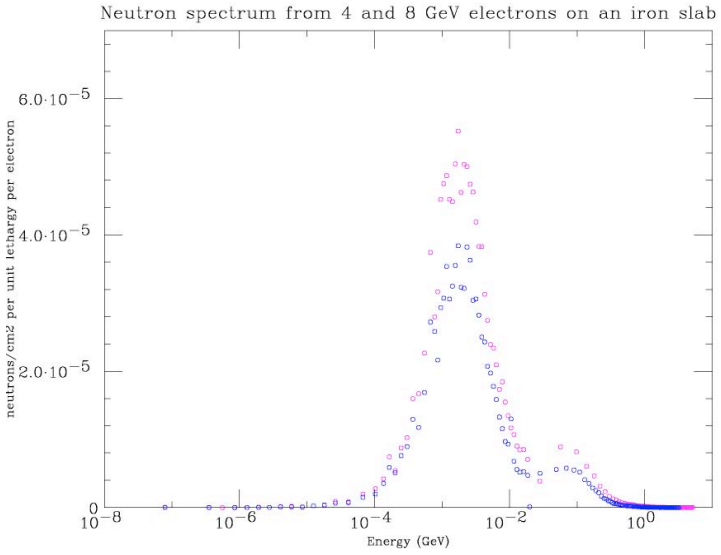
Babar Experience

Two sources from Bhabha scattering hitting flanges (backward side only below)
Backward side more important (lower energy)?

Energy spectrum from FLUKA simulation:
4-8GeV electrons hitting FE slab
Gives ~1 MeV neutrons
Negligible thermal neutrons in Babar (measure without Polyethylene)

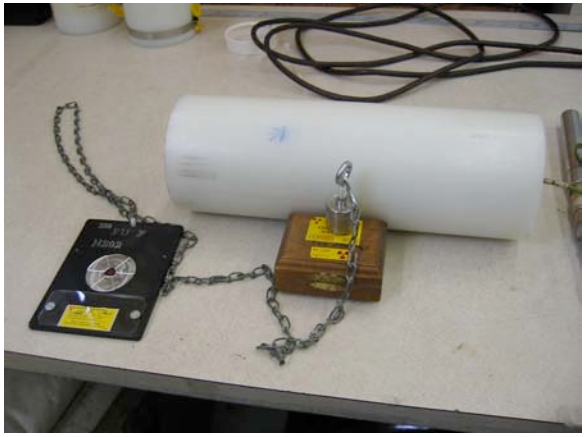
Backward direction:





Neutron Detectors

- BF3 gas proportional counters
  - B(n,α)Li dominant reaction, large cross-section for En<100eV
  - Wrapped in 2” polyethylene to moderate neutrons
  - Calibrate with Pu238-F neutron source: 1.5MeV neutrons (close to expected neutron spectrum)

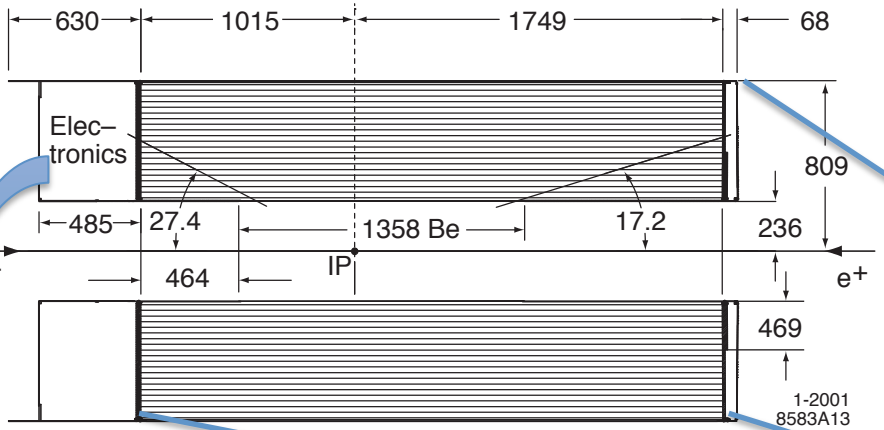


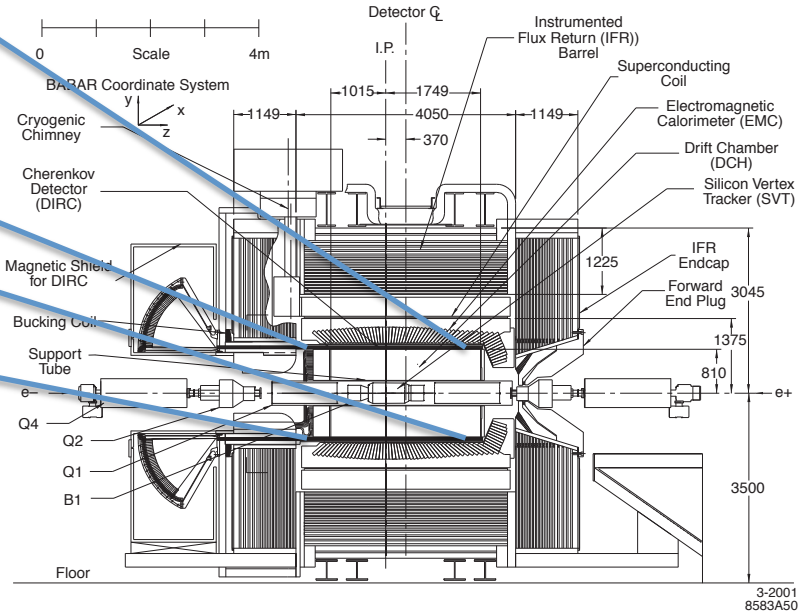
90% efficient for thermal neutrons (~0.02eV)
Few percent for 100eV neutrons

Measured detection efficiency ~2-3% (with Polyethylene)

Drift Chamber Electronics

FPGAs in radiation area….can we learn anything?





Drift Chamber Electronics
48 FPGAs (arranged in quadrants of the wire chamber)

Source Location And Fluxes

- Use simulation and neutron counters to identify **single main** (ignore 2nd source in calculation) source
- Extract neutron background environment from source location and intensity
  - Assume point source and 4pi emission

Neutron detector	
Distance from source:	240cm
Incident rate	6.38e5 Hz
Flux	2.2e3 Hz/cm2

DCH electronics	
Distance from source:	~250cm
Flux	~2.0e3 Hz/cm2

FPGA Failure Rates

Two definitions

1. Standard FPGA soft error rate measure is FIT

FIT: # Failures per 10^9 hours (sea level neutron flux)

=>FIT/Mb: FIT per 10^6 bits (configuration or RAM)

2. Neutron cross-section per bit

Measured with irradiation ~1-100MeV neutrons at LANL (~40k feet spectrum)

Measured per bit (configuration or RAM)

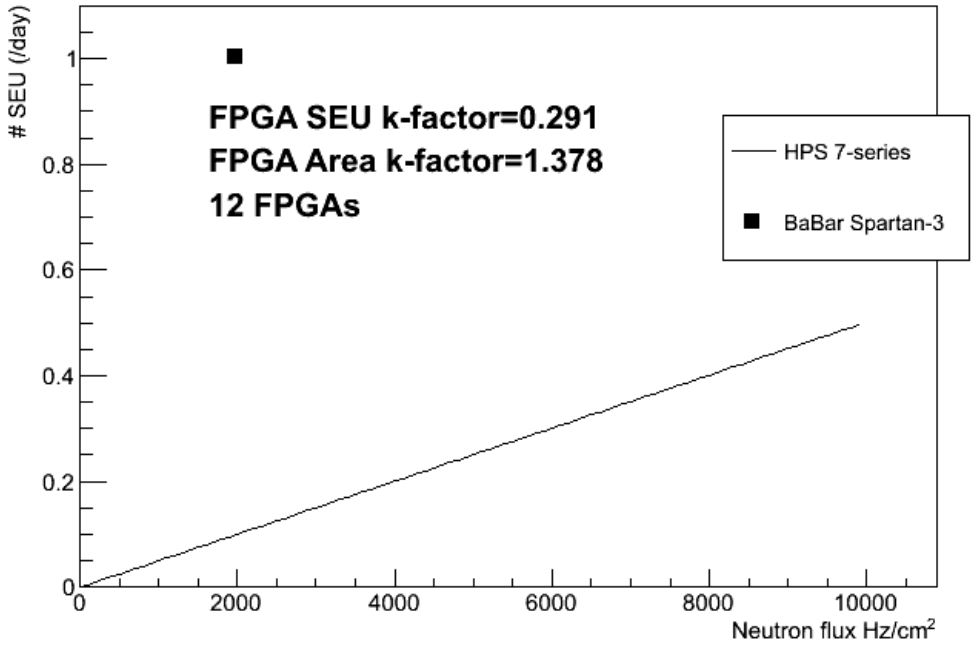
Experiment	FPGA type	Footprint	Neutron cross-section per Bit	FIT/Mb	# configuration bits (used/max)
BaBar	Xilinx Spartan 3, 90nm (XC3S1500)	23x23mm	2.40×10^{-14} (3.48×10^{-14})	190 (173)	2M/5.2M
HPS (?)	Xilinx 5 series, 65 nm (XC5VFX30T)	27x27	6.7×10^{-15} (3.96×10^{-15})	165 (692)	2M/9.7M
HPS (?)	Xilinx 7 series, 28nm (XC7A100T)	27x27	6.99×10^{-15} (6.32×10^{-15})	79 (31)	2M/?M

FPGA for HPS has ~70% lower neutron cross-section (and x2.4 better FIT)

Assuming same area, neutron flux and configuration bits: expect ~22% SEU rate

Failure Rate Predictions for HPS

Experiment	FPGA type	# FPGAs	Neutron cross-section per Bit	FPGA footprint	SEU/day
BaBar	Xilinx Spartan 3, 90nm (XC3S1500)	48	2.40×10^{-14} (3.48×10^{-14})	23x23mm	1
HPS(?)	Xilinx 5 series, 65nm	12	6.7×10^{-15} (3.96×10^{-15})	27x26mm	<<1
HPS(?)	Xilinx 7 series, 28nm	12	6.99×10^{-15} (6.32×10^{-15})	27x27mm	<<1



Takes into account:
- Footprint
- SEU susceptibility

Assumes
- Same nr of configuration/RAM memory blocks
- Same neutron flux profile

Uncertainty: all in all factor of 2-3?

Conclusion so far:
- hard to make this a huge problem?
- Mitigate with detection mechanisms