Half-module testing to do list

- To start, go back to basics i.e. extract noise, pedestal, t_0, gain ... but this time with a T_p of 35 ns.
  - This will require changing the APV25 operating points such that we are able to achieve a 35 ns shaping time. How close can we get to a T_p of 35 ns?
- In order to extract the correct gain and offset error, the amount of charge that is actually being injected by the APV25 calibration circuitry needs to be established
  - When the nominal APV25 operating points are being set, TrackerGUI indicates that the calibration circuitry is injecting 18,125 electrons rather than 25,000 electrons (nominal value) There is strong reasons (MIP plot) to believe that the value being displayed by TrackerGUI is wrong
  - This will skew the offset error when extracting the channel gains
- Half-modules need to be tested at cold temperatures
  - How cold do we want to run at?
  - How much does power consumption increase by?
  - How does noise, response gain, etc. change?
  - What are the new APV25 operating points that will allow us to achieve a 35 ns shaping time.
- Why do we have high noise at the APV25 chip edges (Mark Raymond believes he knows the answer but it was never tested)? Can we do anything about? Do we care to do anything about it? This is something we can live with so it's not crucial ...
- During the previous QA session, some pedestal distributions were observed to have double peaks.
  - Were the double peaks caused by reflections or are the pedestals shifting?
- Do the pedestal shift over time?
- Try running at a higher clock time (50 MHz).
  - How do all APV25 characteristics change?

Full DAQ Testing

- Again, go back to basics i.e. extract noise, pedestal, t_0, gain ... but this time with a T_p of 35 ns.
  - Are we able to achieve a 35 ns shaping time with the full DAQ
- Why causes some APV25 chips to become out of sync?
  - This seemed to almost always occur when a new run was started ... why?
- Top Layer 5, Top Layer 4 and Top Layer 10 all had noisy APV25 chips.
  - Are the APV25 chips the problem? Did the pedestals shift?
  - Establish whether a half-module needs to be replaced.
- Bottom Layer 3 seems to have several problems. Can we fix it? The operating currents were higher than those observed for all other half-modules which might indicate a problem with the hybrid.
- Every 32nd channel on all APV25's have a double peak structure which is likely caused by reflections
  - The FIR filter needs some tweaking