

Test Run SVT Calibrations Overview

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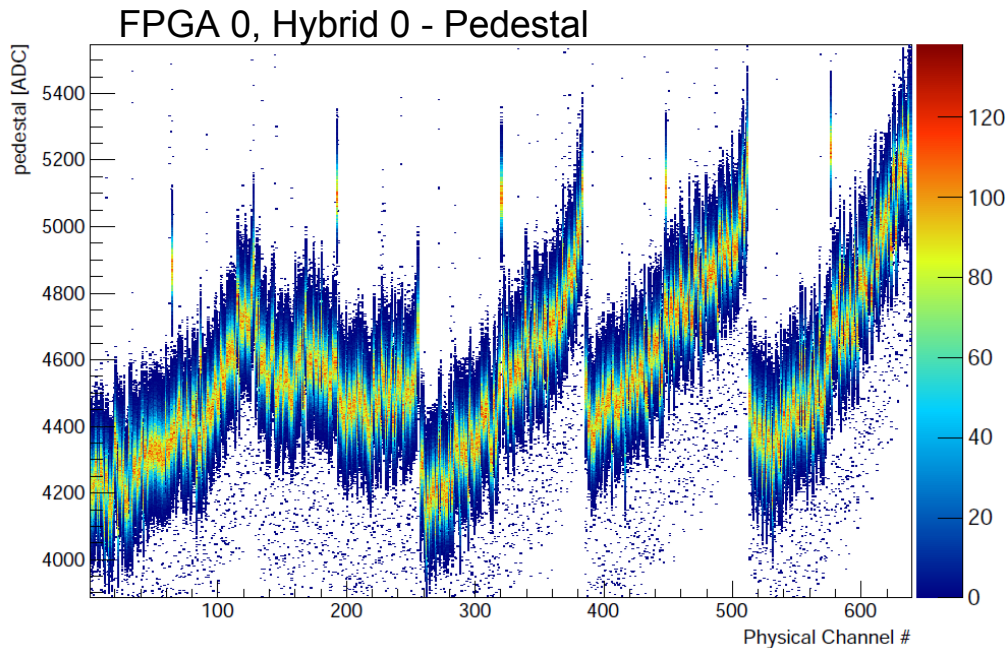
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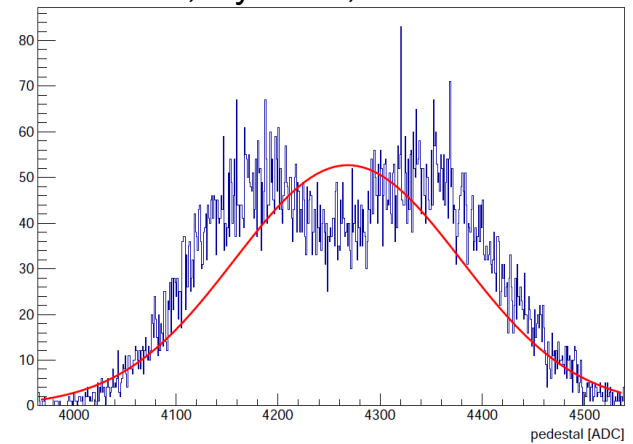
Heavy Photon SVT Meeting

Pedestals

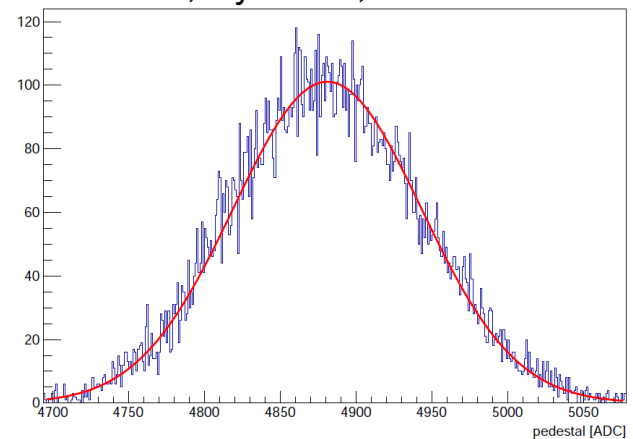
- The pedestals for most sensors looked as expected and were found to be in the range of 4000 - 5500 ADC counts
- The pedestals for some channels have tails associated with them while other channels were exhibiting signs of reflections



FPGA 0, Hybrid 0, Ch32 - Pedestal



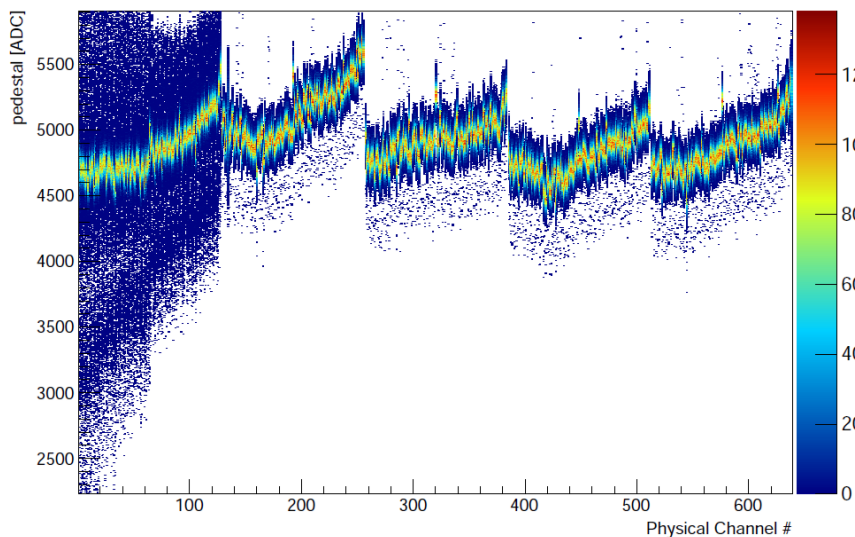
FPGA 0, Hybrid 0, 64- Pedestal



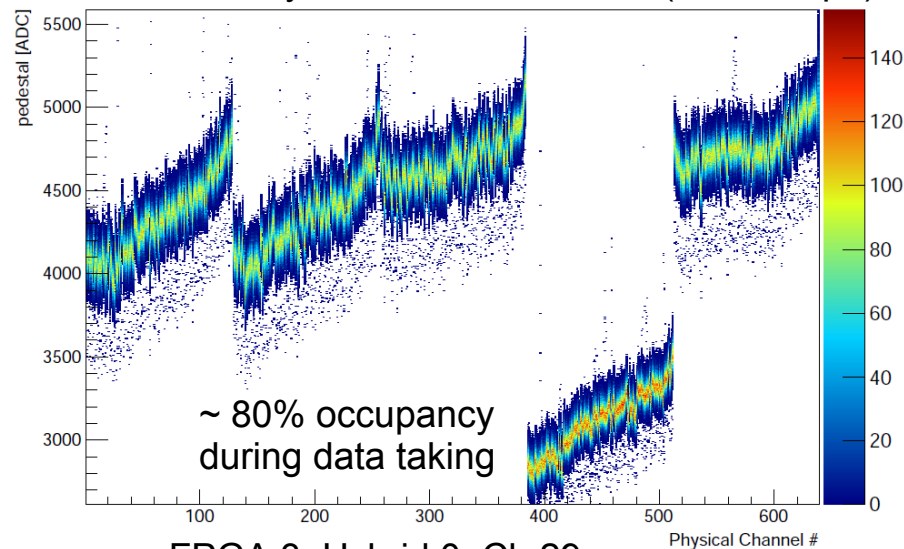
Troubled Sensors

- There were three sensors which showed issues during QA

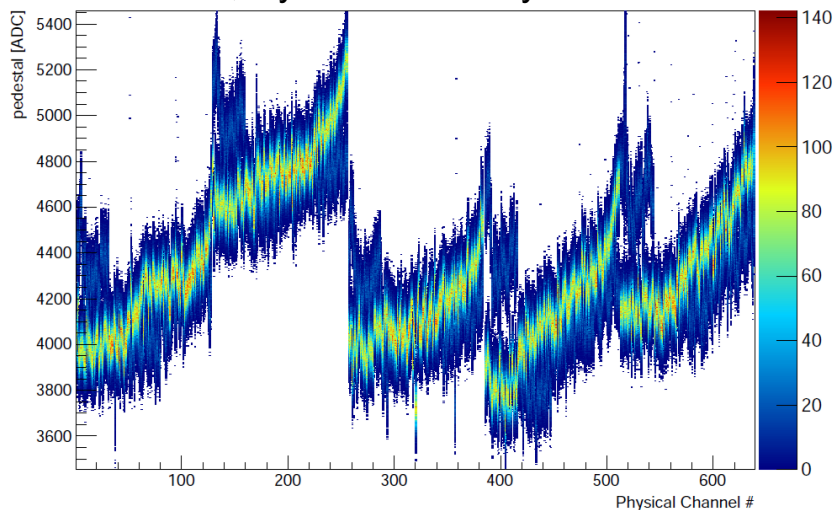
FPGA 0, Hybrid 2 - Noisy chip



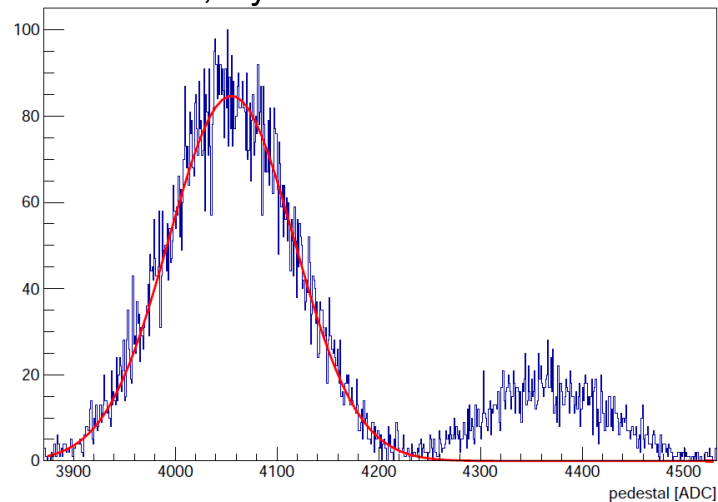
FPGA 1, Hybrid 2 - Baseline shift (Dead chip?)



FPGA 3, Hybrid 0 - Bad hybrid?

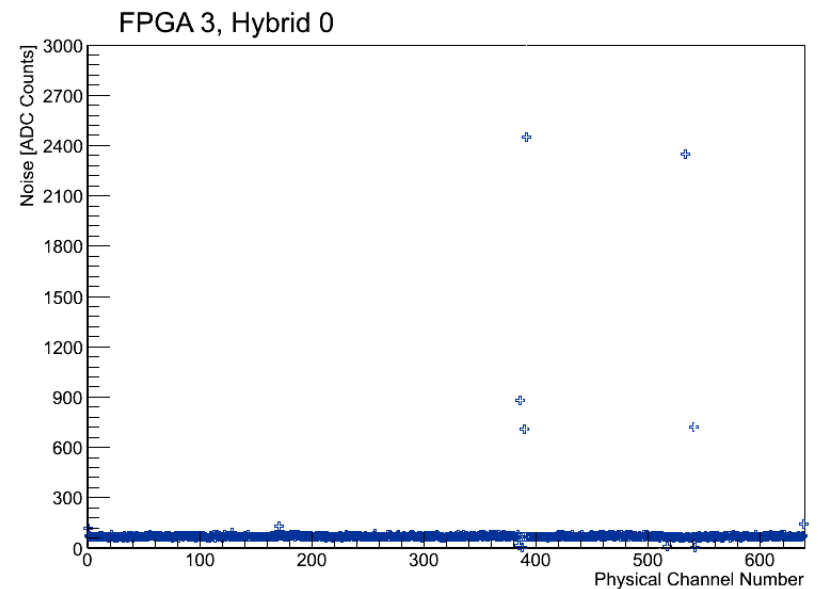
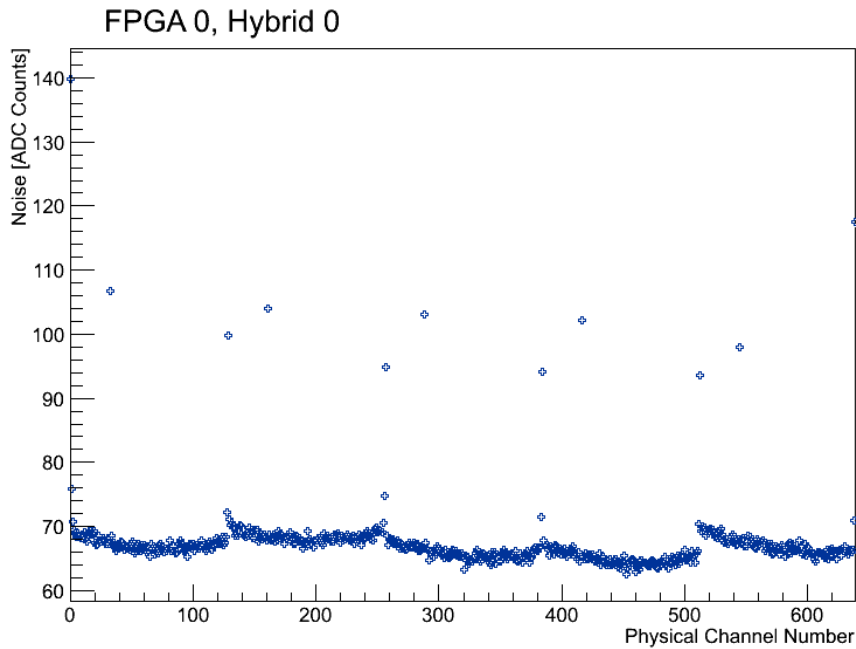


FPGA 3, Hybrid 0. Ch 29



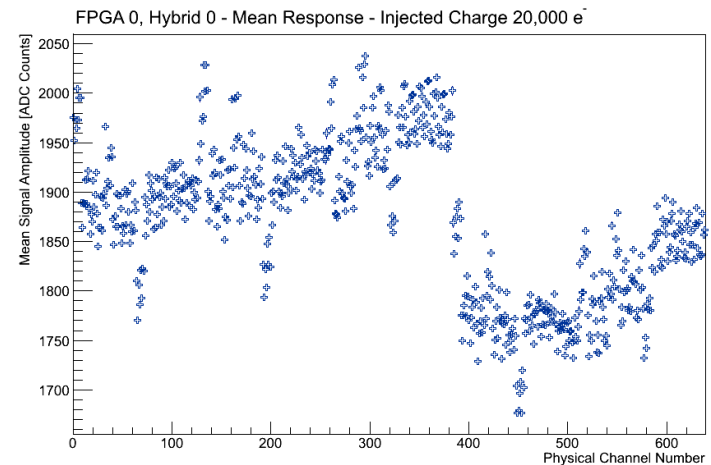
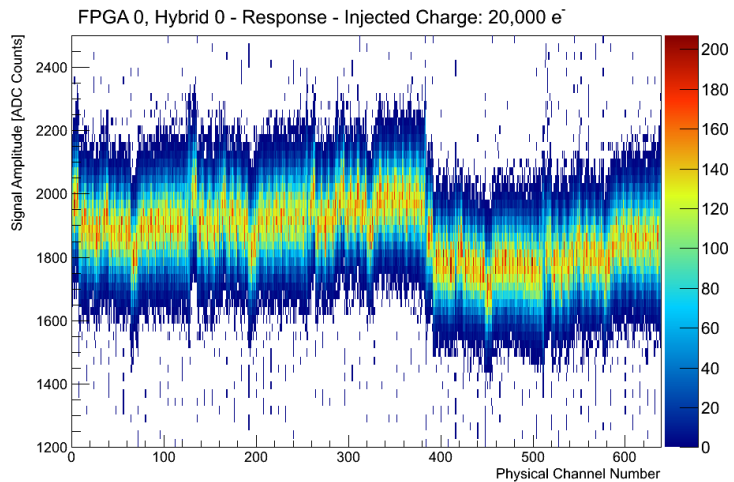
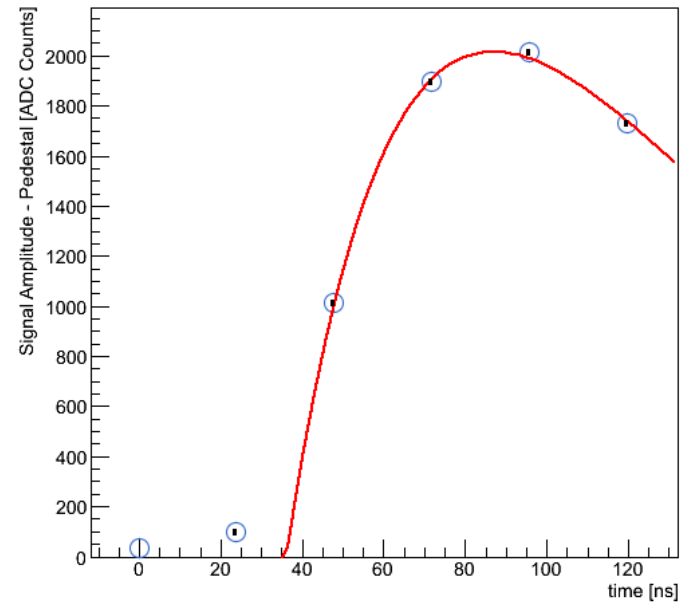
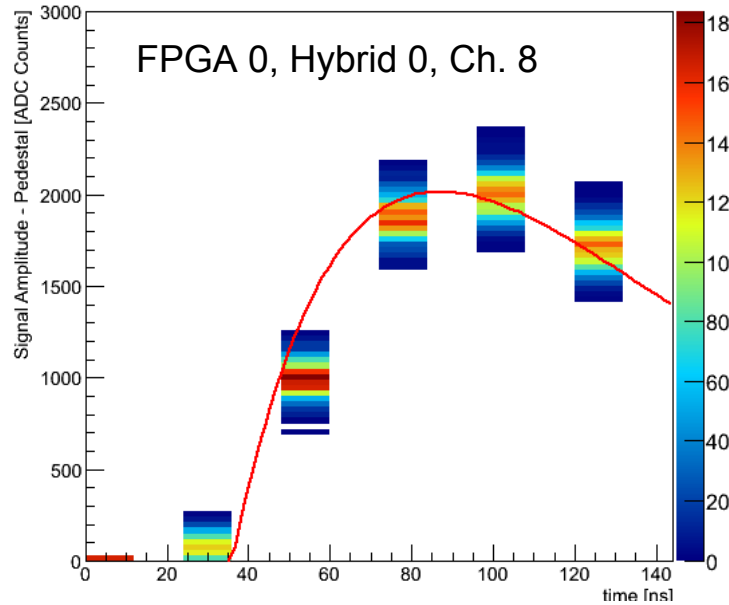
Noise

- The noise throughout most sensors ranged from ~65 to 70 ADC Counts
- As was observed during QA, channels at the chips edges are noisier by up to ~50%

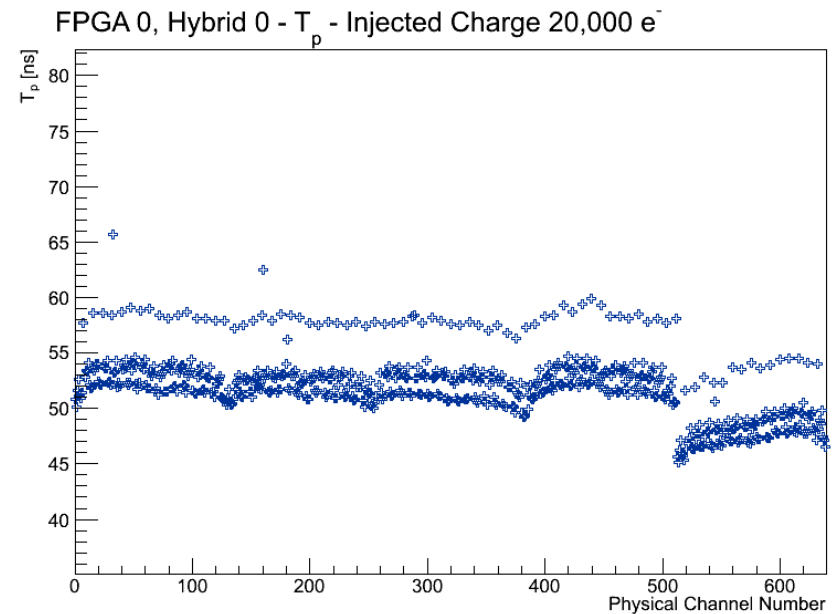
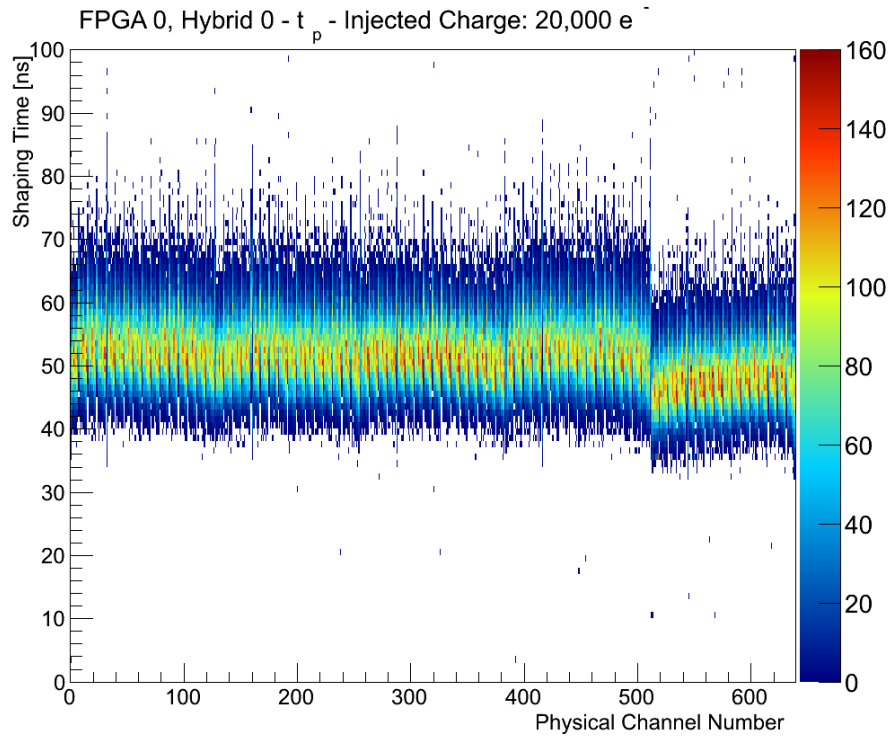


Response

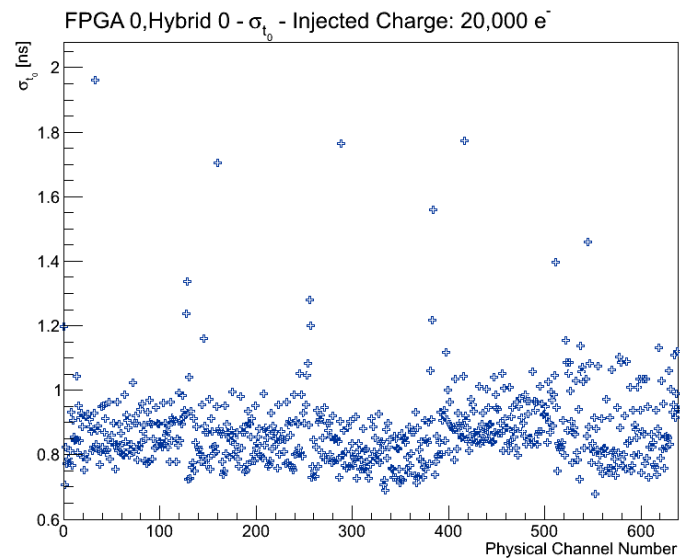
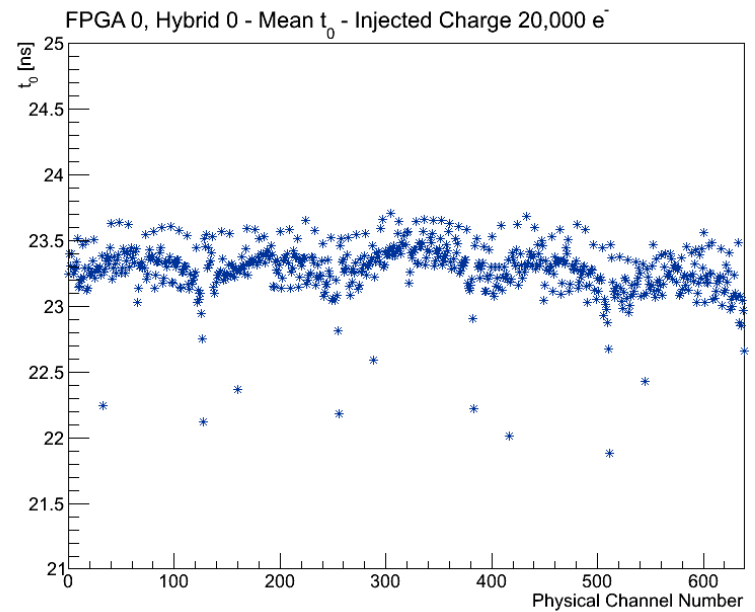
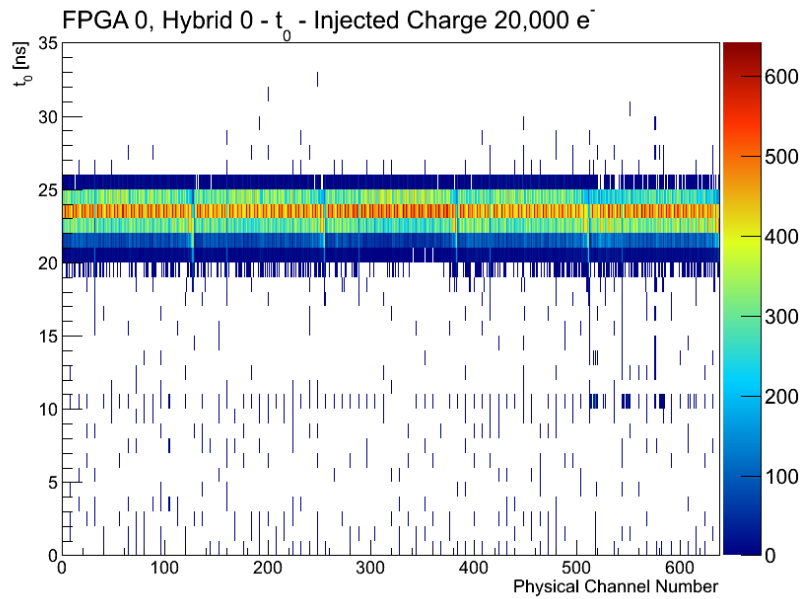
- The response at a given charge was extracted by fitting the six samples to a CR-RC shape



Shaping Time - T_p



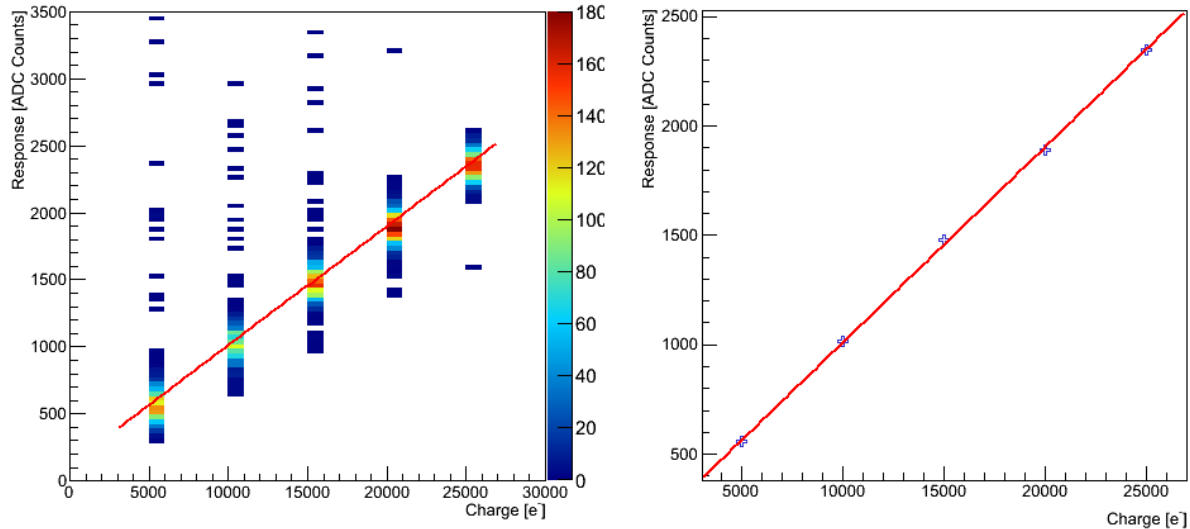
Hit Time - t_0



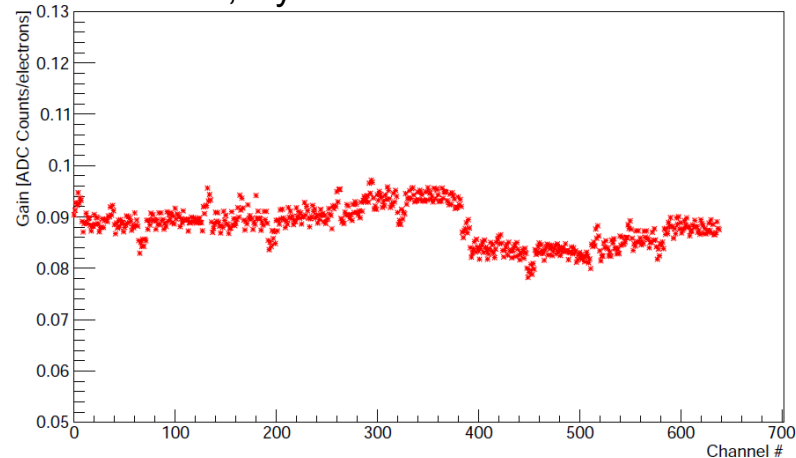
Gain

- The gain and offset error were extracted by linearly fitting the signal response to charges ranging from 5,000 e⁻ to 25,000 e⁻

FPGA 0, Hybrid 0, Ch. 8



FPGA 0, Hybrid 0



Cluster Charge

- The resulting Landau distribution of the cluster charge has a peak at $\sim 15,000 e^-$ which is much lower than expected ($\sim 22,000 e^-$ to $24,000 e^-$)
- If the charge scale is adjusted such that $18,125 e^- = 25,000 e^-$ the peak is at $\sim 26,000 e^-$, closer to the expected value ... this needs to be studied further

