Firmware

Building firmware

ISE

- howto-compile-firmware.txt
- `reseng` method

Vivado

- XAPP890 - Zynq All Programmable SoC Sobel Filter Implementation Using the Vivado HLS Tool

Configuration

- ug470 - 7 Series FPGAs Configuration User Guide

Partitions and partial reconfiguration

1. Partial Reconfiguration in the ISE Design Suite
2. UG702 - Partial Reconfiguration User Guide
    a. NB, this says "Partial Reconfiguration is not currently supported in the Vivado Design Suite."
    b. This comment is apparently out of date; xapp1159 implies that Vivado **can** be used:
3. UG909 - Vivado Desgin Suite User Guide: Partial Reconfiguration
4. UG743 - Partial Reconfiguration Tutorial: PlanAhead Design Tool
5. UG744 - Partial Reconfiguration of a Processor Peripheral Tutorial
6. Zynq 7000 Partial Reconfiguration Reference Design
7. xapp1159 - Partial Reconfiguration of a Hardware Accelerator on Zynq-7000 All Programmable SoC Devices
8. xapp918 - Incremental Design Reuse with Partitions
9. xapp290 - Differencing Method for Partial Reconfiguration
    a. This seems to be an alternate method to using reconfigurable regions, described in the other documents.
    b. It is not advised to use this method if routing changes are desired.
    c. This method is good for changing I/O standards, block RAM contents, and LUT programming.
10. `tool/fpga` contains code for (re)loading the FPGA fabric.
11. According to (5) and (6) above, one needs the base design as input to the partial reconfiguration `.bit`file generation step.
    a. See page 9 of (5).
12. Partial reconfiguration bitstream files seem to always be .bin files.
    a. Generate `.bin` files from `.bit` files using `promgen`.
13. According to UG743, "reconfigurable modules cannot have I/O buffers", so run XST project files with `-iobuf NO`.