PMC SLAC CAMAC Driver

PSCD

2030 Upgrade Project

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PSCD Overview

The PSCD provides in a PCI environment the same functionality that the MBCD and MBCDII provided in the SLC Multibus I environment.

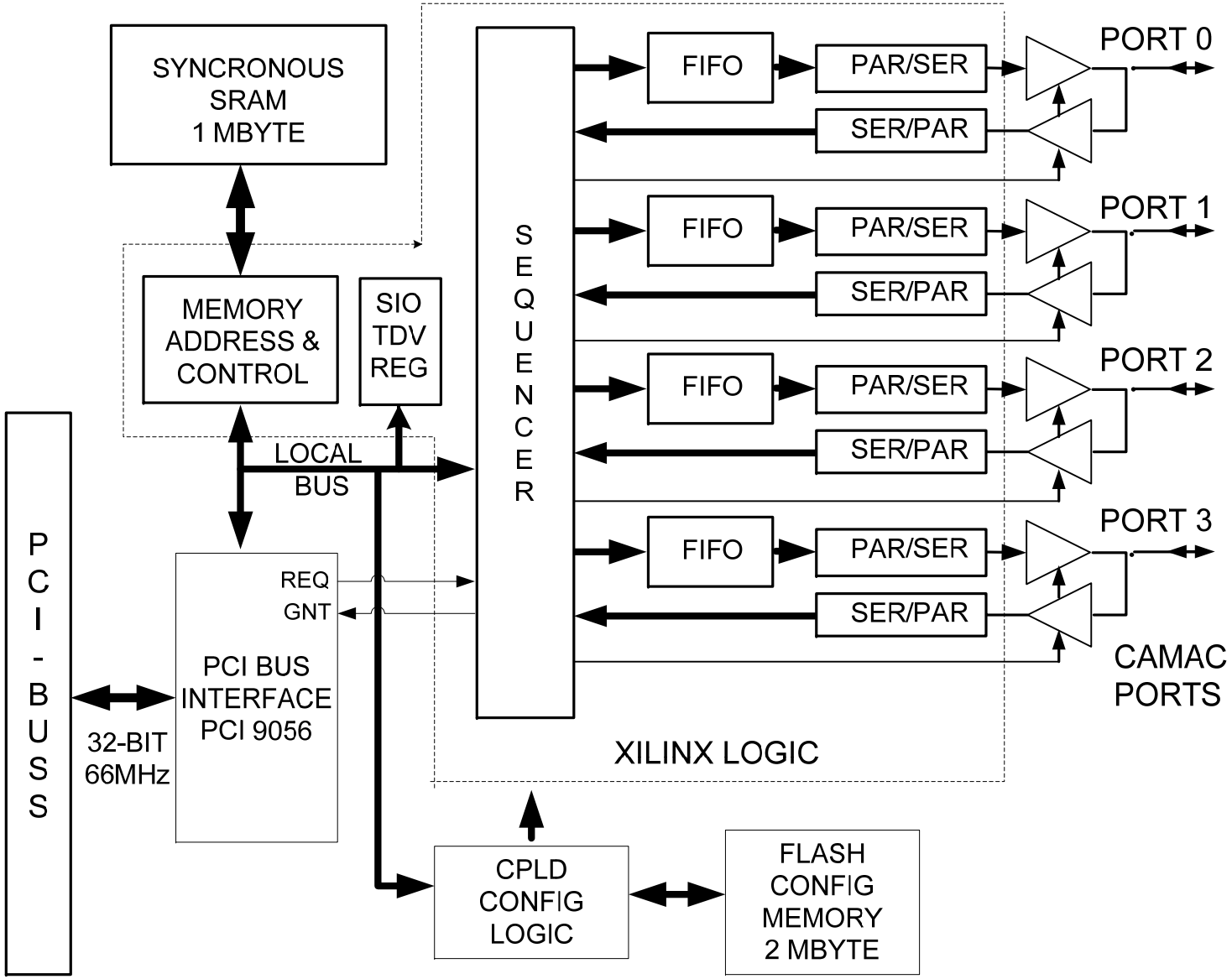
It provides high and low priority access to a SLAC Serial CAMAC branch. It is expected that the high priority path will be used for time critical applications such as the PPYY broadcast.

It also provides the same multi-port capability that is available in the MBCDII.

PSCD

- The PSCD will be a PMC slave module which executes CAMAC Packages directly from its local dual port memory.
- These CAMAC Packages are built up from one or more CAMAC packets.
- CAMAC operations are performed over the SLC standard serial highway using SLC Serial Crate Controllers (SCCs).
- Transmission is at a 5 Mbit/s serial rate.
- Typical CAMAC branch cycle times are between 12 and 15 microseconds per word

Block Diagram



Operation

- Upon receiving a memory pointer in the SIO register, the sequencer fetches a CAMAC Package from its Static Ram. As the Package is read in, it distributes each packet's CNAFs to the appropriate CAMAC Port Controller and FIFO.

- The CAMAC Port Controller, then executes cycles on the CAMAC Serial Link. Data and Status from this CAMAC operation are written into memory and upon completion of the CAMAC Package
- A new feature of the PSCD is that it will have three SIO registers. SIO(0) through SIO(2).
- SIO(0) is the highest priority.
  - Pointers written to this register will be acted on first. This will be used for writing time critical data like PPYY data to the PDUs and PIOPs.
  - Next, pointers written to SIO(1) register will be acted on. This can serve to read back BPM or PIOP data.
  - Lastly, SIO(2) will be used for non time critical data like SAMs, IDIMs, IDOMS etc.

Typical CAMAC Package

• CAMAC operations are started by writing a pointer value to one of the SIO registers.

• This pointer contains the address location in dual port ram of the CAMAC Package that will be executed.

• As mentioned previously, a CAMAC Package is a group of 1 or more CAMAC packets that are strung together one after the other to be executed consecutively.

Packet #	**Address**	**Value of MPC in the Control Word**
1st	SIO Pointer Value	MPC = 1 continue
2nd	SIO Pointer Value + 12d	MPC = 1 continue
3rd	SIO Pointer Value + 24d	MPC = 1 continue
n th	Previous Value +12d	MPC = 1 continue
last	Previous Value +12d	MPC = 0 **STOP after this packet executes**

CAMAC Packet Format

Word*	Name	Definition
0	CTLW	CAMAC control word
1	DATALOC	Address location of Data buffer
2	WCMAX ,CIC	Maximum word transfer max = 128 words CIC, Completion interrupt code NOT USED

* 32 bit words - These were six 16 bit words in the MBCD. Here they have been combined as three 32 bit words. To match the PCI bus.

CAMAC Packet Format cont.

- **CTLW:**

  Control word to be used for the following CAMAC cycle/s.

  (See format table).

- **DATALOC:**

  Pointer to the address of the data buffer to be used for the packet. The first 32 bit word of this data buffer will contain CAMAC status information after the packet has been executed. Read or write data will be written/read to/from the locations following this status information. (see **Data & Packet status)**

- **WCMAX:**

  A 7 bit number representing the maximum number of 16-bit words to be transferred.

- **CIC:** Completion Interrupt Code

  This was never used and was ultimately disabled.

CAMAC Packet Format cont.

Control Word Format

Bits 00	Name	Definition
0 1 2 3	A1 A2 A4 A8	Module Subaddress
6-4	Unused	3 Unused bits
7 8 9 10 11	N1 N2 N4 N8 N16	Module address (Station address)
12 13 14 15	C1 C2 C4 C8	Crate address
16 17 18 19 20	F1 F2 F4 F8 F16	CAMAC function code

CAMAC Packet Format cont.

Control Word – cont.

Bits 00	Name	Definition
21	SA	Enable subaddress counter
22	SN	Scan Module not used
23	Unused	Was SC, Scan Crate. . Not useful with multi-port operation
24	ILQ	Increment Sub-Address counter only if Q=0
25	IN	Reset Sub-Address counter if X=0
26	P24	24-bit mode (Pack 24) If set, data are read as 32-bit words, sign-extended from 24 bits. If reset, data are read as 16-bit words left truncated from 24 bits.
27	QM2	Terminate packet if Q=0
28	QM1	Transfer data if Q=1
29	XM2	Terminate packet if X=0
30	XM1	Transfer data if X=1
31	MPC	More Packets Coming 0 if last packet of package; 1 if more packets follow

CAMAC Packet Format cont.

Special mode bits description

- Bit 22, SN, Scan Module was never used in our system, This function is useful when there are many single width modules of the same type. For example a crate full of scalars or ADCs.
- Bit 23, SC, Scan Crate was discarded when we changed to multi-port operation with the MBCDII.
- Bit 26, P24, (Pack 24) A “1” indicates that data are read as 32-bit words, sign-extended from 24 bits. If “0”, data are read as 16-bit words left truncated from 24 bits.

Q or X Status Dependent Functions

- In general, a state Q = ”1” indicates that the data are valid. If Q = “0” then we may want to read the module again, increment to a new sub-address or terminate the CAMAC operation.
- In general, a state X = ”1” indicates that the module has correctly executed the CAMAC command it was given. If X = “0” we most likely want to terminate the CAMAC operation.

CAMAC Packet Format cont.

Q or X Status Dependent Functions cont.

- Bit 24, ILQ, Increment Sub-Address counter only if Q=0. This used to read all the valid data from an individual sub-address and then move to the next sub-address. Not generally used in our environment. Find use primarily in an experimental environment.
- Bit 25, IN, Increment N and Reset Sub-Address counter if X=0

•**CAMAC Mode Bits QM1, QM2 and XM1, XM2** are similar, however, since Q generally reflects the state of data and X the state the module or CAMAC transaction Bit 29, XM2, is set to terminate the packet if X= 0. XM1 is set to 0 because it maybe in conflict with QM1.

- Bit 29, XM2, Terminate packet if X=0
- Bit 30, XM1, Transfer data if X=1

•**CAMAC Mode Bits QM1, QM2 and Word Count (see table that follows)**

- Bit 27, QM2, Terminate packet if Q=0
- Bit 28, QM1, Transfer data if Q=1

Effect of CAMAC Mode Bits QM1, QM2

WC	Q	QM1	QM2	Meaning	STATUS BITS
= 0	0	0	0	Terminate; WC=0	BAR
= 0	0	0	1	Terminate; WC=0, Q=0	BAR, EMS
= 0	0	1	0	Retry	
= 0	0	1	1	Terminate; WC=0, Q=0; Reject Data	BAR, EMS
= 0	1	0	0	Terminate; WC=0	BAR
= 0	1	0	1	Terminate; WC=0	BAR
= 0	1	1	0	Terminate; WC=0	BAR
= 0	1	1	1	Terminate; WC=0	BAR
> 0	0	0	0	Next Word	
> 0	0	0	1	Terminate; Q=0	EMS
> 0	0	1	0	Retry	
> 0	0	1	1	Terminate; Q=0; Reject Data	EMS
> 0	1	0	0	Next Word	
> 0	1	0	1	Next Word	
> 0	1	1	0	Next Word	
> 0	1	1	1	Next Word	

Data & Packet status

- Read data and status are written into the buffer location specified in the control packet.
- The first two 32 bit word contains the packet status. The subsequent locations contain the data.

The data will be written into these locations on a CAMAC read operation and, read from these locations for a CAMAC write.

32 bit Packet Status	16 bit R/W data	16 bit R/W data	16 bit R/W data	

Packet Status Bits

Bits	Name	Definition
7-0	WCNT	Remaining Word Count. (Bit 7 = msb)
13 - 8	Unused	Unused, Reads 0.
14	LAM	LAM Status of CRATE
15	Unused	Unused, Reads 0.
16	Q	Q Status of last CAMAC operation
17	X	X Status of last CAMAC operation
18	EMS	End-Mode-Signal indicating that the packet was terminated by specified (non-zero) XM2, QM2 condition.
19	EOS	End-Of-Scan indicating that the packet was terminated by the overflow of the Sub-Address counter.
20	BAR	Q-Scan terminated on Word Count
21	CTO	Time-out on last CAMAC operation
22	DNE	DONE. Set if the CAMAC Package is Done. If in the single port compatibility mode, DONE is set in the Status of the Last Packet in the Package. If in the Mulit-Port mode, DONE is set in the Status of the Last Packet to complete.
27 - 23	MOD	Module Number of last CAMAC operation (Bit 27 = msb)
31 - 28	CRATE	Crate Number of last CAMAC operation (Bit 31 = msb)

Control Registers

Relative offset	Name	Definition
0	SIO0	Start Input/Output Channel 0 Highest Priority - Address of the CAMAC Package
4	SIO1	Start Input/Output Channel 1 , Mid-priority "
8	SIO2	Start Input/Output Channel 2, Lowest Priority "
C	PMAP0	Port mapping for Crates 1 - 7
10	PMAP1	Port mapping for Crates 8 - 15
14	TDV0	Status of Channel 0
18	TDV1	Status of Channel 1
1C	TDV2	Status of Channel 2

Control Registers, Bit Formats

Start I/O Register, 32-bit Rd/Wr registers

Name	Bit Field	Description
SIO0-SIO2	Bits [31:0]	32 Bit Starting Address of the CAMAC Package (low order 2 bits always “0”, 32 bit word aligned)

Since in the current design addresses are limited to the internal 1MByte of address space, an 18-bit address would be sufficient to address all of the available memory.

(Control Registers, Bit Formats cont.)

Port Mapping Registers

- There are four CAMAC serial ports on the PSCD.

The Port mapping registers are used to define which port a crate is attached. There are 16 nibbles that are defined in the two Port Mapping registers. The value of this nibble defines the port number, 0-3, to which the crates is physically connected.

Register	Bits 31-28	Bits 27-24	Bits 23-20	Bits 19-16	Bits 15-12	Bits 11-8	Bits 7-4	Bits 3-0
PMAP0	Crate 7	Crate 6	Crate 5	Crate 4	Crate 3	Crate 2	Crate 1	Not used
PMAP1	Crate 15	Crate 14	Crate 13	Crate 12	Crate 11	Crate 10	Crate 9	Crate 8

- A typical Klystron gallery location has only 4 crates and wiring for two ports thus it would appear as follows:

PMAP0	0000	0000	0000	0001	0001	0000	0000	0000
PMAP1	0000	0000	0000	0000	0000	0000	0000	0000

Note these registers are initialized to 0 on start-up. Thus all crates are assigned to port 0 until these registers are written

Status Registers, Bit Format

TDV Register Format TDV0 –TDV2

Bit	Name	Definition
0	DNE*	**Done,** but only valid if DNE = 1.
1	ERR	Summary hardware error
2	LAM	LAM status from any Crate
3	PND	**Pending** - Channel has not started execution
4	CTO	Time-out on last CAMAC operation
5	IAD	Invalid Buffer Offset Address
6	PTO	Package Time-Out
7	NBY	**Not Busy.** Bit 1,2,4, 6 are meaningful only if NBY =1
31-8	na	

* Reading this register clears the Done status bit DNE If it is set.

Status Register State Diagram for DONE, PENDING & NOT BUSY