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Signal Integrity Simulation and On-Chip Evaluation for Low-Cost FPGA Transceivers

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The increase of transceiver data rates over the years has challenged system designers in achieving design closure. Because signal integrity issues can become bottlenecks and jeopardize time-to-market goals, selecting the right productivity tools can be just as important as choosing the right FPGAs and transceiver support. Proper signal modeling, simulation, on-board analysis, and corrective techniques require both the right methodology and most advanced tool set.

The Xilinx 7 series GTP transceiver, available on Artix®-7 FPGAs, operates up to 6.6 Gb/s and is geared towards high performance for cost sensitive, high volume applications. With the highest line rate in its class, the 7 series GTP transceiver also offers the most advanced productivity tools to ensure proper signal integrity and system verification. This white paper describes how IBIS-AMI simulations and 2D Eye Scan—the industry's first on-chip scope for low cost FPGAs—can help analyze system margin at low bit error rates.

Introduction to High-Speed Serial Link Margin Analysis

The data rates of high-speed serial interfaces have been increasing consistently over the past decade. The higher data rates provide enough bandwidth to meet the demands of many new high-speed applications—but at the cost of additional system design and verification challenges.

At higher data rates, the channel attenuation increases but the bit sampling time decreases. Both changes negatively impact the data recovery from the received serial data stream. As the bit error rate (BER) required by a modern system is usually 10^{-12} or below, the channel compensation becomes more critical. For 6.6 Gb/s serial links, equalization techniques, such as transmitter (TX) emphasis and receiver (RX) linear equalization, have been popular to mitigate the channel attenuation. Meanwhile, selecting and verifying the right combination of equalization options and analyzing the link margin are equally critical.

The typical system design process starts with the transceiver selection and link trace budget estimation. The theoretical link margin is used to build confidence that the serial link will work with certain transceivers and projected PCB traces, connectors, cables, etc. The traditional solution has been HSPICE simulation. The accuracy of HSPICE simulation is desirable but the simulation time has become unrealistic for modern transceivers due to the complexity of the circuits.

When the PCB board design is completed and the physical link is ready, verification of the link margin is necessary to ensure that the system works not only the tested transceivers but also with the variation inherent in transceiver channels. The traditional verification solution uses long data streams to monitor the BER. However, sweeping through hundreds (even thousands) of equalization solutions for low BER is very time-consuming.

The Xilinx 7 series GTP transceiver on the Artix-7 FPGA provides programmable TX emphasis and RX linear equalization to mitigate the channel attenuation. The IBIS-AMI simulation model kit and eye scan (on-chip) are provided for signal quality analysis. This white paper describes how to benefit from these tools at different design stages.

Early Stage Link Margin Estimation

IBIS Algorithmic Modeling Interface (IBIS-AMI) has replaced HSPICE as the industry trend for early stage link margin analysis. Developed by the IBIS Advanced Technology Modeling (IBIS-ATM) working group, IBIS-AMI is a modeling standard for transceivers to enable fast and accurate simulation of multi-gigabit serial links. As a member of the IBIS Advanced Technology Modeling Group, Xilinx offers an IBIS-AMI model kit for each 7 series transceiver. The 7 Series GTP Transceiver IBIS-AMI Model Kit is one of them.

Figure 1 illustrates the blocks dedicated to achieving excellent signal integrity in the Xilinx Artix-7 FPGA GTP transceiver. All the shaded blocks — PLL, TX pre-emphasis, RX automatic gain control (AGC), RX linear equalization (EQ), RX clock data recovery (CDR), and adaptation block — are modeled in the GTP Transceiver IBIS-AMI Model Kit. TX and RX generic packages are also provided.

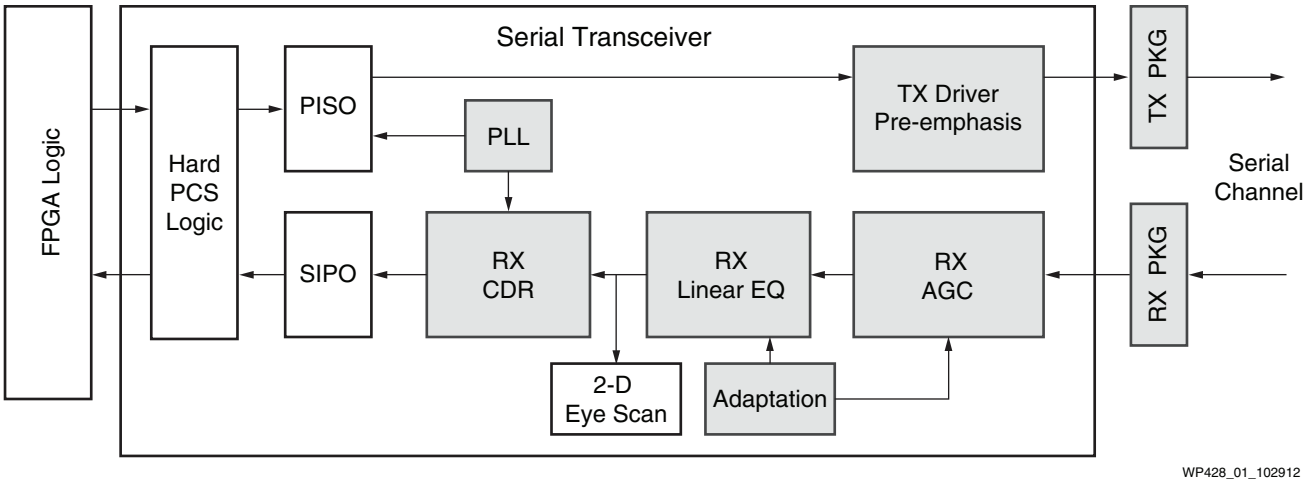

Figure 1: **Xilinx 7 Series GTP Transceiver Highlighting Signal Integrity Blocks**

The 7 series GTP transceiver IBIS-AMI models are fully compatible with the IBIS-AMI 5.0 standard. They have been verified with EDA tools from Agilent Technologies, Cadence Design Systems, Mentor Graphics, and SiSoft. In the following example, Sisoft QCD 2012.08 is used as the simulation vehicle to estimate the link margin.

Simulation-Based Link Margin Estimation Example

At the early stage of designing a 6.25 Gb/s serial link system, the goal is to evaluate whether the 7 series GTP transceiver can successfully compensate a 30-inch FR4 trace at a target bit error rate (BER) of 10^{-15}.

Figure 2 illustrates the simulation setup. The s-parameter file of the FR4 trace is placed between the GTP TX, TX package, and RX package, followed by the GTP RX. The post-equalization output is measured from the simulation.

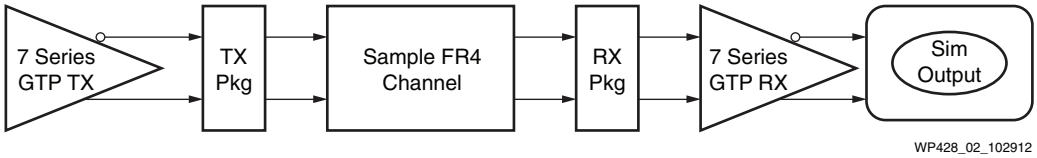

Figure 2: **Example of 7 Series GTP Transceiver Simulation Setup**

To mimic the physical environment in the simulation, the channel characteristics of the FR4 trace must be examined.This is done by extracting the s-parameter file from the physical trace board. The insertion loss based on the s-parameter file is shown in Figure 3. At the Nyquist frequency of 3.125 GHz, the total insertion loss is about 12.0 dB.

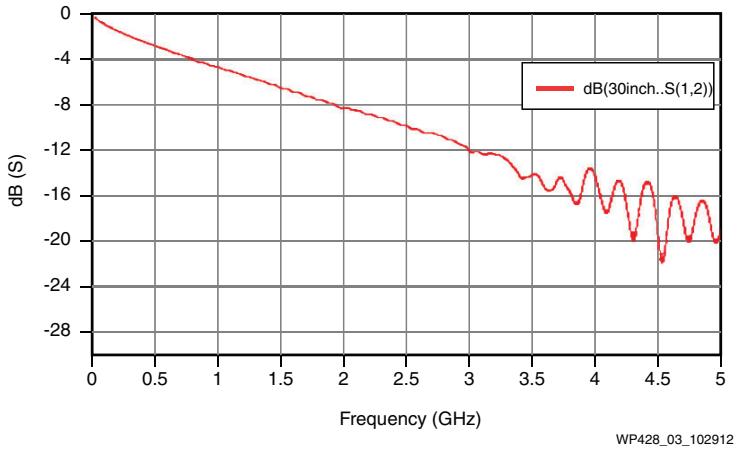

Figure 3: **Insertion Loss in Sample FR4 Trace Used in Simulation**

The next step is to set the TX and RX with appropriate equalization. In this example, the 7 series GTP RX's auto-adaptive equalization is enabled while the TX emphasis is turned off to test the receiver equalization and its auto-adaptation. The jitter characteristics of the TX and RX are also included in the simulation. 1 million bits of PRBS23 data stream were simulated in bit-by-bit mode.

Table 1 lists the parameters used in the simulation tool:

Table 1: **Simulation Parameters**

Line Rate	6.25 Gb/s (160 ps/UI)
Total Simulation Bits	1 million
Samples Per UI	64
Data Pattern	PRBS23
TX Swing	850 mV
TX Emphasis	OFF
RX EQ Adaptation	Auto
TX/RX Random Jitter (RMS)	0.0125 UI (2 ps)
TX/RX Dj	0.02 UI
TX DCD	0.02 UI

The result of the simulation is displayed as a post-equalization eye diagram (see Figure 4). At BER = 10^{-15} (extrapolated), the eye height measures about 230 mV and the eye width about 84 ps (0.53 UI).

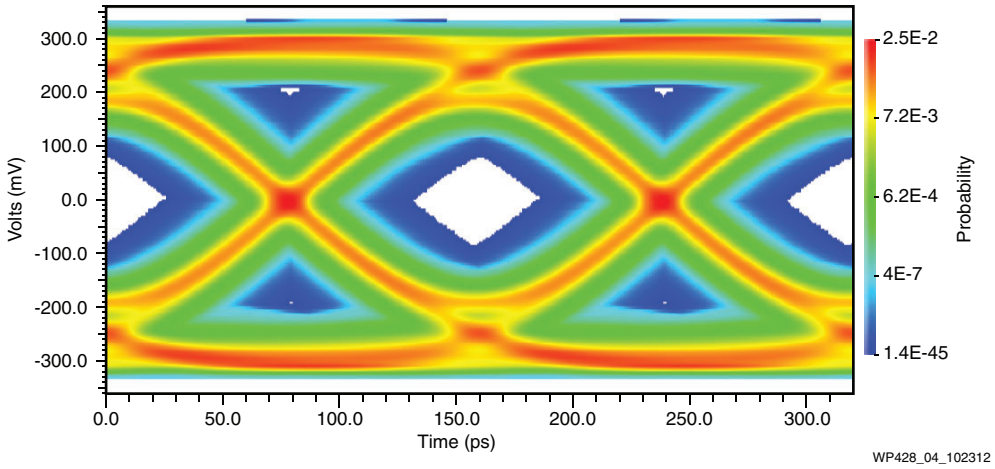

Figure 4: **IBIS-AMI Simulation Result with 7 Series GTP Transceiver**

The 7 series GTP transceiver requires post-equalization eye height of 100 mV and eye width of 0.35 UI in simulation to guarantee the BER performance. The margin for both eye height and eye width is calculated as:

Height Margin:	230/100 – 1	=	130%
Width Margin:	0.53/0.35 – 1	=	51.43%

Therefore, based on the simulation, the link with 7 series GTP transceivers and 30-inch FR4 shows sufficient margin to achieve BER = 10^{-15}, from both eye height and eye width perspectives.

Physical Link Margin Analysis with 7 Series GTP On-Chip Eye Scan

In the IBIS-AMI simulation, it was estimated that the 6.25 Gb/s serial link using a 7 series GTP transceiver and 30 inches of FR4 can achieve BER = 10^{-15} with sufficient margin. The following board verification example uses a physical system that includes a 7 series GTP transceiver characterization board and the 30-inch FR4 trace board to quantify the link margin utilizing the eye scan feature and the IBERT tool in the ChipScope™ Analyzer.

Introduction to Eye Scan

Eye scan is an on-chip scope to visualize post-equalization signal quality in an RX. As described in Figure 5, eye scan runs a separate sampler in parallel with the CDR data sampler. The horizontal (time) and vertical (amplitude) offsets of the new sampler are configurable. For each offset setting, a specified number of bits are transmitted. The data and offset samples are compared sequentially. When the two samples are not equal, the error counter is incremented. Bit error rate can be calculated by dividing the error counts by the number of bits transmitted.

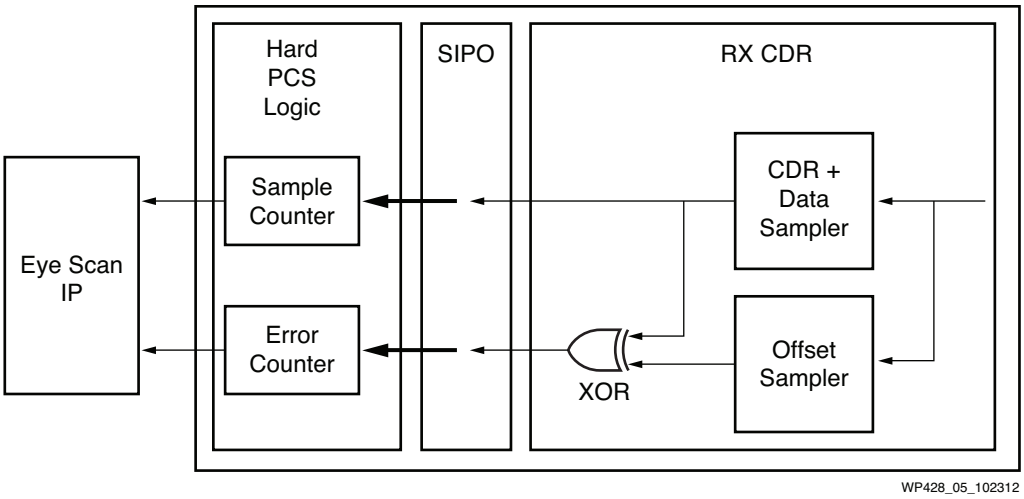

Figure 5: **Eye Scan Uses Both CDR Data Sampler and Offset Sampler**

The eye scan IP tool moves the offsets across the complete eye, calculates the BER for each offset setting, then correlates the BER and offset to statistically rebuild the eye diagram. Figure 6 illustrates the movement of the offsets and shows the resulting statistically rebuilt eye diagram based on the BER records.

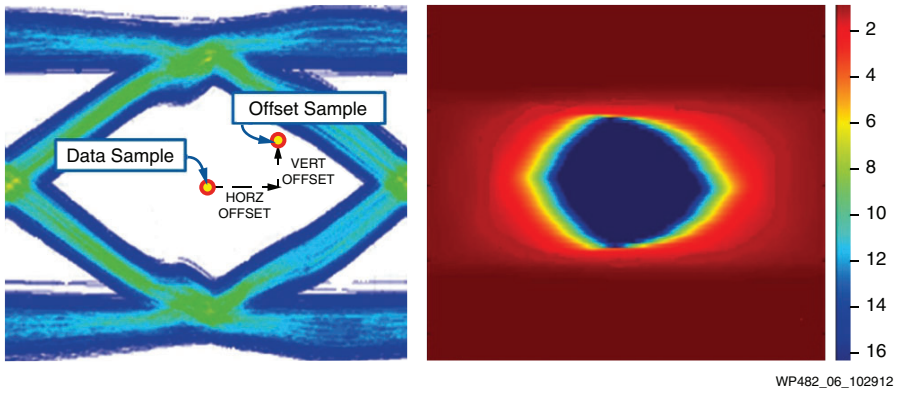

Figure 6: **Eye Scan IP Controls Offsets and Statistically Rebuilds an Eye Diagram**

If the vertical offset is fixed at 0, the BER eye scan records, using different horizontal offsets, can be used to build the bath-tub curve for this link.

The eye contours of different BERs converge as BER decreases. Thus, it is feasible to extrapolate the contour of a low BER from contours of higher BERs.

Without eye scan, the serial link performance for a target low BER (usually < 10^{-12}) is done by running long bitstream testing. The test time is proportional to BER. For example, at 6 Gb/s, it takes about: 3 minutes to reach raw BER of 10^{-12}; 2,780 minutes to reach 10^{-15}, and 193 days to reach 10^{-17}.

Moreover, the number of combinations of swing, post-emphasis, and pre-emphasis can easily run into the hundreds, and this number becomes the multiplier for the single-run test time. If the receiver equalization is also manually controlled, the test times then increase exponentially by the number of receiver equalization settings. It is simply too long to be practical.

Even if a single setting (or a small number of settings) can achieve the target BER with a certain confidence, determining the optimal equalization settings remains difficult to ascertain by monitoring link BER with long bit streams.

In addition, the BER monitoring does not quantify the link margin, which reduces the confidence, considering the impact of the variation of the transceiver channels.

Eye scan can help address these concerns and questions. Together with the appropriate IP tools, on-chip eye scan can analyze system margin using the following steps:

1. Generate bath-tub curves or eye contours from different equalization settings at a relatively high BER — for example, 10^{-8}. This process usually takes minutes to hours, depending on the number of settings.
2. Identify the optimal settings by comparing the margin indicated by the bath-tub curves or eye contours.
3. Quantify the vertical and horizontal system margins with eye contours at the *low* BER and the eye mask provided. Use extrapolation to reach target BER as necessary.
4. Verify system performance by running a single long bitstream test using the identified optimal settings.

All 7 series transceivers are equipped with 2D eye scan. The 7 series GTP transceiver is the first low-cost, high-volume FPGA in the industry to include such a feature.

IBERT in ChipScope Analyzer with Incorporated Eye Scan

Xilinx provides a unique tool for verification of Xilinx transceivers: IBERT in the ChipScope Analyzer. It allows a serial designer to dynamically control the selected transceivers by modifying the transceiver settings, setting the loopback mode, selecting the test pattern, and monitoring the serial link status with parameters such as line rate and bit error rate. Figure 7 shows a screen shot of the IBERT main tab with all the controls listed above.

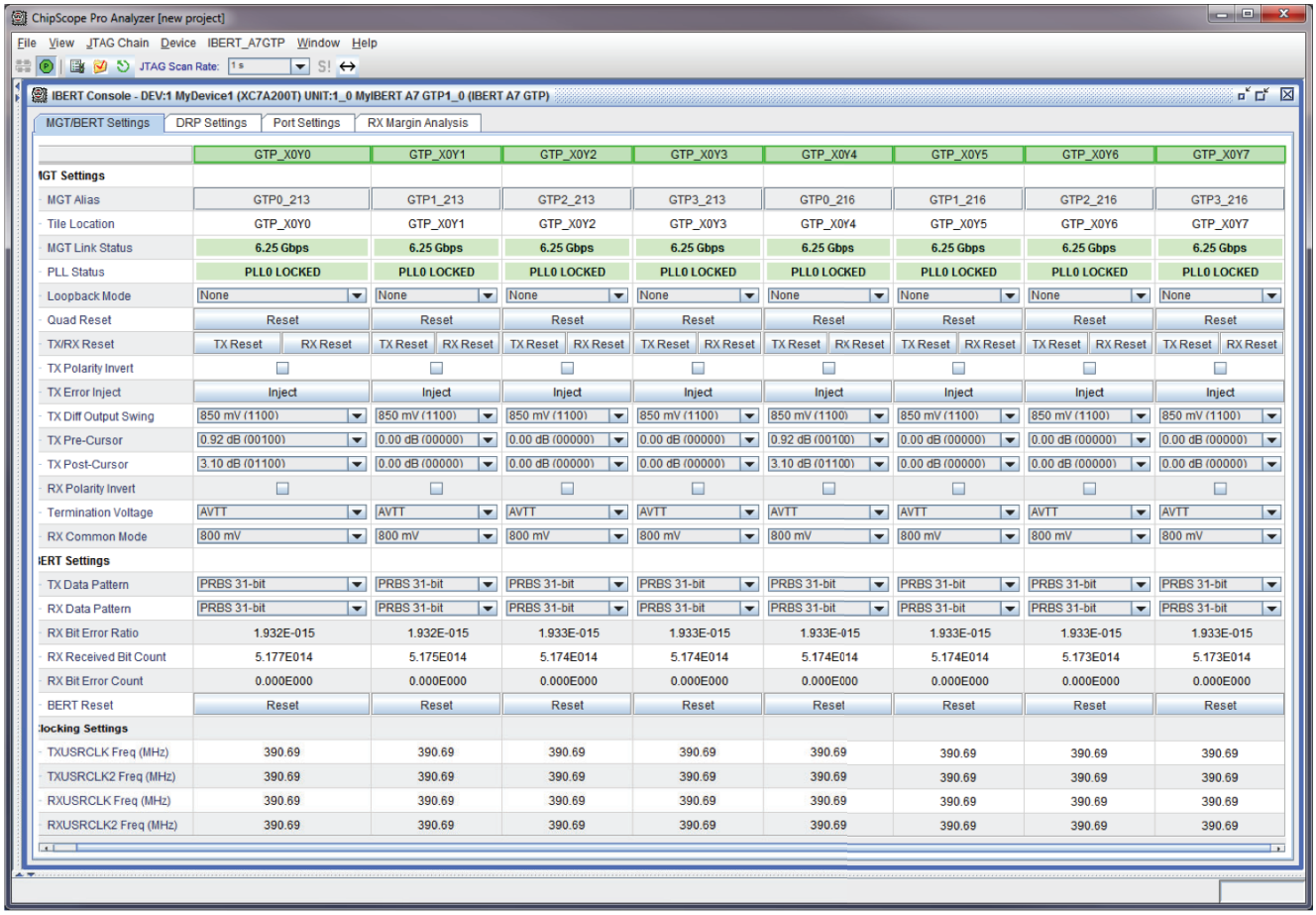

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Figure 7: **The Main Tab of IBERT GUI Running Eight GTP Serial Links**

At 28 nm, the IBERT is improved to incorporate eye scan. The **RX Margin Analysis** GUI tab has the capability to:

1. Select serial link
2. Set sweeping parameters such as TX Emphasis settings
3. Select scan settings: 1-D bath-tub curve, or 2-D Eye, Scan Resolution, and Target BER

Figure 8 is a screen shot of the RX margin analysis tab with the above features highlighted.

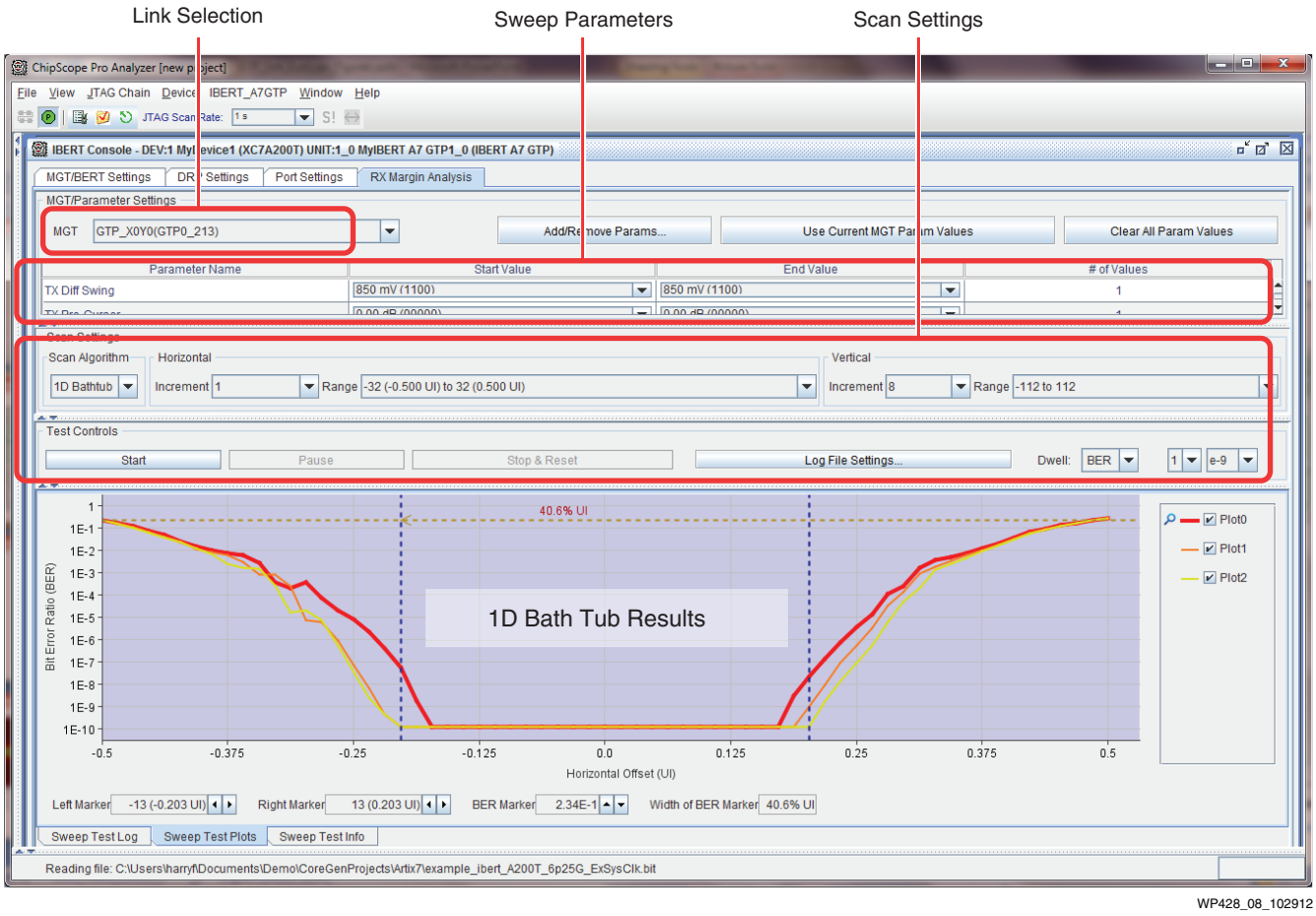

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Figure 8: **The RX Margin Analysis Tab of the IBERT GUI**

Eye Scan Based Link Margin Analysis Example with 30-inch FR4 Trace

Utilizing the RX Margin Analysis with eye scan, the system margin of the 6.25 Gb/s serial link with 30-inch FR4 trace connecting a 7 series GTP TX and RX can be evaluated. Table 2 lists the test setup. The TX swing, emphasis and RX EQ settings are all the same as those used in the simulation.

Table 2: **Hardware Test Setup**

Test Board and Device	AC 722 Characterization Board with A200T
Line Rate	6.25 Gb/s
Data Pattern	PRBS31
TX Swing	850 mV
TX Emphasis	OFF
RX EQ Adaptation	Auto
Link Trace Board	30-inch FR4
Eye Scan Target BER	10^{-8}
Eye Scan Vertical / Horizontal Resolution	2/2

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Figure 9: **AC722 Characterization Board with Cables and Connectors**

The statistical eye captured by eye scan at BER = 10^{-8} is shown in Table 10. The eye height measures ~100 (vertical codes). Thus, the measured eye height is ~200 mV. The eye width measures ~ 0.56 UI.

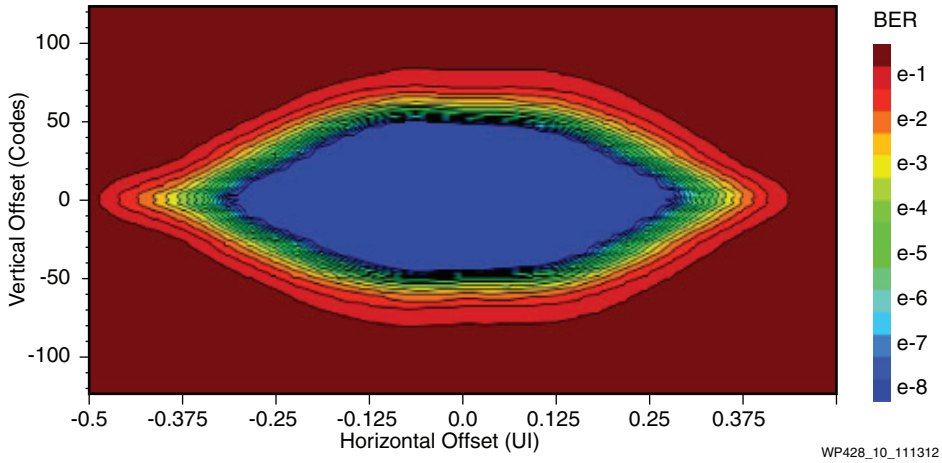

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Figure 10: **7 Series GTP Eye Scan Result with 30-Inch FR4 Measured on AC722 Characterization Board**

From the eye contours at BERs of no less than 10^{-8}, the eye shrink from BER = 10^{-8} to BER = 10^{-15} is estimated to be less than 5 codes vertically and 0.05 UI horizontally. Thus, the eye opening at BER = 10^{-15} is estimated to be no smaller than 95 vertical codes high and 0.51 UI wide.

Applying the eye mask of 50 vertical codes and 0.35 UI to guarantee BER performance with channel variations:

Height Margin:	95/50-1	=	90%
Width Margin:	0.51/0.35 – 1	=	45.7%

Therefore, similar to the simulation results, the eye scan measurement shows that the link built with a 7 series GTP transceiver and 30-inch FR4 has enough system margin to achieve BER = 10^{-15}. The BER shown in Figure 7, page 8 is the result of 24-hour testing; it reaches BER = $1.9x10^{-15}$ without a single bit error.

Summary

The Xilinx 7 series GTP transceivers provide programmable equalization options to mitigate channel attenuations. An IBIS-AMI simulation kit is available to do link margin estimation on projected link channels. The on-chip 2D eye scan feature also enables customers to quantify link margin with real hardware. With appropriate extrapolation, link margin at very low BER is achievable from both simulation and eye scan.

Go to WP419, *Equalization for High-Speed Serial Interfaces in Xilinx 7 Series FPGA Transceivers* for more information about equalization options.

The IBIS-AMI model kit can be requested through Xilinx FAEs and I/O Specialists.

Detailed information regarding on-chip eye scan can be found in UG482, *7 Series FPGAs GTP transceivers User Guide*. This white paper utilizes the IBERT tool in the ChipScope Analyzer to enable eye scan. To implement eye scan in a customized design, refer to XAPP743, *Eye Scan with MicroBlaze Processor MCS*.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/07/2017	1.0.1	Typographical edits.
11/30/2012	1.0	Initial Xilinx release.

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